



**ALPHA & OMEGA**  
SEMICONDUCTOR

**AOTF4126**

**100V N-Channel MOSFET**  
**SDMOS™**

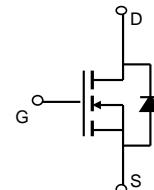
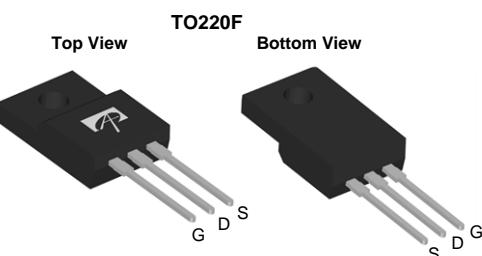
### General Description

The AOTF4126 is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

### Product Summary

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	27A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 24mΩ
$R_{DS(ON)}$ (at $V_{GS} = 7V$ )	< 30mΩ

100% UIS Tested  
100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current <sup>B</sup>	$I_D$	27	A
$T_C=100^\circ C$		19	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	110	
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	6	A
$T_A=70^\circ C$		5	
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	28	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	39	mJ
Power Dissipation <sup>B</sup>	$P_D$	42	W
$T_C=100^\circ C$		21	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.1	W
$T_A=70^\circ C$		1.4	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	10	12	°C/W
Maximum Junction-to-Ambient <sup>A,D</sup>		48.5	58	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	2.9	3.5	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	100			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			10 50	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm25\text{V}$			100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2	3.3	4	V
$I_{D(\text{ON})}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	100			A
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$		19 36	24 43	$\text{m}\Omega$
		$V_{GS}=7\text{V}, I_D=15\text{A}$		23.5	30	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		34		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.66	1	V
$I_S$	Maximum Body-Diode Continuous Current				40	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=1\text{MHz}$	1400	1770	2200	pF
$C_{oss}$	Output Capacitance		115	165	214	pF
$C_{rss}$	Reverse Transfer Capacitance		33	55	80	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$	0.3	0.65	1.0	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, I_D=20\text{A}$	14	28	42	nC
$Q_{gs}$	Gate Source Charge		4	9	14	nC
$Q_{gd}$	Gate Drain Charge		6	10	14	nC
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, R_L=2.5\Omega, R_{GEN}=3\Omega$		12		ns
$t_r$	Turn-On Rise Time			4		ns
$t_{D(\text{off})}$	Turn-Off Delay Time			17		ns
$t_f$	Turn-Off Fall Time			5		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	12	20	26	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, dI/dt=500\text{A}/\mu\text{s}$	60	82	110	nC

A. The value of  $R_{QJA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{QJA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature  $T_{J(\text{MAX})}=175^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J=25^\circ\text{C}$ .

D. The  $R_{QJA}$  is the sum of the thermal impedance from junction to case  $R_{QJC}$  and case to ambient.

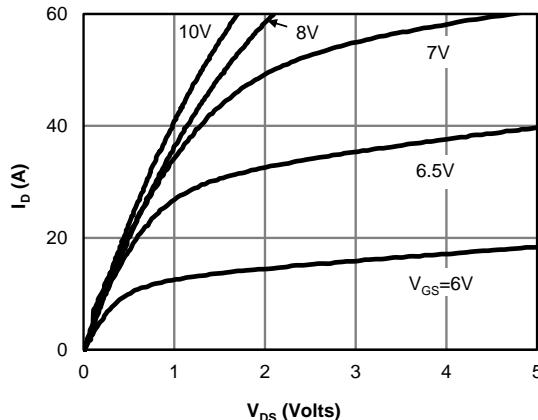
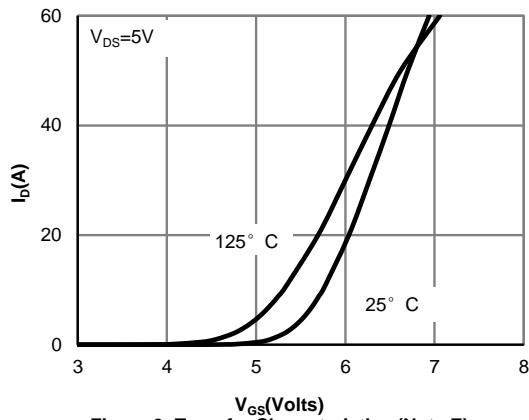
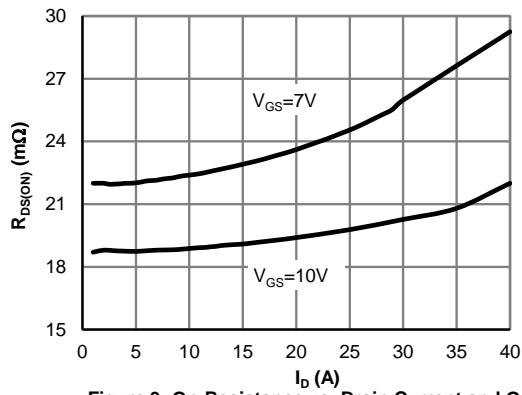
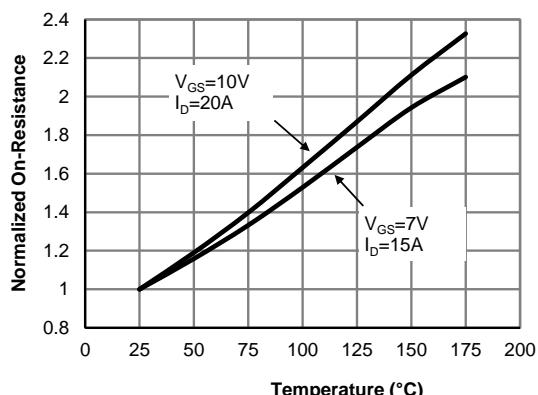
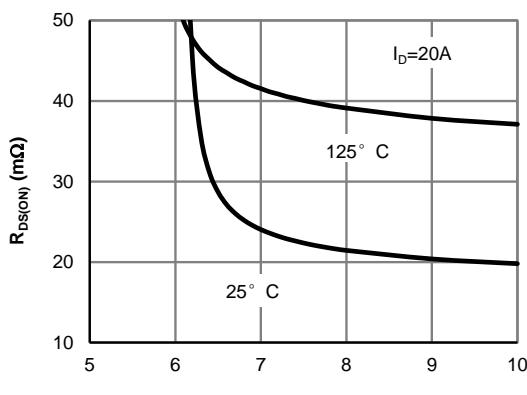
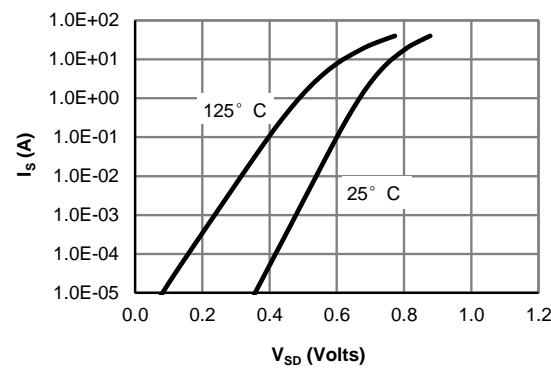
E. The static characteristics in Figures 1 to 6 are obtained using <300 $\mu\text{s}$  pulses, duty cycle 0.5% max.

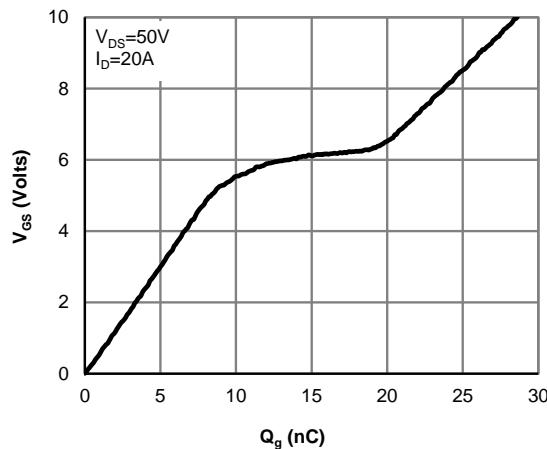
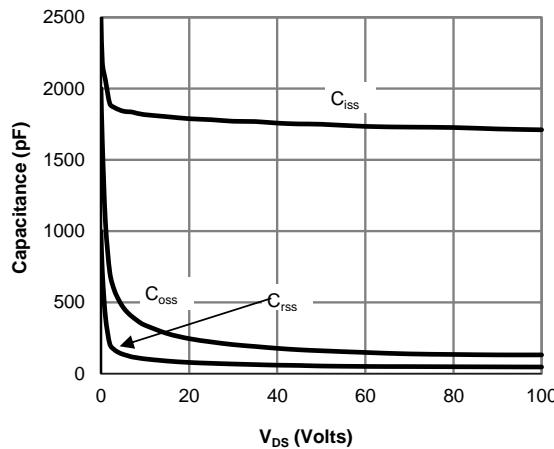
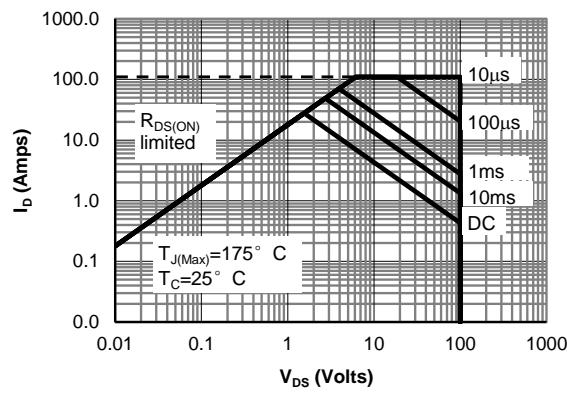
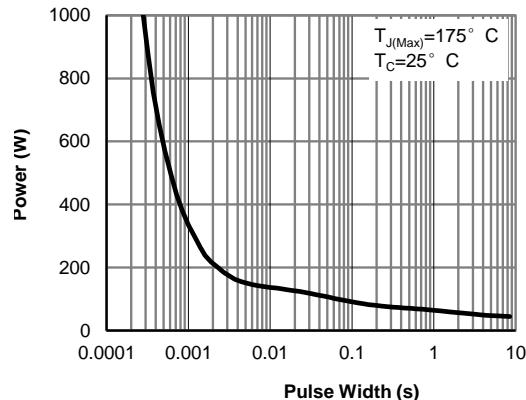
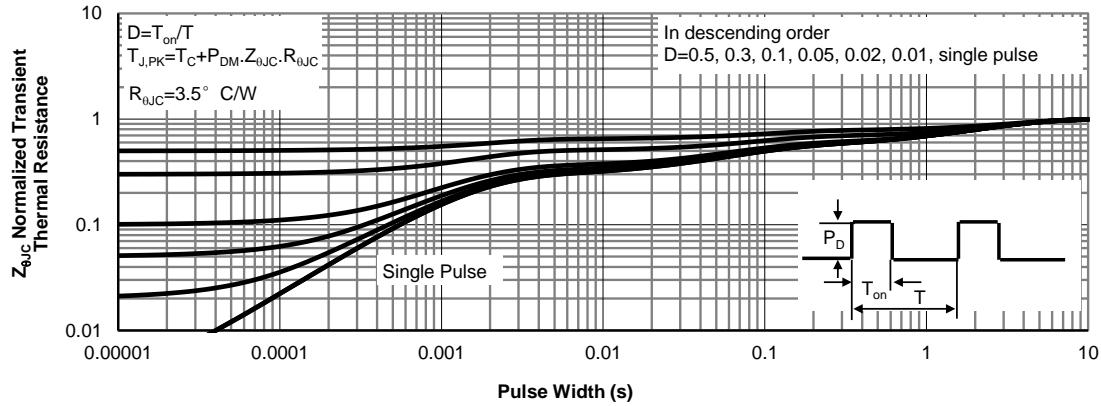
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})}=175^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Fig 1: On-Region Characteristics (Note E)**

**Figure 2: Transfer Characteristics (Note E)**

**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

**Figure 6: Body-Diode Characteristics (Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 7: Gate-Charge Characteristics**

**Figure 8: Capacitance Characteristics**

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

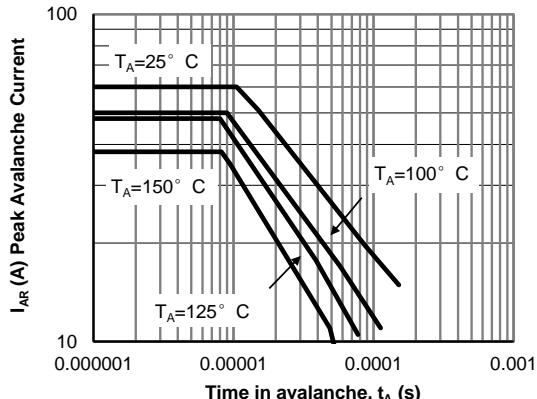
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 12: Single Pulse Avalanche capability (Note C)

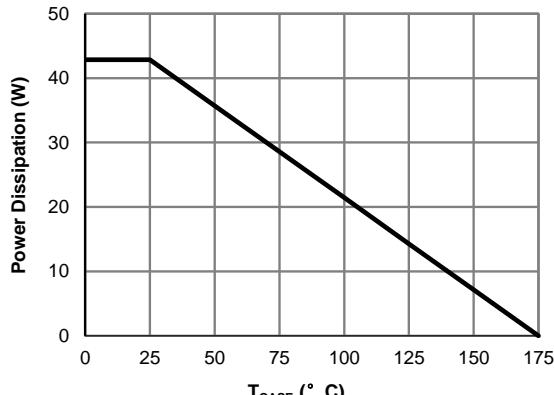


Figure 13: Power De-rating (Note F)

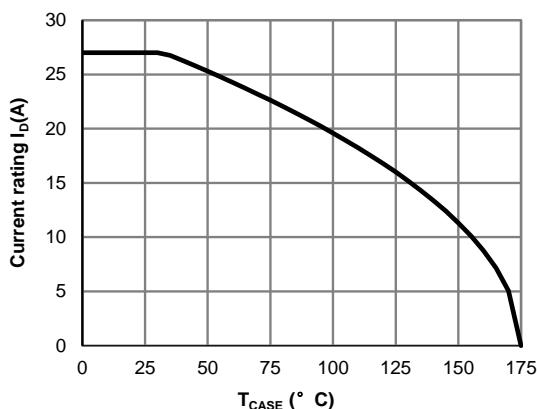


Figure 14: Current De-rating (Note F)

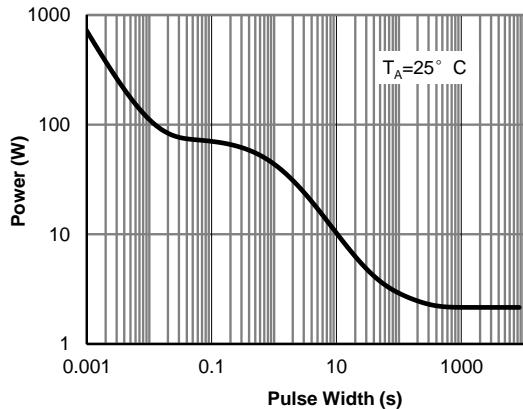


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

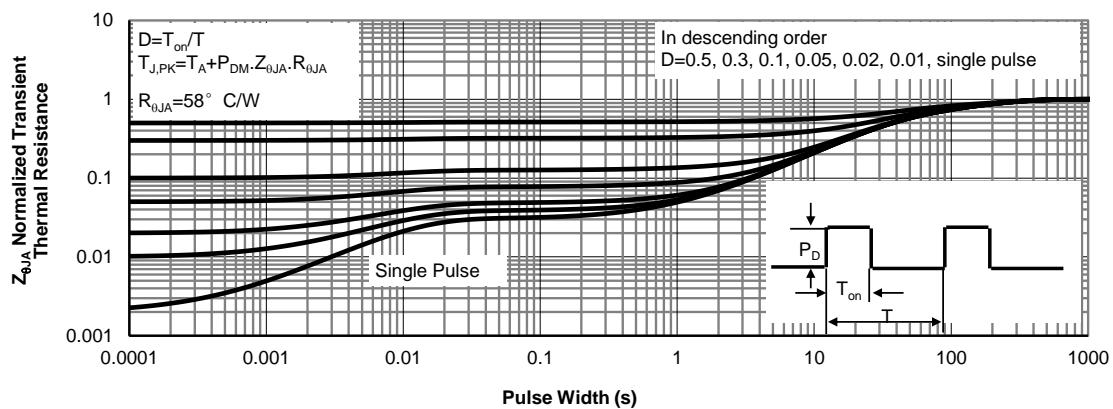


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

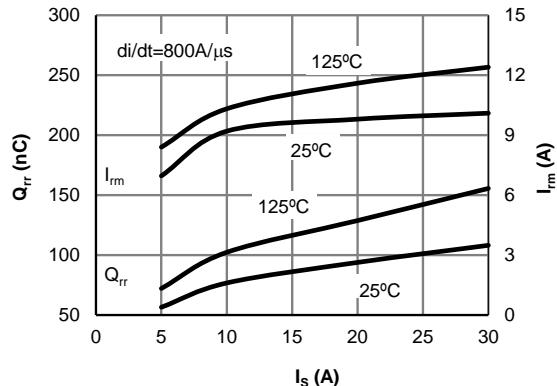
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

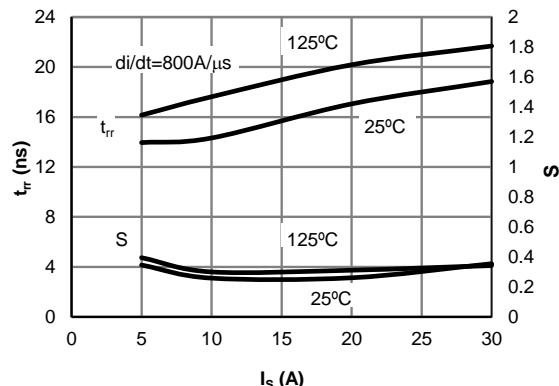


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

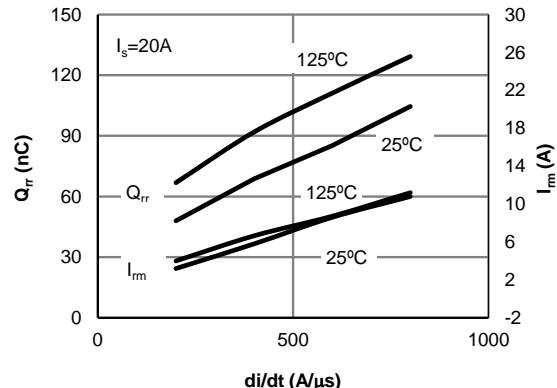


Figure 19: Diode Reverse Recovery Charge and Peak Current vs.  $\frac{di}{dt}$

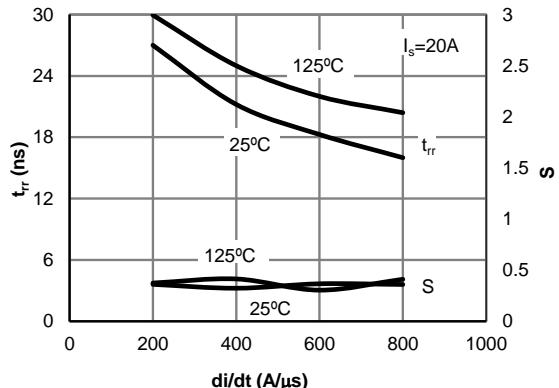
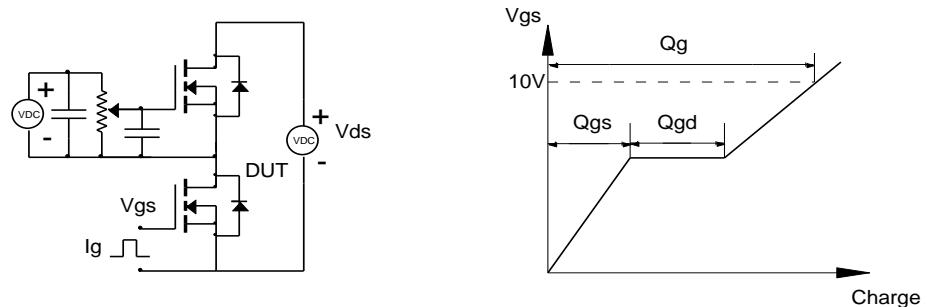
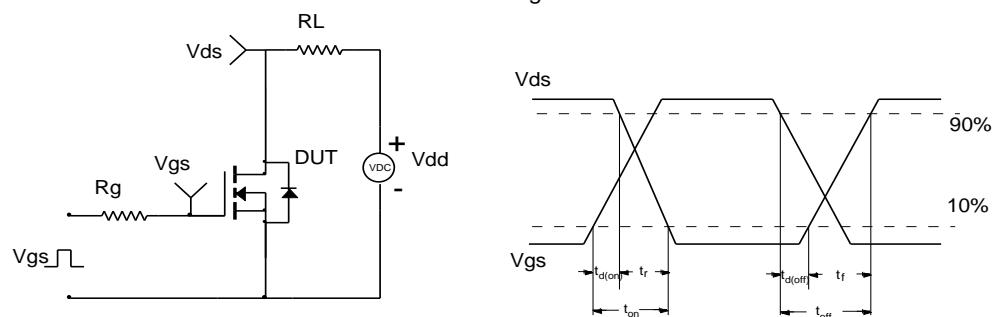
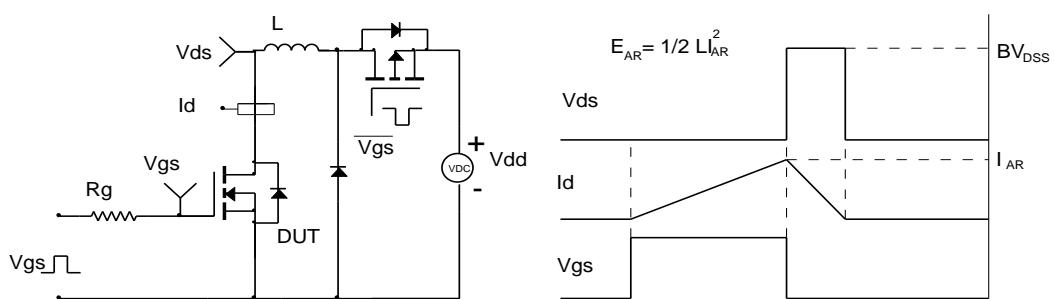


Figure 20: Diode Reverse Recovery Time and Softness Factor vs.  $\frac{di}{dt}$

**Gate Charge Test Circuit & Waveform**

**Resistive Switching Test Circuit & Waveforms**

**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

**Diode Recovery Test Circuit & Waveforms**
