

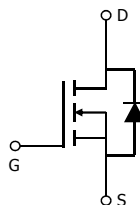
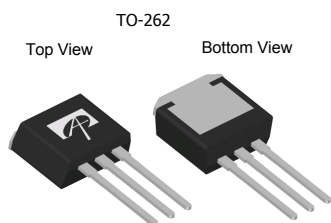
**General Description**

The AOW298 uses Trench MOSFET technology that is uniquely optimized to provide the most efficient high frequency switching performance. Power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $C_{rSS}$ . In addition, switching behavior is well controlled with a soft recovery body diode. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.

**Product Summary**

$V_{DS}$	100V
$I_D$ (at $V_{GS}=10V$ )	58A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 14.5m $\Omega$

100% UIS Tested  
 100%  $R_g$  Tested


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	58
		$T_C=100^\circ C$	41
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	130	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ C$	9
		$T_A=70^\circ C$	7
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	20	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	20	mJ
$V_{DS}$ Spike <sup>I</sup>	$V_{SPIKE}$	120	V
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	100
		$T_C=100^\circ C$	50
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	2.1
		$T_A=70^\circ C$	1.33
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	12	15	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A D</sup>		Steady-State	50	60
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	1.5	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.7	3.3	4.1	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	130			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		12 19	14.5 24	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		30		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				70	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1MHz		1250	1670	pF
C <sub>oss</sub>	Output Capacitance			727	970	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			25	43	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		2	3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, I <sub>D</sub> =20A		19	27	nC
Q <sub>gs</sub>	Gate Source Charge			5.5		nC
Q <sub>gd</sub>	Gate Drain Charge			6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =50V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		7.5		ns
t <sub>r</sub>	Turn-On Rise Time			14		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			15		ns
t <sub>f</sub>	Turn-Off Fall Time			14		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =20A, dI/dt=500A/μs		39	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		140		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>D(SM)</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

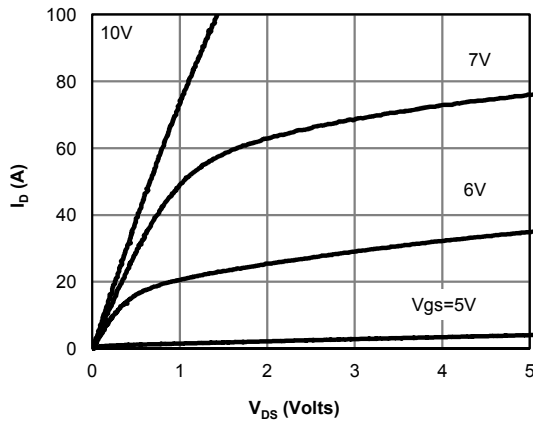
G. The maximum current limited by package.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

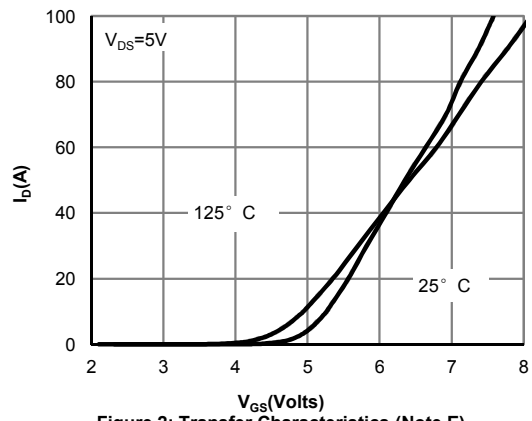
I. The spike duty cycle 5% max, limited by junction temperature T<sub>J(MAX)</sub>=120° C.

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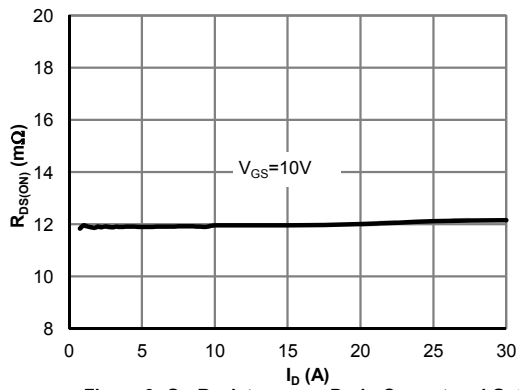
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



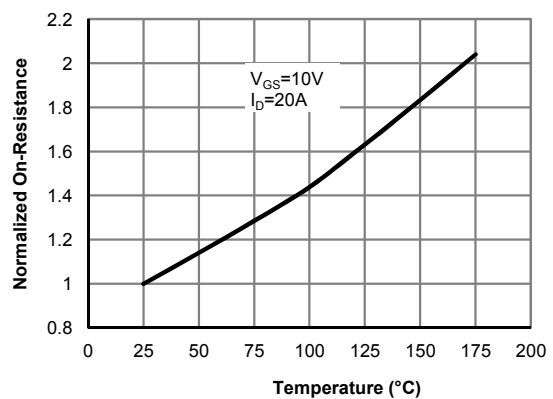
**Fig 1: On-Region Characteristics (Note E)**



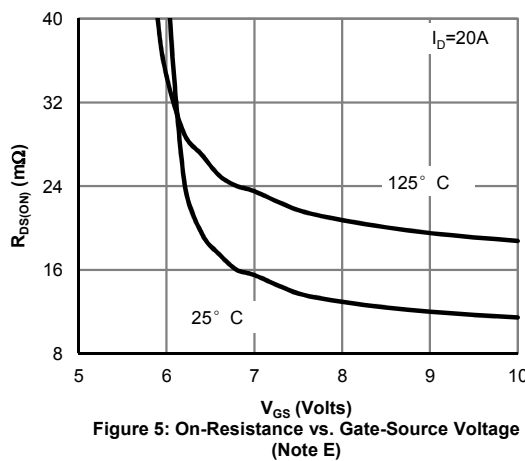
**Figure 2: Transfer Characteristics (Note E)**



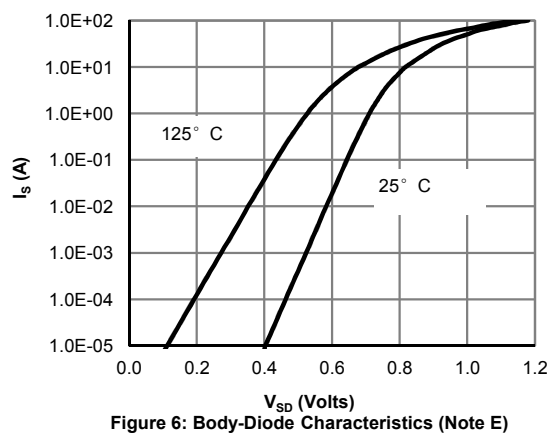
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

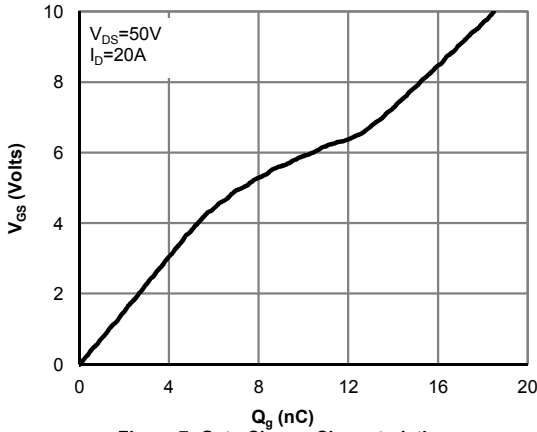


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

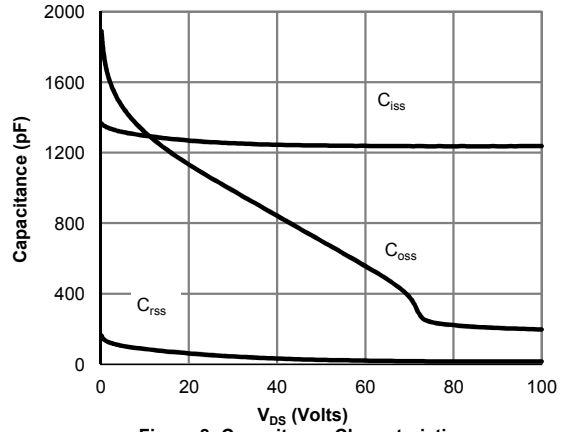


**Figure 6: Body-Diode Characteristics (Note E)**

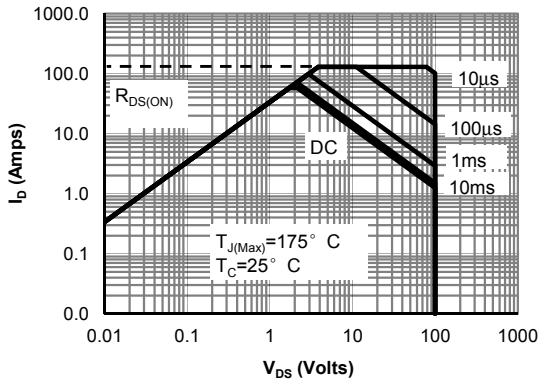
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



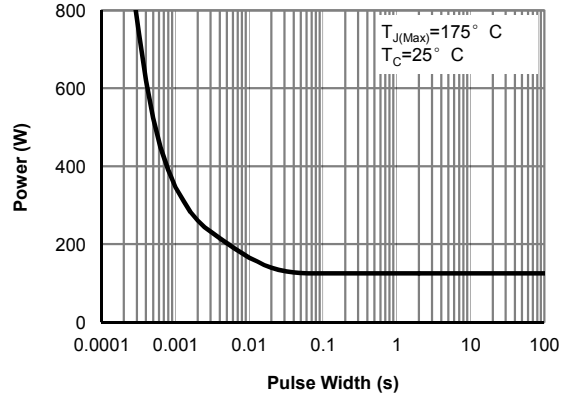
**Figure 7: Gate-Charge Characteristics**



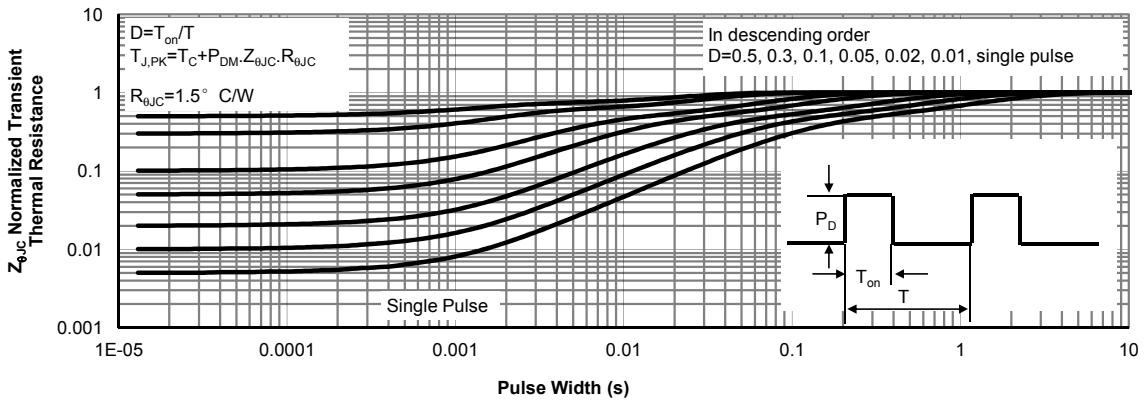
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case for (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

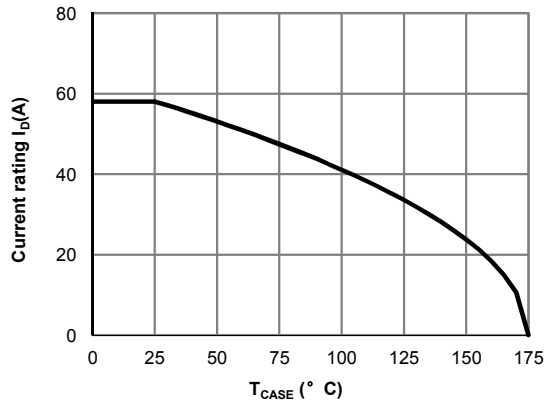


Figure 17: Current De-rating (Note F)

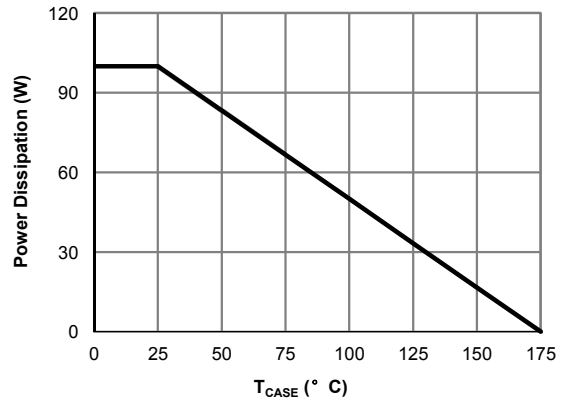


Figure 18: Power De-rating (Note F)

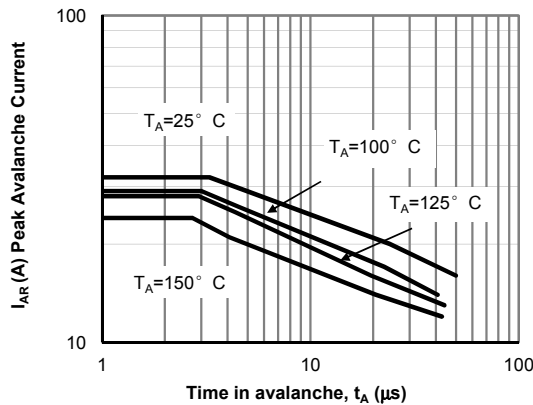


Figure 19: Single Pulse Avalanche capability (Note C)

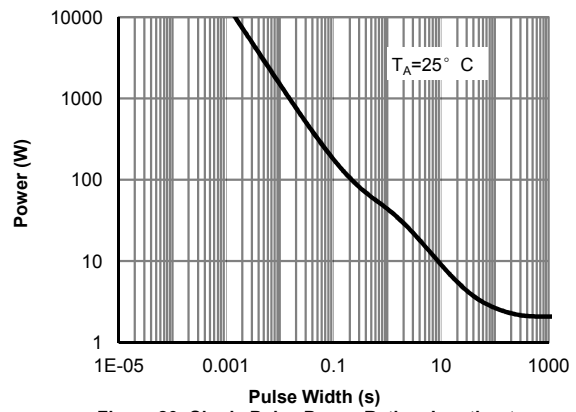


Figure 20: Single Pulse Power Rating Junction-to-Ambient (Note H)

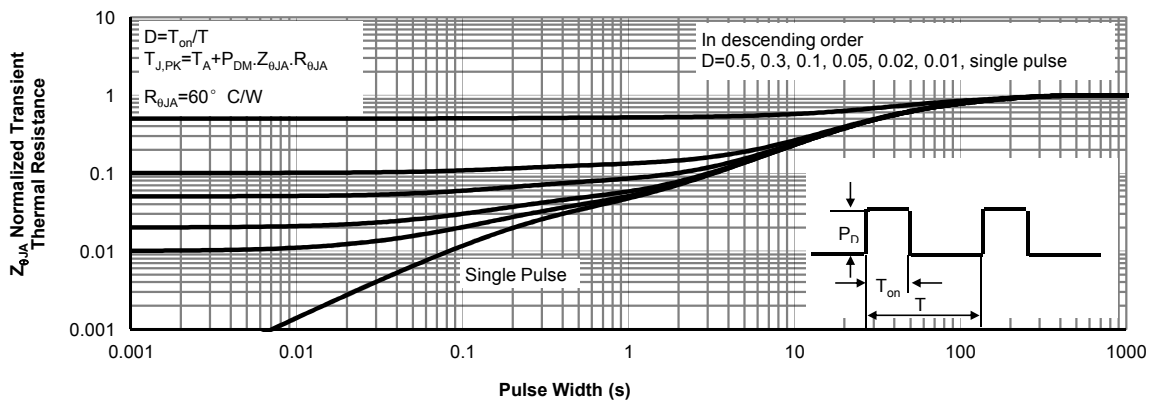
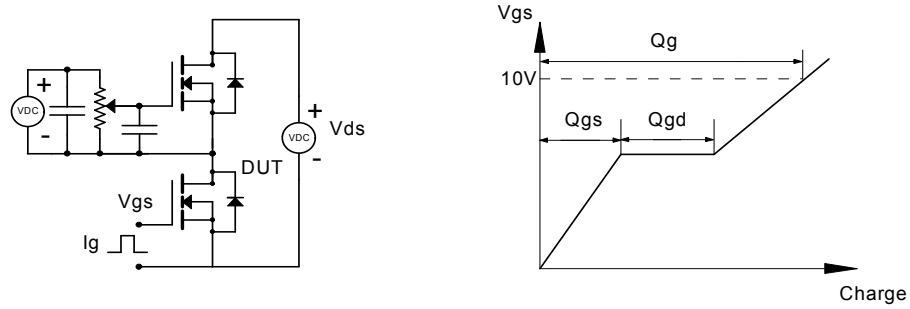
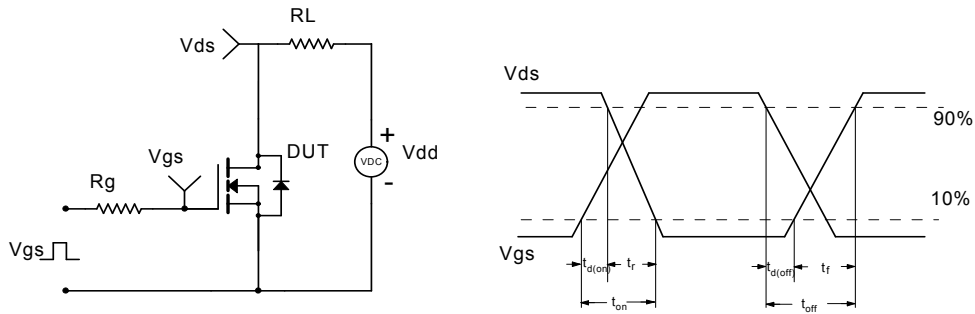


Figure 21: Normalized Maximum Transient Thermal Impedance (Note H)

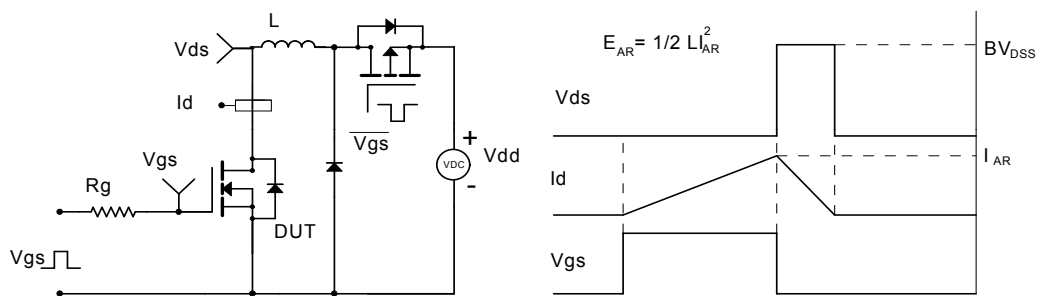
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

