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AOW7S65/AOWF7S65
650V 7A αMOS™ Power Transistor

## General Description

The AOW7S65 & AOWF7S65 have been fabricated using the advanced αMOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications.
By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

Product Summary

V_{DS} @ $T_{j,max}$	750V
I_{DM}	30A
$R_{DS(ON),max}$	0.65Ω
$Q_{g,typ}$	9.2nC
E_{oss} @ 400V	2μJ

100% UIS Tested
100% R_g Tested

Green Product

TO-262 Top View Bottom View
AOW7S65
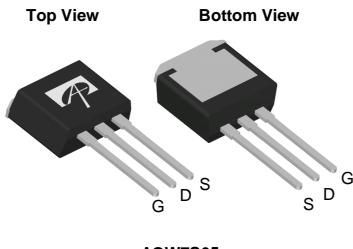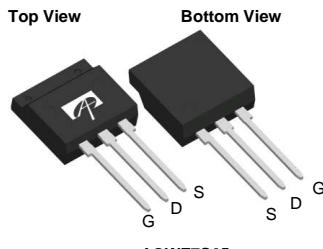
TO-262F Top View Bottom View
AOWF7S65
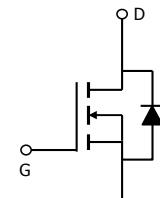
Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	AOW7S65	AOWF7S65	Units
Drain-Source Voltage		V_{DS}	650		V
Gate-Source Voltage		V_{GS}	±30		V
Continuous Drain Current	T_C=25℃	I_D	7	7*	A
	T_C=100℃		5	5*	
Pulsed Drain Current [C]		I_{DM}	30		
Avalanche Current [C]		I_{AR}	1.7		A
Repetitive avalanche energy [C]		E_{AR}	43		mJ
Single pulsed avalanche energy [G]		E_{AS}	86		mJ
Power Dissipation [B]	T_C=25℃	P_D	104	25	W
	Derate above 25°C		0.8	0.2	W/ °C
MOSFET dv/dt ruggedness		dv/dt	100		V/ns
Peak diode recovery dv/dt [H]			20		
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		℃
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds [J]		T_L	300		℃

Thermal Characteristics

Parameter	Symbol	AOW7S65	AOWF7S65	Units
Maximum Junction-to-Ambient [A,D]	$R_{θJA}$	65	65	℃/W
Maximum Case-to-sink [A]	$R_{θCS}$	0.5	--	℃/W
Maximum Junction-to-Case	$R_{θJC}$	1.2	5	℃/W

* Drain current limited by maximum junction temperature.

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Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V, T$_J$=25℃	650	-	-	V
		I$_D$=250µA, V$_{GS}$=0V, T$_J$=150℃	700	750	-	
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=650V, V$_{GS}$=0V	-	-	1	µA
		V$_{DS}$=520V, T$_J$=150℃	-	10	-	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±30V	-	-	±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=5V,I$_D$=250µA	2.6	3.3	4	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=3.5A, T$_J$=25℃	-	0.54	0.65	Ω
		V$_{GS}$=10V, I$_D$=3.5A, T$_J$=150℃	-	1.48	1.64	Ω
V$_{SD}$	Diode Forward Voltage	I$_S$=3.5A,V$_{GS}$=0V, T$_J$=25℃	-	0.82	-	V
I$_S$	Maximum Body-Diode Continuous Current		-	-	7	A
I$_{SM}$	Maximum Body-Diode Pulsed Current^C		-	-	30	A
DYNAMIC PARAMETERS						
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz	-	434	-	pF
C$_{oss}$	Output Capacitance		-	30	-	pF
C$_{o(er)}$	Effective output capacitance, energy related ^{H}	V$_{GS}$=0V, V$_{DS}$=0 to 480V, f=1MHz	-	23	-	pF
C$_{o(tr)}$	Effective output capacitance, time related ^{I}		-	80	-	pF
C$_{rss}$	Reverse Transfer Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz	-	1	-	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz	-	17.5	-	Ω
SWITCHING PARAMETERS						
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=480V, I$_D$=3.5A	-	9.2	-	nC
Q$_{gs}$	Gate Source Charge		-	2.5	-	nC
Q$_{gd}$	Gate Drain Charge		-	2.7	-	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=400V, I$_D$=3.5A, R$_G$=25Ω	-	21	-	ns
t$_r$	Turn-On Rise Time		-	14	-	ns
t$_{D(off)}$	Turn-Off DelayTime		-	55	-	ns
t$_f$	Turn-Off Fall Time		-	15	-	ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=3.5A,dI/dt=100A/µs,V$_{DS}$=400V	-	224	-	ns
I$_{rm}$	Peak Reverse Recovery Current	I$_F$=3.5A,dI/dt=100A/µs,V$_{DS}$=400V	-	19	-	A
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=3.5A,dI/dt=100A/µs,V$_{DS}$=400V	-	2.8	-	µC

A. The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25℃.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150℃, Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25℃.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.

G. L=60mH, I$_{AS}$=1.7A, V$_{DD}$=150V, Starting T$_J$=25℃

H. C$_{o(er)}$ is a fixed capacitance that gives the same stored energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

I. C$_{o(tr)}$ is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

J. Wavesoldering only allowed at leads.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL

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FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
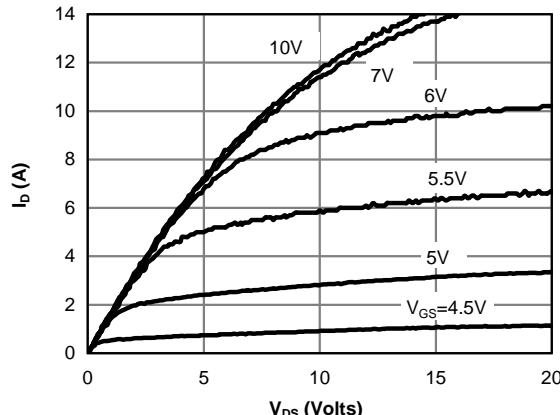

Figure 1: On-Region Characteristics @ 25℃
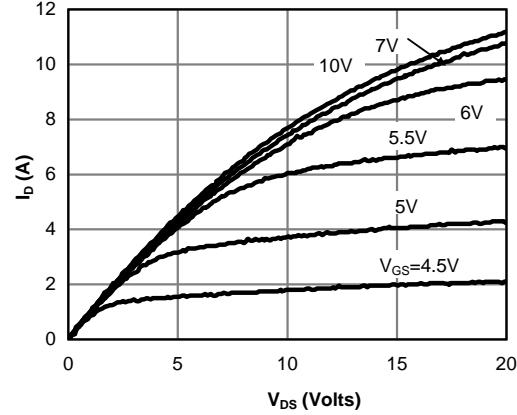
Figure 2: On-Region Characteristics @ 125℃
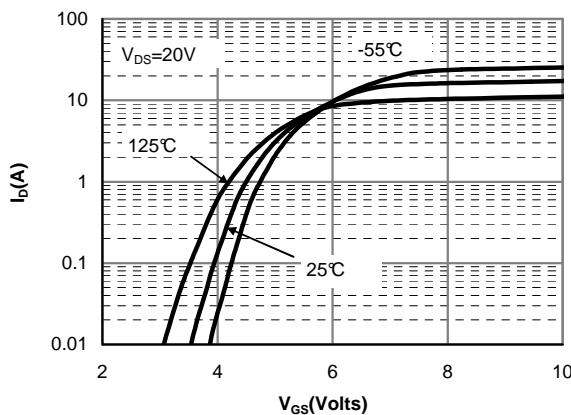
Figure 3: Transfer Characteristics
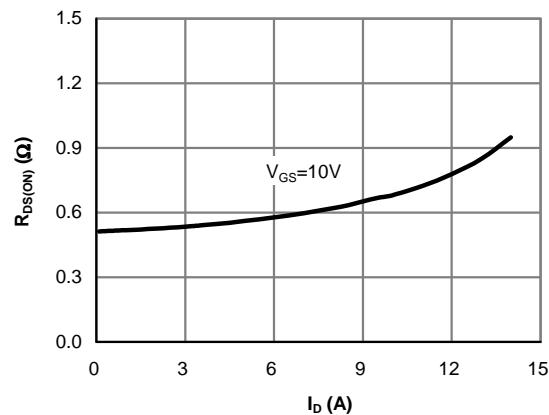

Figure 4: On-Resistance vs. Drain Current and Gate Voltage
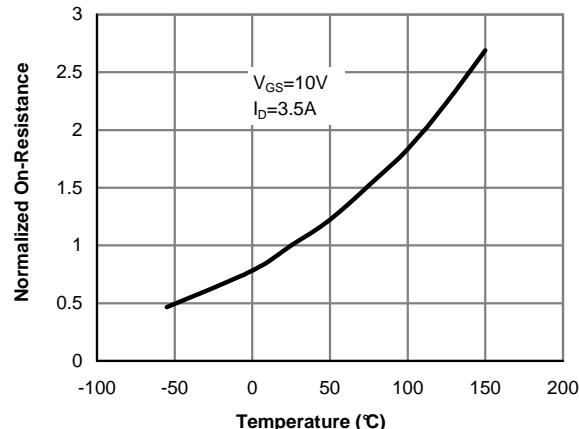

Figure 5: On-Resistance vs. Junction Temperature
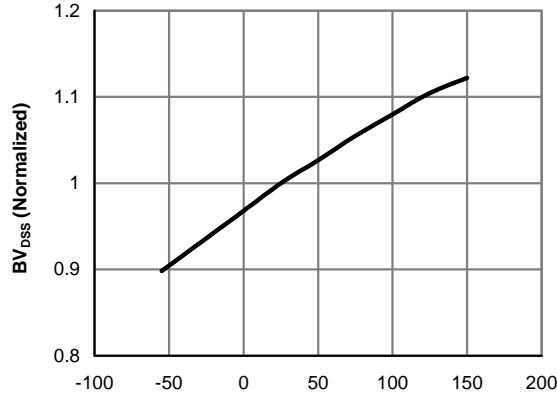
Figure 6: Break Down vs. Junction Temperature

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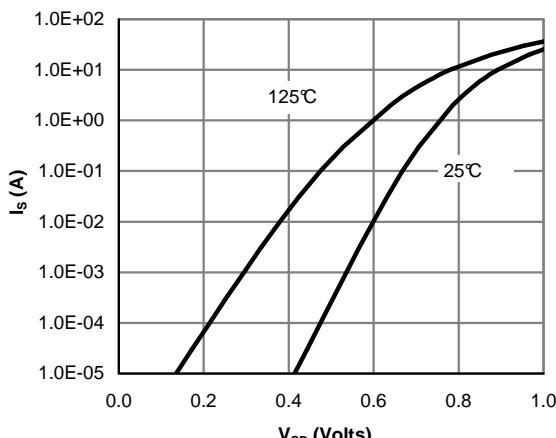
Figure 7: Body-Diode Characteristics (Note E)
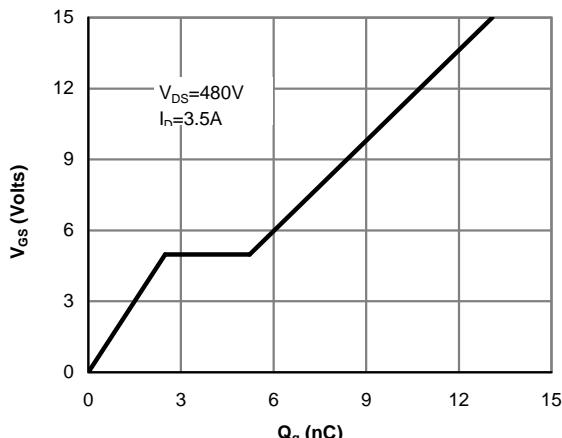
Figure 8: Gate-Charge Characteristics
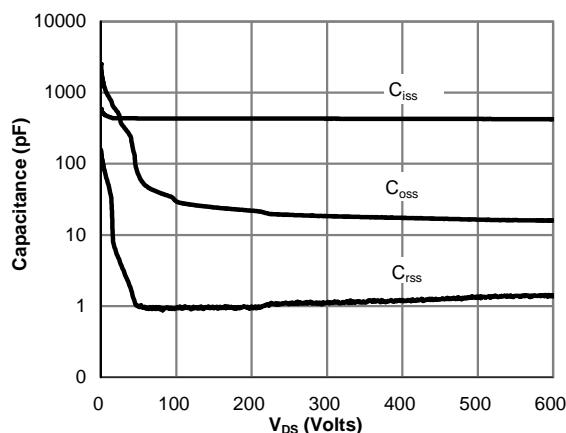
Figure 9: Capacitance Characteristics
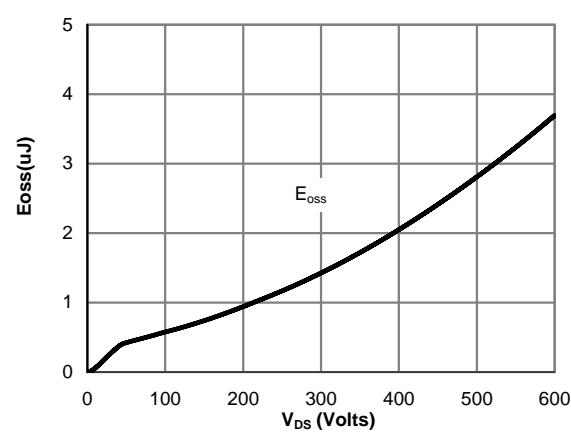
Figure 10: Coss stored Energy
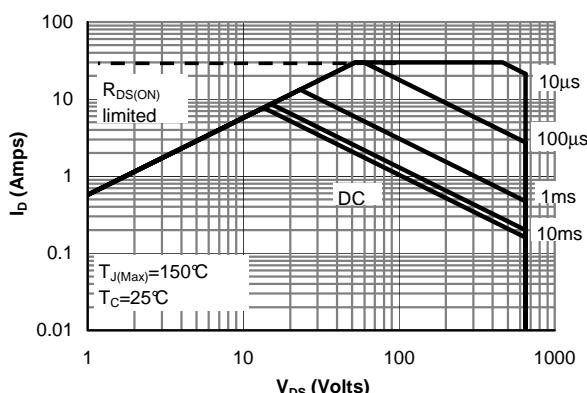
Figure 11: Maximum Forward Biased Safe Operating Area for AOW7S65 (Note F)
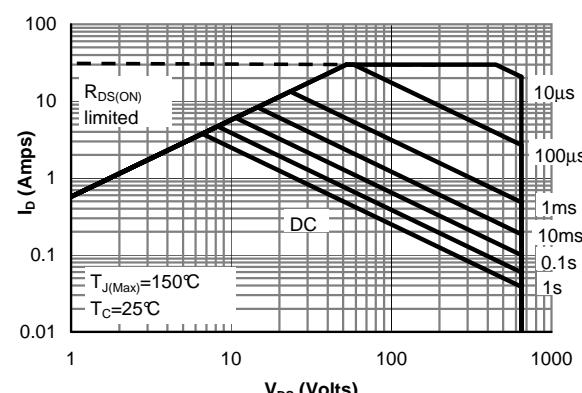
Figure 12: Maximum Forward Biased Safe Operating Area for AOWF7S65(Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
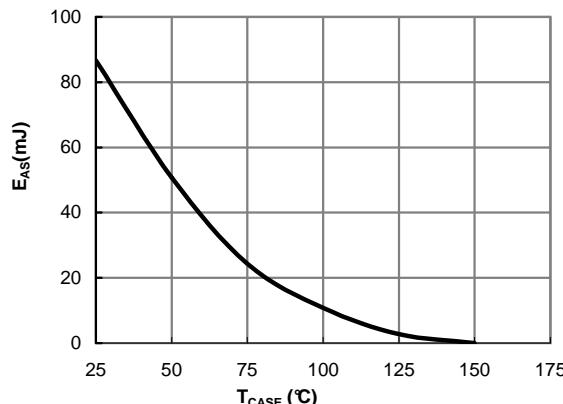
Figure 13: Avalanche energy
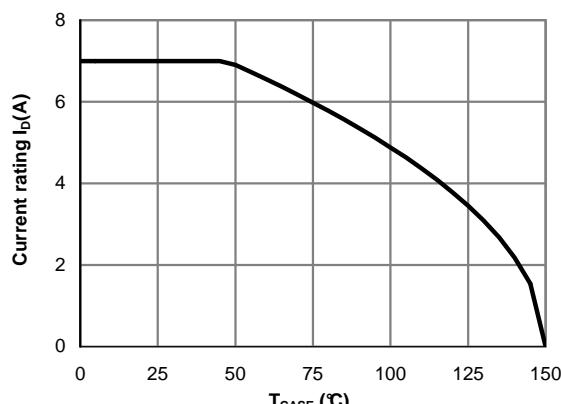
Figure 14: Current De-rating (Note B)

$D=T_{on}/T$
$T_{J,PK}=T_C+P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$
$R_{\theta JC}=1.2°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
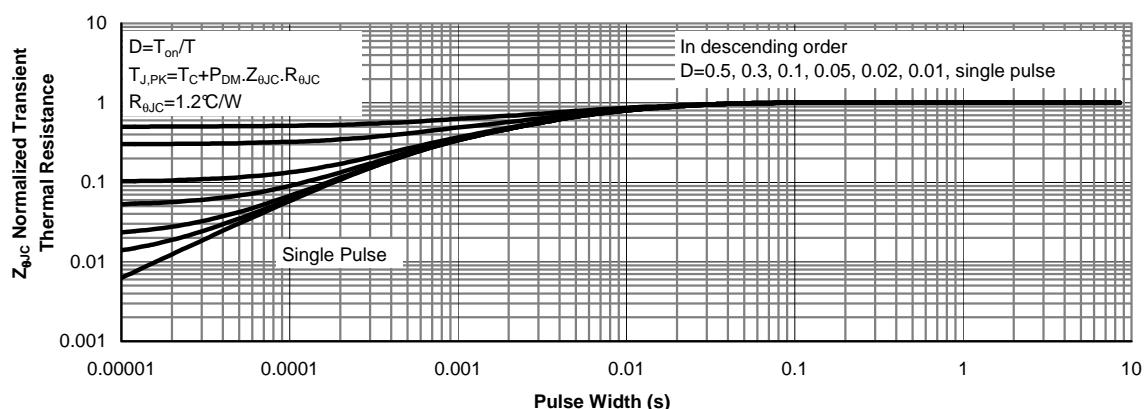
Figure 15: Normalized Maximum Transient Thermal Impedance for AOW7S65 (Note F)

$D=T_{on}/T$
$T_{J,PK}=T_C+P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$
$R_{\theta JC}=5°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
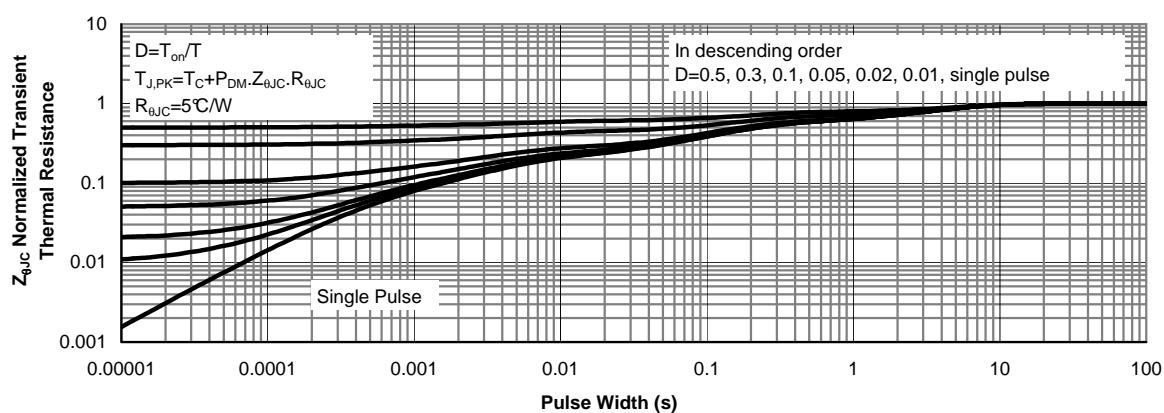
Figure 16: Normalized Maximum Transient Thermal Impedance for AOWF7S65 (Note F)

Gate Charge Test Circuit & Waveform
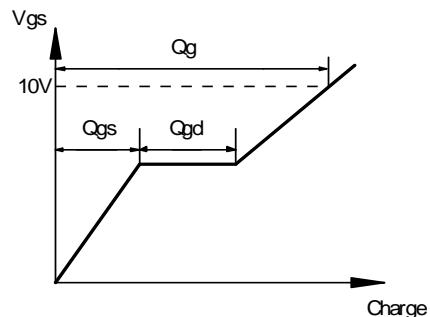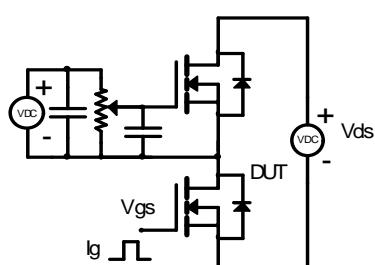
Resistive Switching Test Circuit & Waveforms
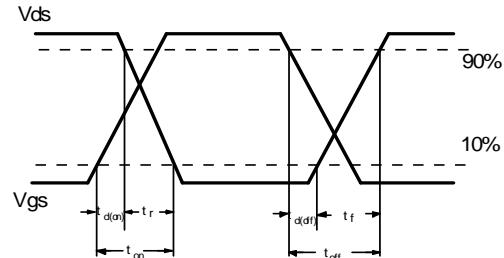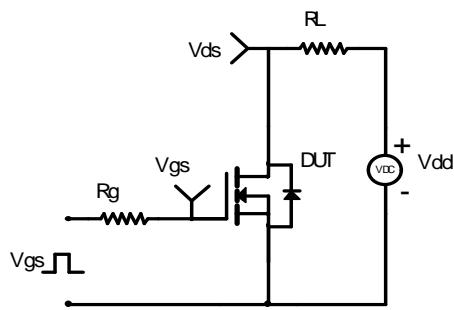
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \, LI_{AR}^2$$
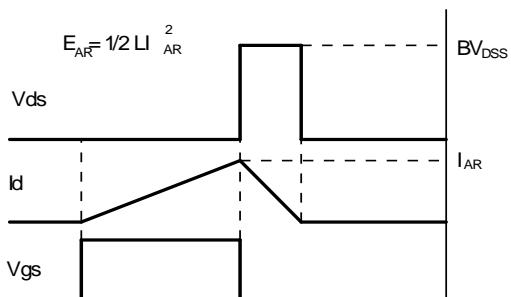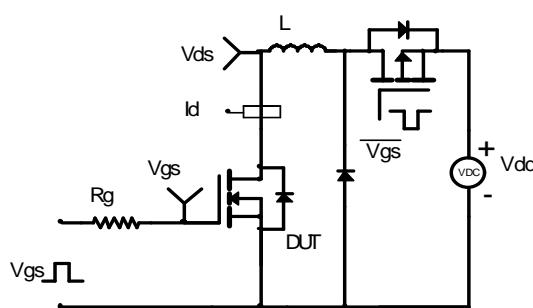
Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int I \, dt$$