



# ***AOS Semiconductor Reliability Report***

**HVMOS 650V/600V/550V/500V  
TO220/TO220F/TO262/TO262F, rev C**

**ALPHA & OMEGA Semiconductor, Inc**

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## **“Commitment to Excellence at Quality & Reliability!”**

To achieve this vision, AOS continuously strive for the excellence in design, manufacturing, reliability and proactively response to the customer’s feedback.

AOS ensures that all the product quality and reliability exceed the customer’s expectation by constantly assessing any potential risk, identifying cause of the suspected failures, driving corrective actions and developing prevention plan within the committed time through the continuously improvement.

This AOS product reliability report summarizes AOS Product Reliability result. The published product reliability data combines the results from new product Qualification Test Plan and routine Reliability Program activities. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. The released product will be categorized by the process family and be monitored on a quarterly basis for continuously improving the product quality. Table 1 lists the generic reliability qualification requirements and conditions:

**Table 1:AOS Generic Reliability Qualification Requirements**

<b>Test Item</b>	<b>Test Condition</b>	<b>Time Point</b>	<b>Sample size</b>	<b>Acc/Reject</b>
<b>HTGB</b>	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 hrs 1000 hrs	77 pcs / lot	0/1
<b>HTRB</b>	Temp = 150°C , Vds=80% of Vdsmax	168 / 500 hrs 1000 hrs	77 pcs / lot	0/1
<b>Solder reflow precondition</b>	168hr 85°C /85%RH + 3 cycle reflow @250°C  (MSL level 1)	-	The sum of PCT ,TC and HAST	0/1
<b>HAST</b>	130 +/- 2°C , 85%RH, 33.3 psi, Vgs = 80% of Vgs max	100 hrs	55 pcs / lot	0/1
<b>Pressure Pot</b>	121°C , 29.7psi, 100%RH	96 hrs	77 pcs / lot	0/1
<b>Temperature Cycle</b>	-65°C to 150°C, air to air,	250 / 500 cycles	77 pcs / lot	0/1
<b>Power Cycle</b>	$\Delta T_j = 125 \text{ }^\circ\text{C}$	4286 cycles	77 pcs / lot	0/1

## High Temperature Gate Bias (HTGB) & High Temperature Reverse Bias (HTRB)

HTGB burn-in stress is used to stress gate oxide at the elevated temperature environment hence any of the gate oxide integrity issue can be identified. HTRB burn-in stress is used to verify junction degradation under the maximum operation temperature.

Through HTGB & HTRB B/I stress test, the device lifetime in field operation & long term device level reliability can be determined. FIT rate is calculated by applying the Arrhenius equation with the activation energy of 0.7eV and 60% of upper confidence level at 55 deg C operating conditions.

## Solder reflow precondition (pre-con)

Solder reflow precondition is the test that simulates shipment and storage of package in under uncontrollable environment. Precondition is the pre-requirement for the mechanical related reliability tests (such as Temperature Cycle, Pressure Pot and High Acceleration Stress TEST (HAST). The routine of the test are: parts will be soaked in moisture then bake in pressure pot, or being placed into 85% RH, 85 deg C environment for 168 hrs. Then they will be run through a solder reflow oven with temperature at 260°C+/- 5°C. The test condition totally complies with MSL level 1. Pre-condition is a test that is detected package delamination, lifted bond wire issue.

## Temperature Cycling (TC)

Temperature cycling test is to evaluate the mechanical integrity of the package and the interaction between the die and the package. This is an air to air test at temperature range from -65°C/150°C and stress duration is from 250 cycles to 500 cycles.

## Pressure Pot (PCT)

PCT test is the test that measures the ability of the device withstand to moisture and contaminant environment. The test is done under enclosed chamber with the condition 121°C 15+/- 1PSIG, 100%RH and stress duration is 96 hrs.

## High Acceleration Stress Test (HAST)

High acceleration stress test is to stress the devices under high humidity, high pressure environment under DC bias condition. If ionic contamination involved, the corrosion from metal layer can be accelerated by the HAST stress condition.

## Power Cycle

The power cycle test is performed to determine that the ability of a device to withstand alternate exposures at high and low junction temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst case conditions encountered in typical application.

The following tables summarize the qualification results based on the device/process families and the package types, respectively.

## Summary of AOS High Voltage MOSFET product with TO220 /TO220F and TO262/TO262F package Qualification Results

**Table 2 Product Family**

Device No.	Package	Rdsmax ohms
AOW12N65	TO262	0.72
AOW10N65		1.00
AOWF12N65	TO262F	0.72
AOW12N60	TO262	0.55
AOW10N60		0.75
AOWF12N60	TO262F	0.55
AOWF10N60		0.75
AOTF12N60	TO-220F	0.55
AOTF10N60		0.75
AOTF8N60		0.9
AOTF7N60		1.2
AOTF4N60		2.2
AOTF2N60		4.4
AOT12N60	TO-220	0.55
AOT10N60		0.75
AOT8N60		0.9
AOT7N60		1.2
AOT5N60		1.8
AOT4N60		2.2
AOT3N60		3.5
AOT2N60		4.4
AOT1N60	8.8	
AOW12N50	TO262	0.52
AOW14N50		0.38
AOWF12N50	TO262F	0.52
AOWF14N50		0.38
AOTF14N50	TO-220F	0.34
AOTF12N50		0.52
AOTF8N50		0.85
AOTF5N50		1.5
AOTF3N50		3
AOT14N50	TO-220	0.38
AOT12N50		0.52
AOT8N50		0.85
AOT5N50		1.5
AOT3N50		3

**Table 3 Reliability Test and Package test Result:**

Test Item	Test Condition	Time Point	Total Sample size	Number of failure
<b>HTGB</b>	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 hrs 1000 hrs	2387	0
<b>HTRB</b>	Temp = 150°C , Vds=80% of Vdsmax	168 / 500 hrs 1000 hrs	2310	0
<b>Solder reflow precondition</b>	168hr 85°C /85%RH + 3 cycle reflow @250°C  (MSL level 1)	-	3839	0
<b>HAST</b>	130 +/- 2°C , 85%RH, 33.3 psi, Vgs = 80% of Vgs max	100 hrs	605	0
<b>Pressure Pot</b>	121°C , 29.7psi, 100%RH	96 hrs	1386	0
<b>Temperature Cycle</b>	-65°C to 150°C, air to air,	250 / 500 cycles	1848	0
<b>Power Cycle</b>	$\Delta T_j=125^\circ\text{C}$	4286 cycles	231	0
<b>Solder dunk</b>	260°C, 10secs	3 cycles	77	0

## Reliability Evaluation:

**FIT rate (per billion): 1.88**

**MTTF = 60832 years**

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the selected product. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

$$\text{Failure Rate (FIT)} = \text{Chi}^2 \times 10^9 / [2 (N) (H) (Af)] = 1.83 \times 10^9 / [2 (2541) (168) (258) + 2(1386)(500)(258)+2(770)(1000)(258)] = 1.88$$

$$\text{MTTF} = 10^9 / \text{FIT} = 5.338 \times 10^8 \text{hrs} = 60832 \text{ years}$$

**Chi<sup>2</sup>** = Chi Squared Distribution, determined by the number of failures and confidence interval

**N** = Total Number of units from HTRB and HTGB tests

**H** = Duration of HTRB/HTGB testing

**Af** = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)

Acceleration Factor [**Af**] = **Exp** [Ea / k (1/Tj u – 1/Tj s)]

### Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
<b>Af</b>	<b>258</b>	<b>87</b>	<b>32</b>	<b>13</b>	<b>5.64</b>	<b>2.59</b>	<b>1</b>

**Tj s** = Stressed junction temperature in degree (Kelvin), K = C+273.16

**Tj u** = The use junction temperature in degree (Kelvin), K = C+273.16

**k** = Boltzmann's constant, 8.617164 X 10<sup>-5</sup>eV / K