Power MOSFET Continuous Drain current rating and Bonding wire limitation

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Abstract

Power MOSFET datasheets will usually show maximum values for continuous drain current $I_{d,}$ on the first page of datasheets.

For bottom exposed part such as DPAK, TO220, D²PAK, there is always a note besides I_d rating saying that I_d is limited by bonding wires. Is this true? The answer is no for most of the cases.

The reason would be shown in this article and more studies will be present to show, how low the silicon resistance should be to lead to a bonding wire limitation issue.

Introduction

Power MOSFET maximum rating of I_d is base on one of the following limitation, whichever limitation reaches first:

1. Thermal resistance limitation for transistor die and thermal runaway.
2. Bonding wire limitation
   a. Wire fusion
   b. Thermal degradation of molding compound.

For packages with no bottom exposure, the heat sinking capability is limited from transistor die to PCB. I_d is usually limited by max junction temperature MOSFET can take. Because the usually low duty cycle real applications, to give a close to truth and meaningful current rating for power MOSFET, there is a convention in MOSFET business to rate the I_d the non-bottom exposure devices by 10s Max Junction to Ambient thermal resistance:

$$I_D = \sqrt{\frac{P_D}{R_{DS(on)\max} @ T_{J(\max)}}}$$

$$P_D = \frac{T_{J(\max)} - T_a}{R_{\Theta J(\max)}}$$

For package with bottom exposure, heat sinking to PCB or heat sink can be maximized by properly circuit and heat sink design. On datasheet for all these kind of MOSFET, Junction to Case thermal resistance will be used to calculate power dissipation P_D. By doing so bonding wire limitation has to be taking account.

Physics of I_d Limitations

A. Thermal Runaway

Power MOSFETs display increase of the on-resistance with temperature. Power dissipated in this resistance causes more heating of the junction, which further increases the junction temperature, in a positive feedback loop. (However, the increase of on-resistance with temperature helps balance current across multiple MOSFETs connected in parallel and current hogging does not occur). If the transistor produces more heat than the heat sink can dissipate, the thermal runaway happens and destroys the transistor. This problem can be alleviated to a degree by lowering the thermal resistance between the transistor die and the heatsink.

B. Bonding wire limitation theory

The fire impression of bonding wire limitation is wire fusing. The whole MOSFET business calculates bonding wire limitation base on the wire fusing theory. We'll discuss the validity of the implementation of this theory later.

The basic design equation for wire fuses is the Preece equation (W.H. Preece, Royal Soc. Proc., London, 36, p464, 1884) for wires in free air:

$$I = A \times D^{1.5}$$

Where A=10244 for cupper/gold, A=7585 for aluminum. D is the diameter of wire in inches. However, nowadays most chips are encapsulated in plastic and conduction through the molding compound usually slows the temperature increase in the wire significantly, the existing formulas limit the allowable DC current too much. In case of transient loading, heat is also stored as internal energy in the molding compound. As a result, the wire will not become as warm as predicted by known formulas. In free air, wire current limited by melting temperature. In usual molding compounds decomposition occurs if temperature exceeds about 220 C. This temperature limit restricts the permissible current.

People modified the constant A for bonding wire limitation:

$$I = A \times D^{1.5}$$

- D = wire diameter in inches
- I = DC or rms current.

For bonding wires in plastic packages.

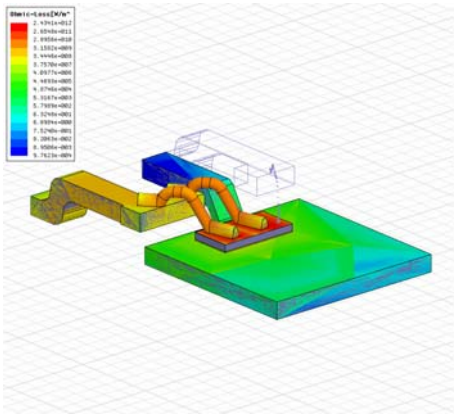
- A = 30000 for Gold or Copper with a bond-to-bond length <= 0.040 in. (0.1cm)
- A = 20500 for Gold or Copper with a bond-to-bond length >0.040 in. (0.1cm).
- A = 22000 for Aluminum with a bond-to-bond length <= 0.040 in. (0.1cm)
- A = 15200 for Aluminum with a bond-to-bond length >0.040 in. (0.1cm).

From this equation, we can derive the wire bonding limitation table we are using for datasheet:

Merterial	D(mils)	I (A) <1mm	I (A) >1mm
Cu/Au	1	0.9	0.6
Cu/Au	1.3	1.4	1.0
Cu/Au	1.5	1.7	1.2
Cu/Au	2	2.7	1.8
Al	1	0.7	0.5
Al	1.25	1.0	0.7
Al	1.5	1.3	0.9
Al	2	2.0	1.4
Al	3	3.6	2.5
Al	4	5.6	3.8
Al	5	7.8	5.4
Al	8	16	11
Al	10	22	15
Al	12	29	20
Al	15	40	28
Al	18	53	37
Al	20	62	43

Table 1: Bonding wire limitation for different wire materials and wire diameters, based on Modified Peece equation.

By doing simple calculation, it's easy to find out most bottom exposed MOSFETs are bonding wire limited. Is this true? To answer this question we run the electrical and thermal simulation for one of our D-PAK MOSFET AOD452 ($R_{ds(on)}$=6.5mohm, V_{gs}=10V) with 2 x 12mils wire bonded on Source. Wire resistance is around 0.6mohm.



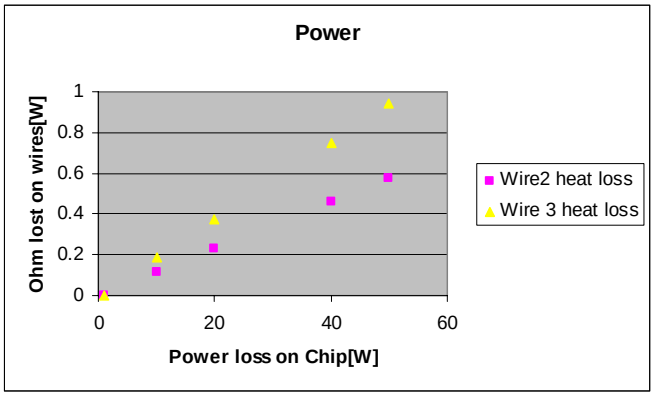


Figure 1: AOD452 (D-PAK) electrical simulation. Ohm loss in wire and transistor die are calculated

Based on the result of electrical simulation in Fig 1, the thermal simulation results are followed. Two different cases are simulated.

Case 1: datasheet case→ Junction to case thermal is used to for datasheet I_d rating, in which case the MOSFET is mounted on a big enough (ideal) heat sink so that the temperature rise for heat sink is negligible, Fig 2.

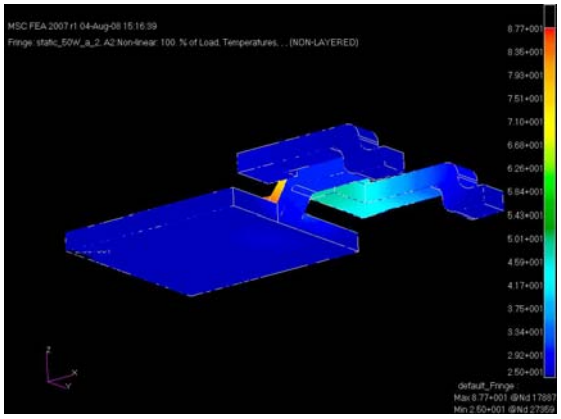


Figure 2: AOD452 (D-PAK) thermal simulation- Case 1_bottom view

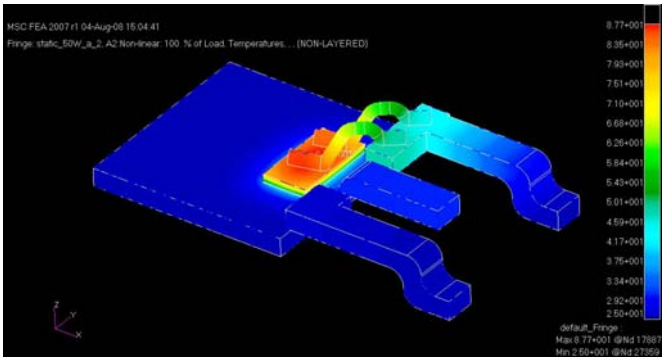


Figure 3: AOD452 (D-PAK) thermal simulation- Case 1_top view

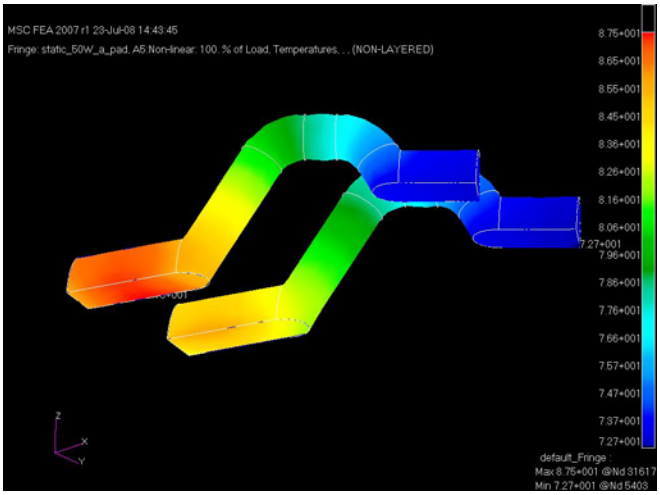


Figure 4: AOD452 (D-PAK) thermal simulation- Case 1_wire view

Heat distribution for this case is shown in Fig. 3 and Fig. 4. Because $R_{ds(on)}$ of MOSFET is more than 10 times wire resistance, more than 90% of total heat is generated by the die, even though the die attached to lead frame whose back side have ideal convection for heat releasing, the die surface, where wire bond landed, has the highest current density, therefore, is the hottest spot. These results are linear, which means T_{jmax} will always be firstly achieved before the bonding wire would ever reach 220 °C, namely, never there is a bonding wire limitation issue.

A question may be raised that the wire temperature is low because it heat sink through source lead which also has ideal convection at the end. To answer this question we did another simulation (Case 2.) with all other conditions the same and remove ideal convection from source lead. The result is in Fig. 4 and Fig. 5. The hottest spot is still on the surface of the die. The only different is now almost all heat convection thru bottom exposure. Temperature gradient on source lead changed and absolute value on the die increased a little.

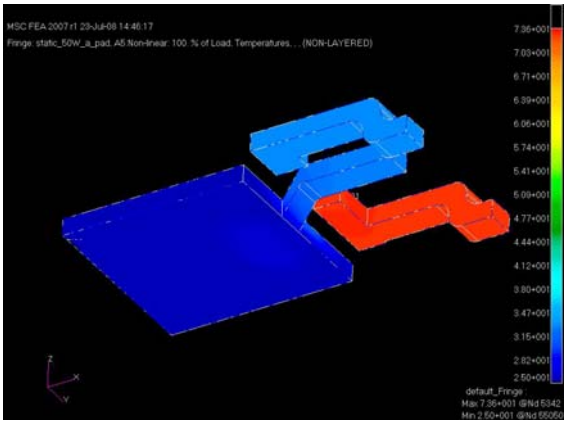


Figure 5: AOD452 (D-PAK) thermal simulation- Case 2_bottom view

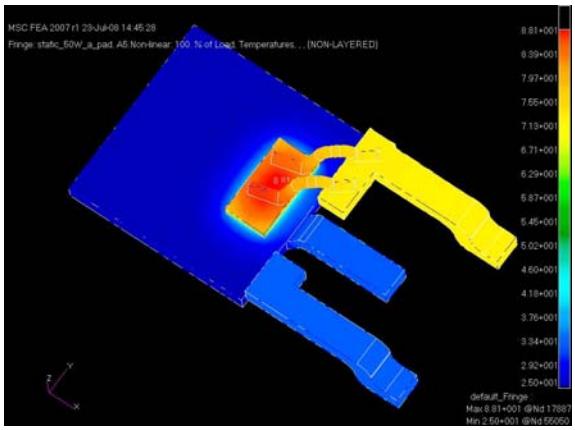


Figure 6: AOD452 (D-PAK) thermal simulation- Case 2_top view

So far we know for the thermal condition we use on datasheet, which is use junction to case thermal to calculate maximum continuous drain current, there would be no bonding wire limitation issue. Datasheet condition is an ideal condition which gives us the maximum I_d the MOSFET can get. In reality the MOSFET usually soldered on a finite size PCB with limited convection for heat releasing. Therefore we simulated the third case with MOSFET mounted on a 1 in^2 1 oz. PCB in still air. All other conditions are the same. The results are shown in Fig.7 and Fig.8. Now the temperature gradient on lead frame appears and absolute temperature values are much higher due to finite convection. But the hottest spot is still on the surface of the die. Our previous conclusion still stands.

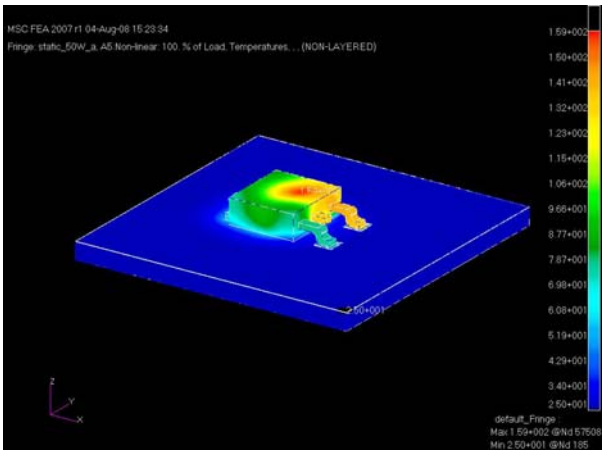


Figure 7: AOD452 (D-PAK) thermal simulation- Case 3_top view with molding compound

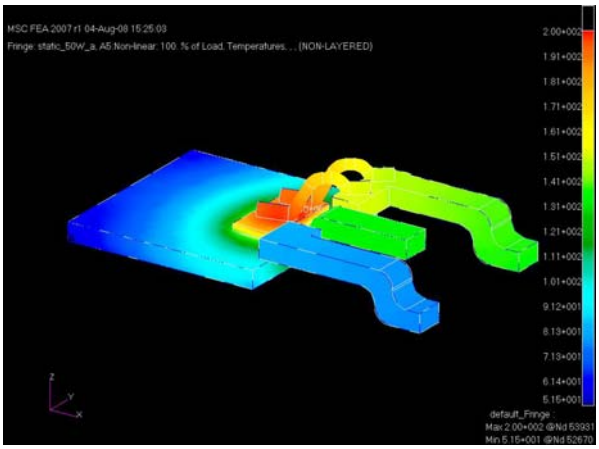


Figure 6: AOD452 (D-PAK) thermal simulation- Case 3_top view

From the 3 cases we have seen above, there obviously no bonding wire limitation for I_d (continuous drain current) setting for this device. This leads to another question people might ask: does bonding wire limitation apply to any MOSFET at all? This particular MOSFET you are investigating is 6.5mohm $R_{ds(on)}$ with only 0.6mohm wire resistance. There is MOSFET on the market with as low as 0.9mohm $R_{ds(on)}$. Does lower $R_{ds(on)}$ leads to Bonding wire limitation issue for I_d?

To answer this question, another simulation has been set up to study: how low the silicon resistance is needed to shift the hottest spot from die surface to bond wire.

Figure 7a/b shows that by lowering the silicon resistance to 10% of real resistance (0.65mohm). The hottest spot shift to bonding wire, which means bonding wire may have a chance reach its maximum temperature limit 220°C before the die reaches its max temperature 175°C.

Figure 7a/b shows that by lowering the silicon resistance to 20% of real resistance (1.3mohm). The hottest spot shift back to the silicon surface.

Figure 7 and Figure 8 tell us, to shift the hottest spot from silicon to wire, you need a silicon resistance around <1mohm. Please keep in mind the wire I am using are 2x12mil (0.6mohm) Al wires. If someone want to package a <1mohm silicon, the wires or even clip or ribbon boding they are using should have much less resistivity. Low resistivity bonding would shift the hot spot to Silicon surface again.

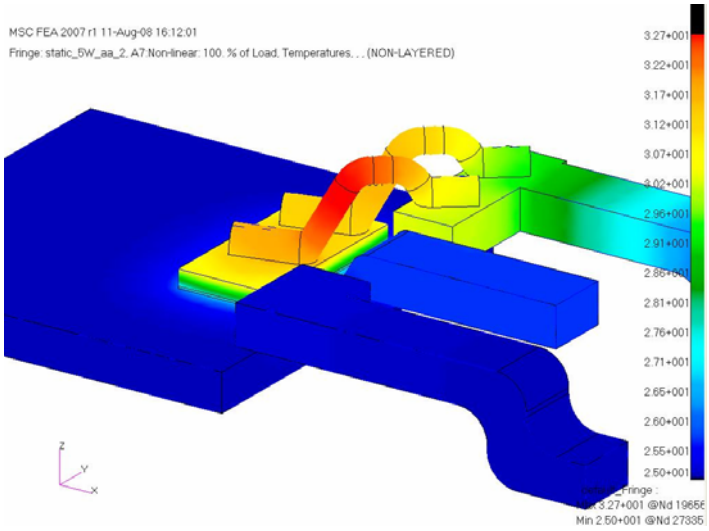


Figure 7a: AOD452 (D-PAK) (with 10% silicon resistance) thermal simulation_top view

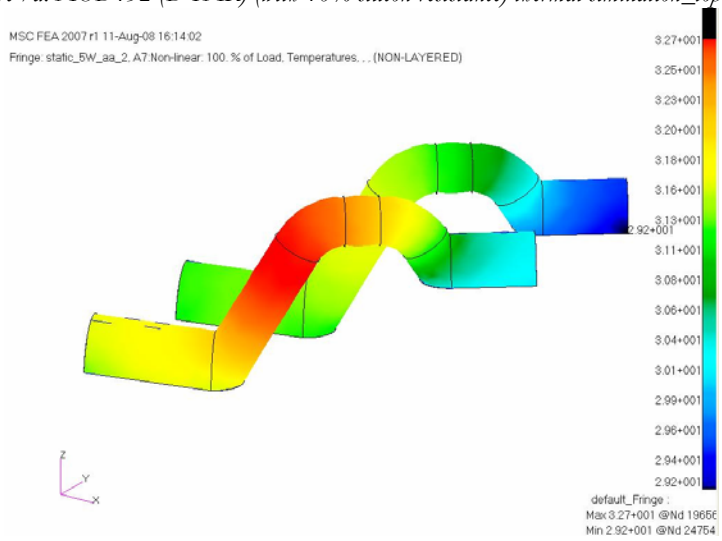


Figure 7b: AOD452 (D-PAK) (with 10% silicon resistance) thermal simulation_wire view

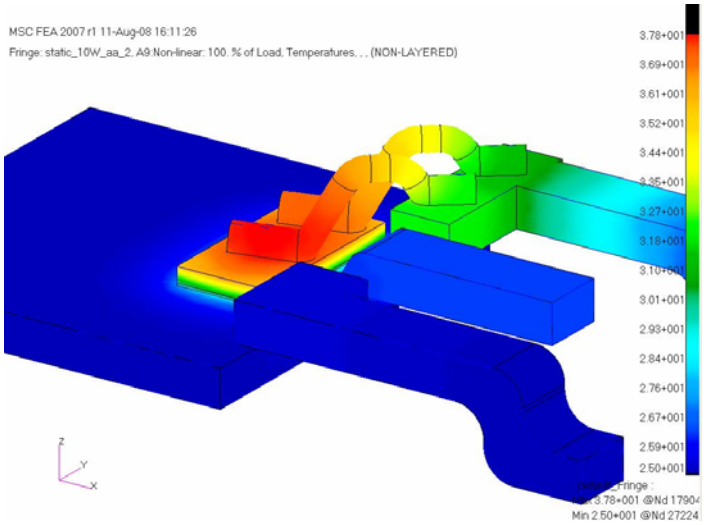


Figure 8a: AOD452 (D-PAK) (with 20% silicon resistance) thermal simulation _ top view

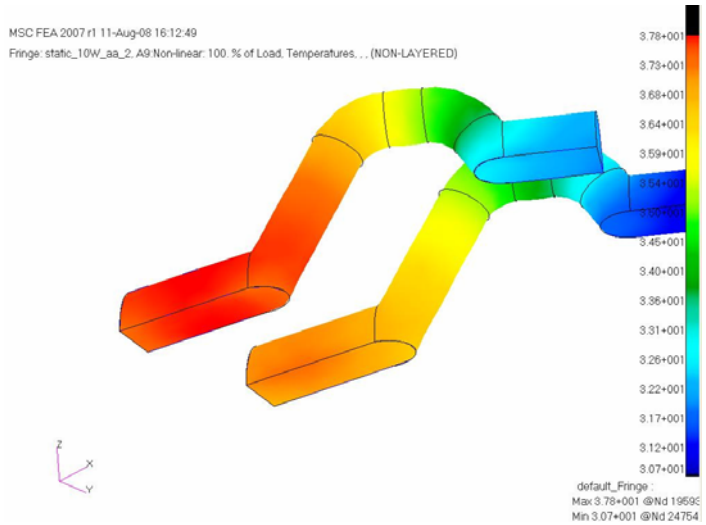


Figure 8b: AOD452 (D-PAK) (with 20% silicon resistance) thermal simulation _ wire view

Summery

MOSFET bonding wire limitation calculated based on wire fusing temperature in free air is a misunderstanding of thermal conduction inside MOSFET package. There would not be an issue of bonding or package thermal limitation unless the silicon resistivity is comparable to bonding resistivity.

Revision History

Date	Revision	Changes
5/21/2009	1	Initial release

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