Paralleling Power MOSFETs in Switching Applications

Abstract: This paper discusses issues involved in paralleling MOSFETs in high-power, high-frequency switching applications. It investigates root cause problems such as unbalanced voltage and current by taking a closer examination of PCB layouts and important circuit design parameters for driving paralleled MOSFETs.

1. Introduction

MOSFETs with low on-resistance and fast switching characteristics are widely used in switch-mode power supplies and motor drivers in e-bikes, electric-motor cars, power tools and electric lawn mowers. In these high power applications, multiple MOSFETs used in parallel are often necessary to increase current capability and improve efficiency.

Multiple factors influence successful paralleling of high-speed power MOSFETs. Variance in the actual device parameters, asymmetric gate drivers, and poor layout of the PCB can cause a number of problems. First, unbalanced current flow in parallel MOSFETs can provoke over-current conditions and damage one or more MOSFETs. Second, the drain-to-source voltage applied to each MOSFET can actually be different, potentially reaching damaging levels on the drain of one of the devices. Finally, parasitic oscillations can appear at the gate of each MOSFET, causing excessive gate-to-source voltage, potentially damaging one or more of the MOSFETs by exceeding its maximum rated V_{GS}. This application note conducts a detailed study of each of these issues and provides recommended solutions.

2. Unbalanced Current and Voltage- in Parallel MOSFET Applications

Under steady-state conditions, paralleled MOSFETs work well, sharing current with an equal amount of voltage across each. The on-resistance ($R_{DS(on)}$) of a MOSFET has a positive temperature coefficient, meaning that $R_{DS(on)}$ increases with temperature. This known phenomenon assists in paralleling MOSFETs as it helps balance the current among multiple MOSFETs. Current flows through the path of least resistance and as current increases in one MOSFET, power dissipation also increases, heating the device and increasing the $R_{DS(on)}$. At that point, current will flow to one of the other MOSFETs with a lower resistance, causing the inherent current sharing amongst the MOSFETs.

Under switching conditions, the story is very different. Generally speaking, a MOSFET behaves like a voltage-controlled switch. During the dynamic process of switching, many factors can cause current and voltage imbalances, especially at higher frequencies. The characteristics of the MOSFET, including the gate threshold voltage, its forward transconductance, total gate charge (Q_g), $R_{DS(on)}$, the actual driver circuit and parasitic inductances in the PCB all factor in to current and voltage imbalances. The MOSFET parameters are fixed at the time of device production and cannot be changed in the application, and screening MOSFETs to get exactly matched parameters can be economically challenging. The best way to prevent these problems is to use proper gate driver design techniques that ensure that the current and voltage across the paralleled MOSFETs are properly balanced.

2.1. Current Unbalance Resulting From MOSFET Parameters

Understanding MOSFET parameters and how they affect current and voltage balancing in paralleled MOSFET applications is an important first step to determining the right solution to the problems that may arise.

Threshold Voltage, Gate-to-Sourec ($V_{GS(TH)}$): Paralleled MOSFETs are normally driven by the same gate driver or gate driver signal. A MOSFET with a lower gate-to-source threshold voltage ($V_{GS(TH)}$) will turn on faster than a second MOSFET with a slightly higher $V_{GS(TH)}$. This results in higher current flowing through the MOSFET with the lower $V_{GS(TH)}$ and an unbalanced current situation.

Forward Transconductance (g_{FS}): In the saturation region between the cut-off region where the MOSFET turns off and the Ohmic region where the MOSFET is fully on, the drain current is controlled by the gate-to-source voltage, V_{GS}. This region is governed by the forward transconductance (g_{FS}) characteristics of the device. Different gate-to-source voltages will cause current imbalances during the transition from on to off and vice-versa.

Gate Charge (Q_g): Total gate charge, the total charge required at the gate to turn-on the MOSFET and enable current flow from drain-to-source, will significantly affect the switching speed of the MOSFET. When multiple MOSFETs are paralleled, if one of the MOSFETs has a lower Q_g value, it will turn on faster than the rest of the MOSFETs. This faster turn on causes that MOSFET to handle the majority of the current during the transition, causing another unbalanced current condition.

2.2. The Effect of the Gate Driver Resistance on Current Imbalance

In the gate driver circuit shown in figure 1, an intentional mismatch has been created and tested to show the impact of mismatched gate resistances. As will be shown in section 3, the use of gate resistors is recommended in high-frequency applications to avoid additional complications, and it is critical to ensure that these gate resistors are matched as closely as possible. In the gate driver circuit shown in figure 1, Q1 and Q2 are paralleled. R1 is the driving resistor connected in series with the gate of Q1. R3 is connected to R1 and the gate of Q2. This creates the gate driver mismatch.

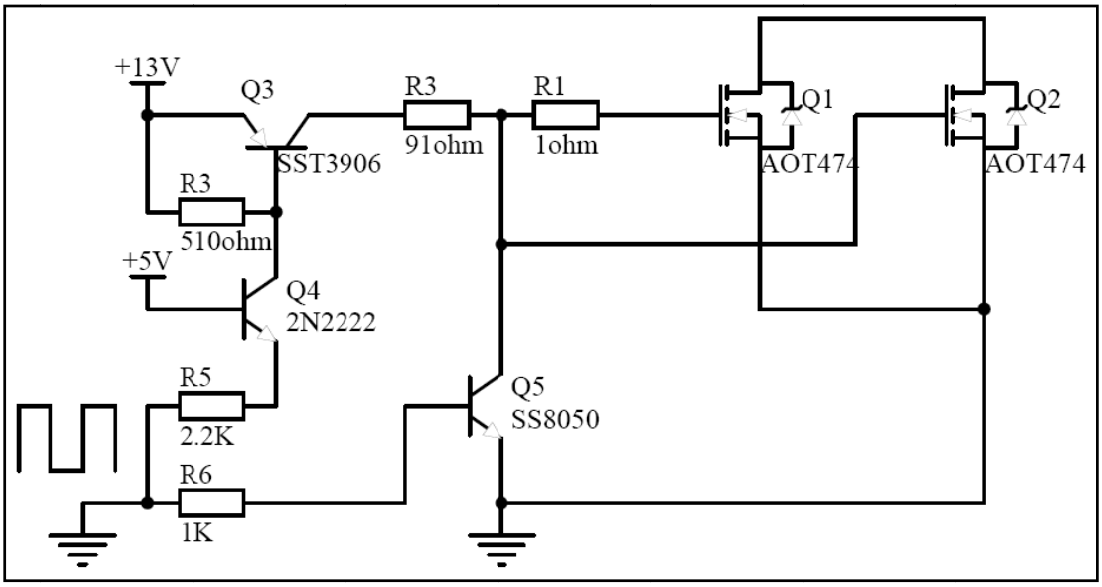

Figure 1. Driving Circuit with the Gate Resistor Mismatch

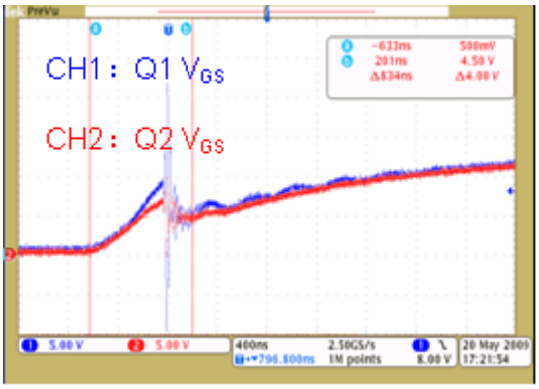

Figure 2a. Turn-On Waveforms

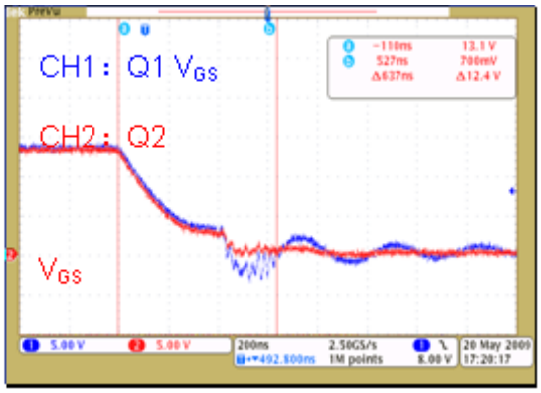

Figure 2b. Turn-Off Waveforms

Figures 2a and 2b show the gate-to-source voltages during turn-on and turn-off that result from the gate driving resistor mismatch. Channel 1 shows the faster turn-on and turn-off times of Q1, the result of the slightly lower gate resistance. These faster switching times provoke higher current flow through Q1, compared to the current flow through Q2. The higher current flow through the parasitic inductance in the drain and source of Q1 causes larger voltage peaks and ringing. The difference between Q1 and Q2 in figures 2a and 2b shows that Q1 is handling larger peak currents during the transitions due to the mismatched gate driver resistors. It is important to balance current through each MOSFET during transitions to avoid excessive stress on one of the MOSFETs in a paralleled application, and using matching gate resistance is the key to achieving the desired performance.

2.3. The Effect of the Gate Driver Circuit Layout on Voltage Unbalance

In high-power, high-frequency applications, the parasitic inductance of the PCB can negatively impact the overall system. Excessive stray inductance in the drain may cause the MOSFET to fail if they are not well controlled.

Figure 3 shows parasitic inductance in two paralleled MOSFETs, intentionally skewed to simulate a poor layout. In this circuit, the drain inductance of Q1 is 40nH (L1) and the inductance of Q2 is 20nH (L2). AOT470 is a 75V MOSFET that was chosen for this simulation.

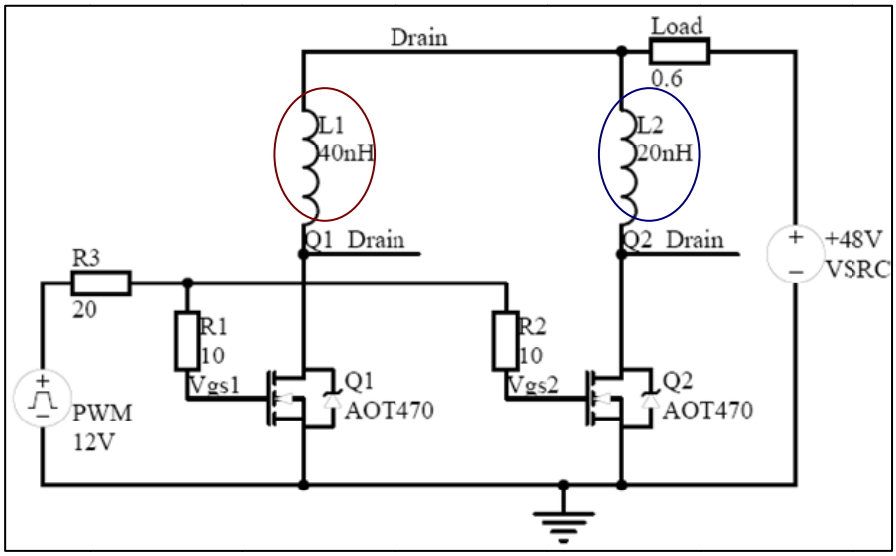

Figure 3. A Simulating Circuit with Different Drain Inductance

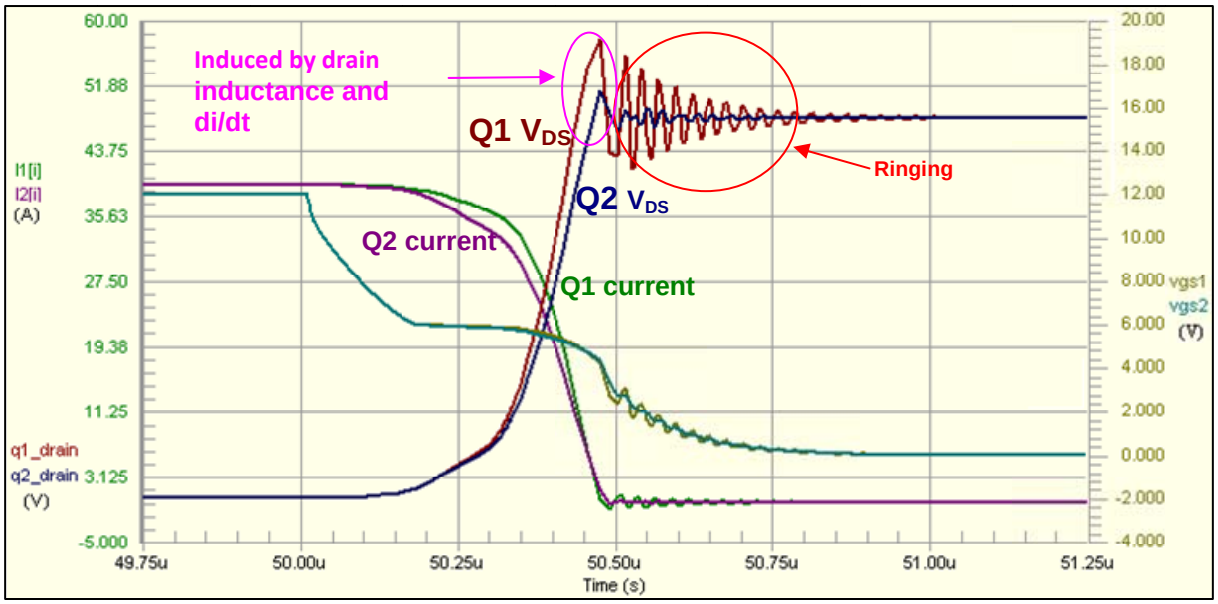

Figure 4. Simulation Waveforms with Different Drain Inductances

During turn-off a voltage will be added to the maximum drain voltage as determined by the parasitic inductance and the changing current (V = L* di/dt). If the matching circuits consist of the same di/dt characteristic and the parasitic inductance is optimized for each MOSFET, the max drain voltage seen by each device will be approximately the same.

When the parasitic inductances in the drains are different, the two excessive voltages caused by the V = L * di/dt term will be unequal. This difference, in turn, influences the magnitude of the di/dt and eventually will result in a higher drain voltage on Q1. Additionally, since the drain inductance of Q1 is larger, its ringing amplitude (as shown in figure 4) is also larger when L1 rings with the Coss of the AOT470 and the parasitic resistance in the circuit. This combination of ringing and the voltage spike on the drain during turn-off can easily make the MOSFET exceed its maximum rated drain-to-source voltage and cause failure. By carefully designing the gate driver circuit as shown in section 2.2, and minimizing parasitic circuit inductance during PCB layout, the circuit designer can avoid these mismatches.

3. Managing Potential Oscillations in Paralleled MOSFET Applications

Many designers tend to directly connect both gates and both drains together when paralleling two MOSFETs. However, this approach can easily cause an oscillation on the gate. Worst case, the oscillation amplitude can even surpass the maximum rated gate voltage and wind up damaging the MOSFET.

3.1. Examples of Oscillation

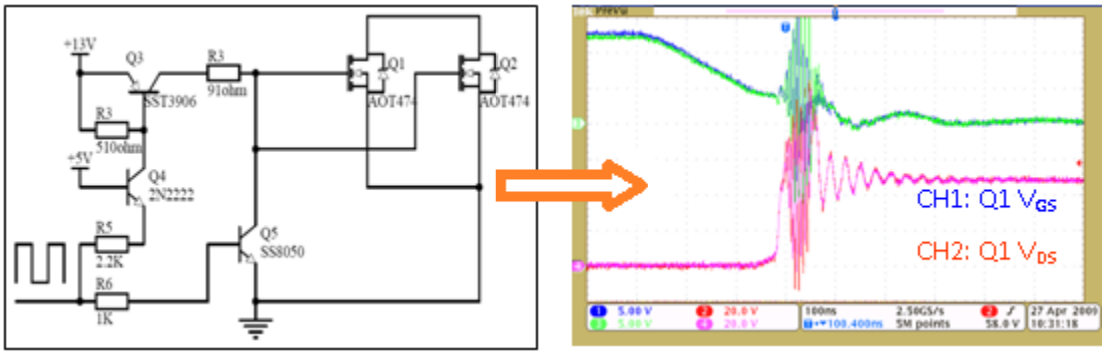

Figure 5. Turn-Off Waveforms of Two MOSFETs Directly Paralleled

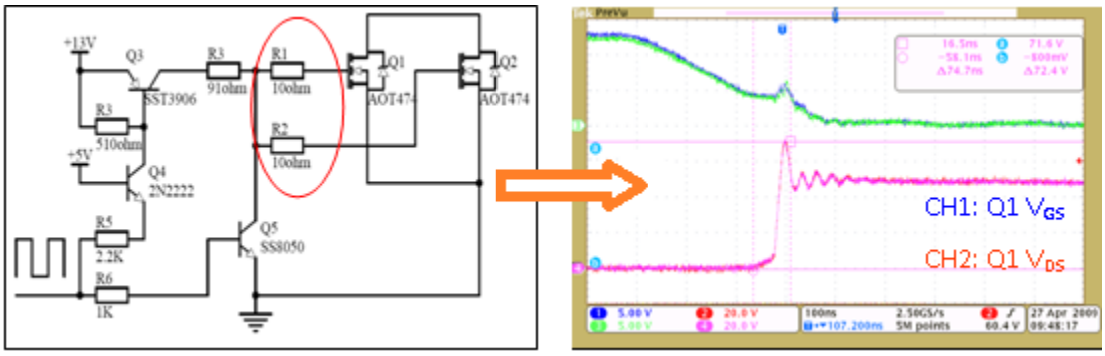

Figure 6. Turn-Off Waveforms of Two MOSFETs Paralleled with Separate Driving Resistors

Figure 5 shows a clear example of an oscillation that can occur when the two gates are directly connected together. The high frequency oscillation of ~150MHz occurs during the turn-on and turn-off transitions. These oscillations often have very high amplitudes and can easily exceed the maximum rating of gate-to-source voltage or drain-to-source voltage and damage the device.

Through the use of individual gate driving resistors, the oscillation can easily be removed. Figure 6 shows the result of adding a single resistor in the gate of each MOSFET. Both gate and drain voltages are virtually identical on the two MOSFETs, meaning that the current through each device can be assumed to be the same when paralleled. This greatly improves the reliability of the circuit.

3.2. Root Cause Analysis of Gate Oscillation

To understand the cause of the high frequency oscillation at the gate of two MOSFETs that are directly connected together, it is important to analyze the equivalent circuit. Figure 7 shows the two paralleled MOSFETs with the parasitic drain inductances, gate capacitances (Cgd), and gate resistances all detailed. These components form a low-impedance loop and can be considered as a series RLC equivalent circuit.

Resonant frequency of a series RLC circuit ：

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \qquad (1)$$

Quality factor of a series RLC circuit：

$$Q = \frac{\omega_0 L}{R} = \frac{1}{R\omega_0 C} \qquad (2)$$

Equations 1 and 2 determine the resonant frequency of the series equivalent circuit and the quality factor (Q) at that resonant frequency. The lower impedance the circuit has, the higher the resulting Q factor. The more selective a circuit behaves in responding to signals of a given frequency, the higher the resulting oscillation amplitude. In order to avoid this oscillation, equal gate resistors are recommended in series with each gate, which will help to suppress the oscillation when the loop impedance is very low.

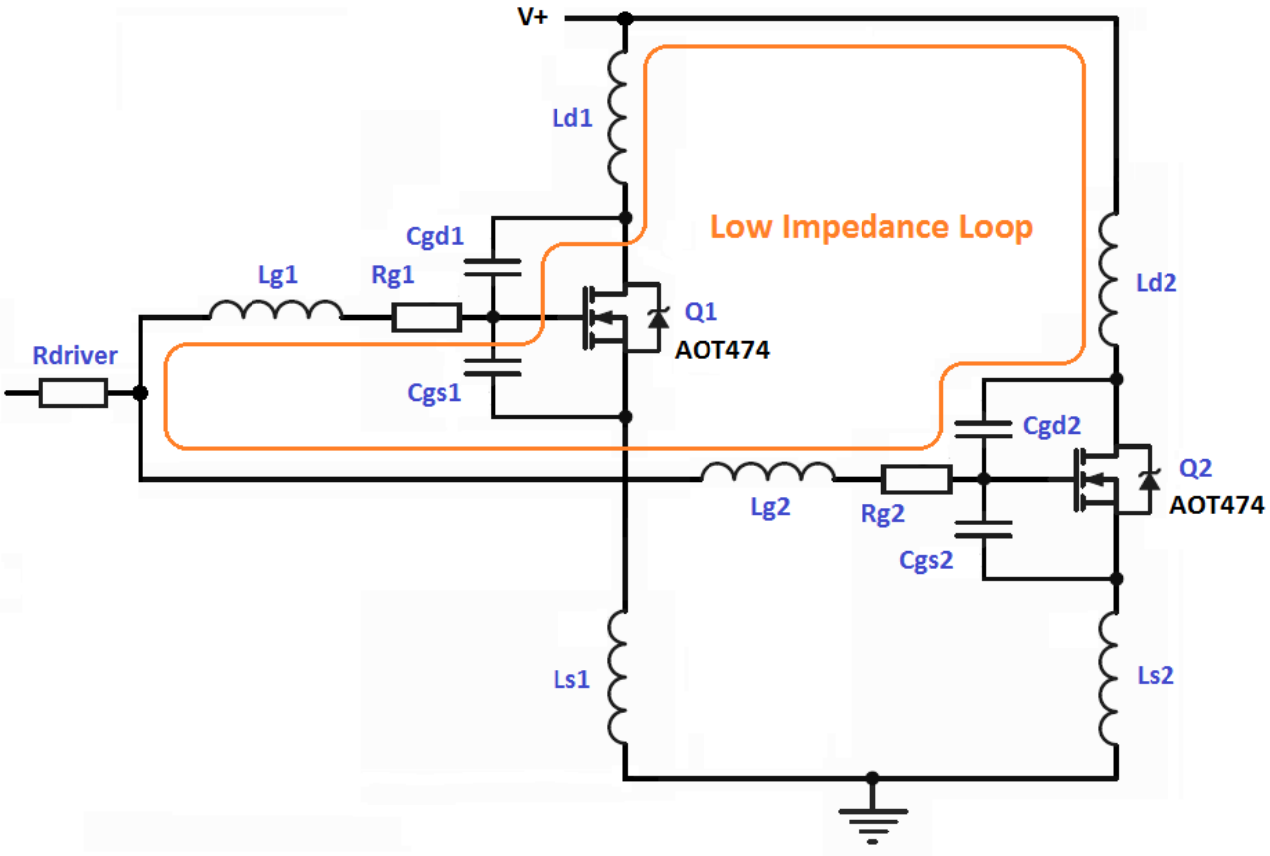

Figure 7. Model of Paralleling of MOSFETs

When two AOT474 power MOSFETs are paralleled, the oscillation that results is due to the reduced C_{gd} value, which in turn increases the Q factor (Q is inversely proportional to C_{gd}). The solution is to connect a separate gate resistor of 10Ω to the gate of each MOSFET to reduce the Q factor and suppress the oscillation on the gates, as shown in figure 6.

The circuit simulation in figures 8a, 8b and 9 further demonstrates why series gate resistances are important to suppressing oscillations. The parameters used in this model were obtained from the electrical specification of the AOT474 datasheet. The device's internal R_g is 2.8Ω and the C_{gd} is 36pF. Assuming the parasitic inductance of 60nH in the loop, the new equivalent circuit and the values of the equivalent impedances are show in figure 8a. Figure 8b shows the impact of adding a 10Ω series gate resistor each MOSFET, increasing the effective gate resistance from 5.6Ω to 25.6Ω.

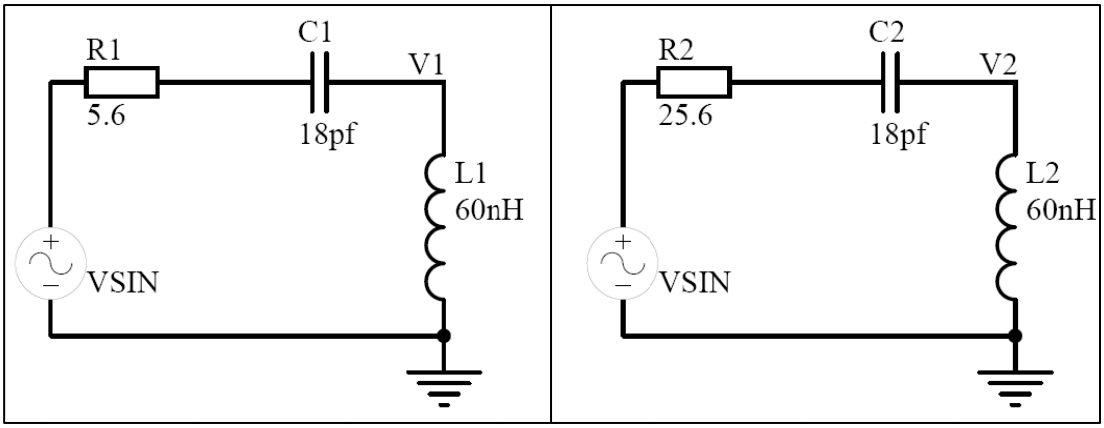

Figure 8a. RLC Circuit Model with Internal Rg

Figure 8b. RLC Circuit Model with a 10Ohm Resistor in Series with the Gate

Small-signal analysis performed using the parameters obtained from the AOT474 datasheet and the equivalent circuit models shown in figures 8a and 8b yielded the results shown in figure 9. The red curve obtained by simulating the circuit in figure 8a shows the approximately 150MHz resonant frequency at high Q, which corresponds nicely to the waveform shown in figure 5. The blue curve is the simulation result for the equivalent circuit in figure 8b, showing the impact of adding a 10Ω gate resistor to each MOSFET gate. The Q factor of the circuit is significantly reduced, explaining the result shown in figure 6 of a very clean gate drive waveform.

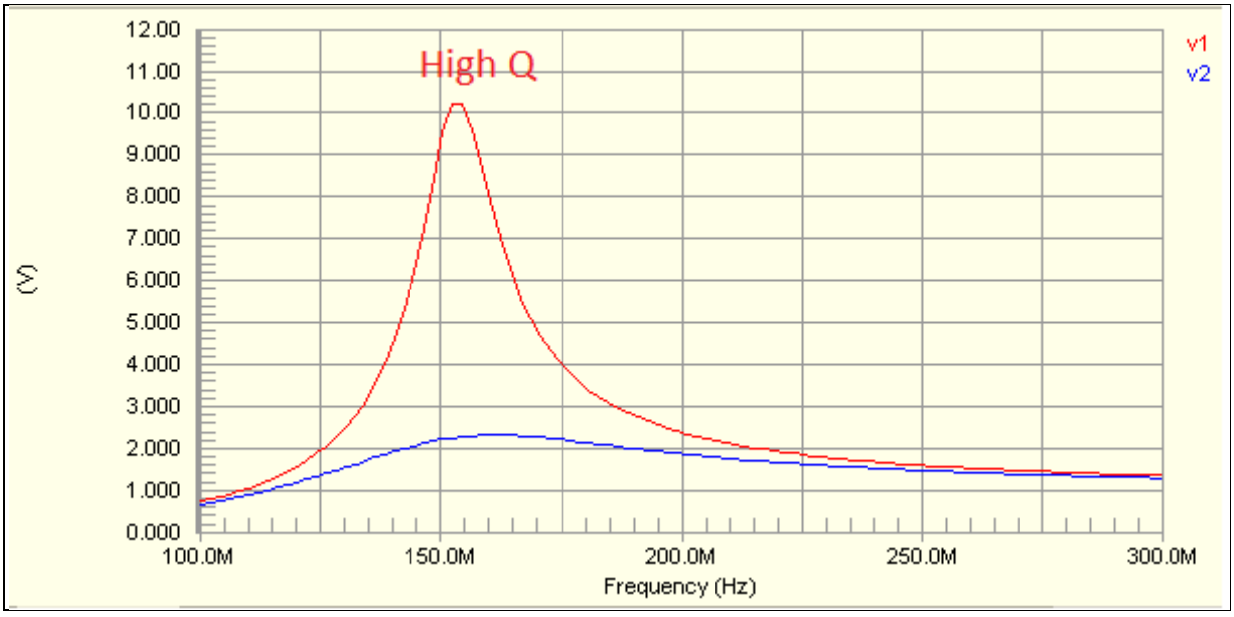

Figure 9. Simulation Waveforms of a Series RLC Circuit

4. Conclusion

For optimal current sharing and voltage balance when using paralleled MOSFETs in switching applications, care must be taken while designing the circuit. Dedicated gate resistors for each MOSFET will help match turn-on and turn-off times while removing the possibility for high-frequency oscillations. Proper care during PCB layout in order to minimize current loops while keeping trace lengths short, wide and matched to reduce the amount of parasitic inductance in high current paths will help keep the voltages equal and within the design specification.

References

1. Paralleling of MOSFETs

   J.B. Forsythe, IEEE-IAS Conference Record, October 1981.

2. Analysis of Power MOSFET Performance in Parallel Operation

   QAIN Min, XU Ming-qian, Min Zhi-nan (Institute of Mechanical Engineering, Tongji University, Shanghai 201804, China, 2007.11