Application of Power MOSFETs in Battery Management Charge-Discharge Systems

By Quan Li and Elin Gao

Introduction

Power MOSFETs are required to be connected in series between the lithium-ion battery pack and the output load. At the same time, a dedicated IC is used to control the on and off of the MOSFET for managing the charge and discharge of the battery, as shown in Figure 1. In consumer electronic systems such as cell phones, laptops, etc., the complete circuit system with control IC, power MOSFET, and other electronic components is called the Protection Circuit Module (PCM).

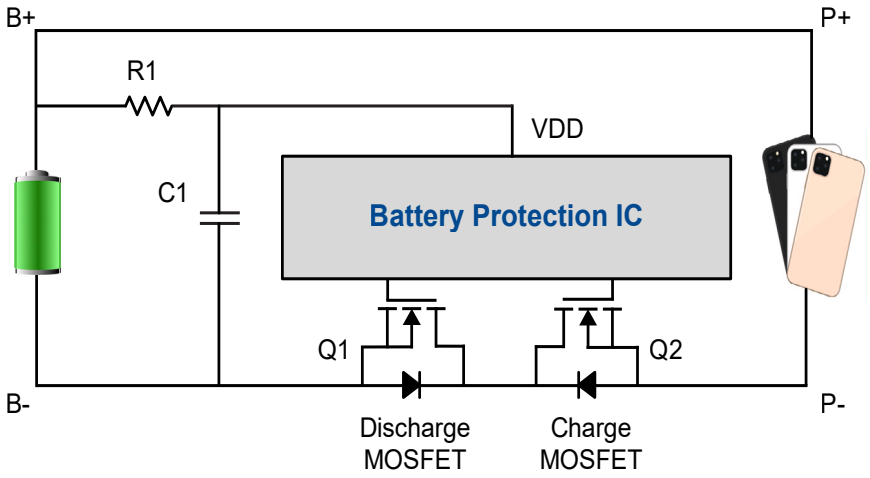


Figure 1. Battery Protection Board Circuit Diagram

In the PCM, one power MOSFET is used for charging and another for discharging. The Power MOSFETs are connected in series, back-to-back, in two configurations. One configuration is when two power MOSFETs drains are connected together. In the second configuration, the two power MOSFETs sources are connected together. In addition, there are two ways to place the power MOSFET in series with the battery. One way is to place it on the negative end of the battery, called “ground end” or low-side; the other one is to place it at the positive end of the battery called the high-side. The two different power MOSFET back-to-back connection modes and their different placement have their own advantages and disadvantages, corresponding to different system requirements.

The PCM requires a low on-resistance MOSFET, so N-channel power MOSFETs are usually used. Some applications use P-channel MOSFETs on the positive end due to simple and flexible driving. However, P-channel MOSFETs on-resistance is relatively higher than N-channel MOSFETs and the selection is also limited.

Power MOSFET Connected Back-to-Back

The Working Principle

The two N-channel power MOSFETs used to manage the charge and discharge are placed at the ground end, and the drains are connected back-to-back, which is one of the common schemes of PCMs (Figure 2). In this configuration, Q1 is the power MOSFET for battery discharge, Q2 is the power MOSFET for battery charge, B+ is the positive end of the battery, B- is the negative end of the battery, P+ is the positive end of the battery pack, P- is the negative end of the battery pack, VSS is the ground of the battery protection management IC, the negative end of the battery, and VSS and the source of Q1 are connected together. Before the PCM board is operational, Q1, Q2 are both off.

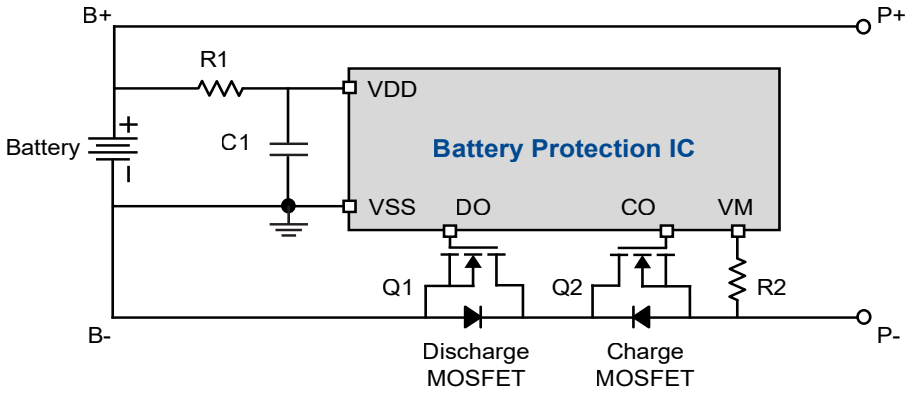


Figure 2. Power MOSFET Ground End and Drain Back-to-Back Circuit Diagram

Charging

When charging, the control IC gate provides the driving signal CO to the charging power MOSFET(Q2), and the driving signal path of Q2 gate is: the positive end of the external charging circuit→P+→B+→R1→VDD→CO→Q2 Source→P-→the negative end of the external charging circuit. A complete driving loop is shown in Figure 3.

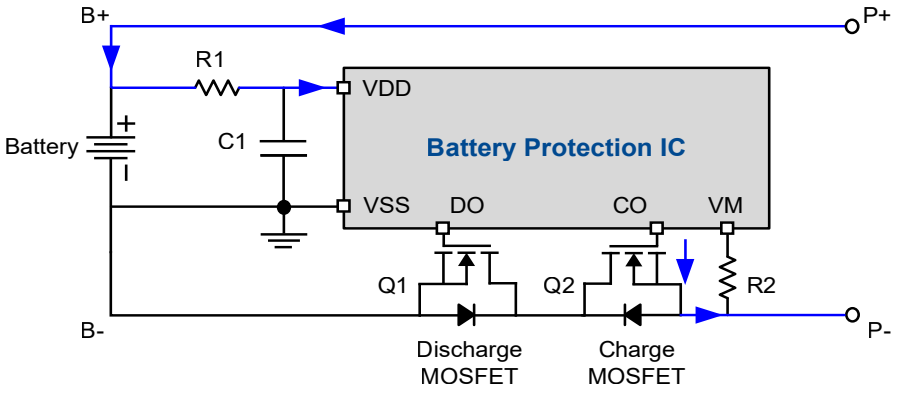


Figure 3. Charging, the Driving Signal Loop of Q2 Gate

When Q2 is on, the charging current path is: P+→B+→B-→Q1 internal parasitic diode→Q2 channel→P-. The battery can then be charged as shown in Figure 4.

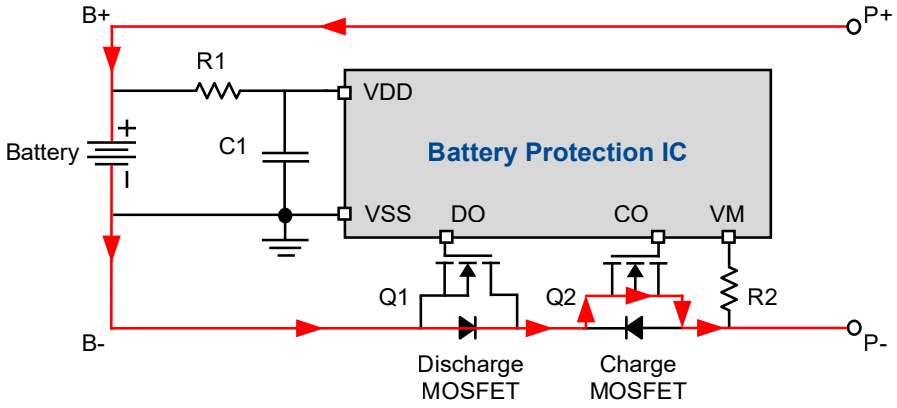


Figure 4. Charging Loop when Q2 is On

In order to reduce the loss of Q1 when Q2 is turned on, the DO pin of the control IC is pulled high to make the discharge power MOSFET Q1 turn on. Due to the low $R_{DS(ON)}$ of Q1, its conduction loss is far lower than that of the parasitic diode, and the efficiency of charging can be improved. The current driving path of Q1 is: VDD→DO→Q1 gate→Q1 Source→B- →VSS, as shown in Figure 5.

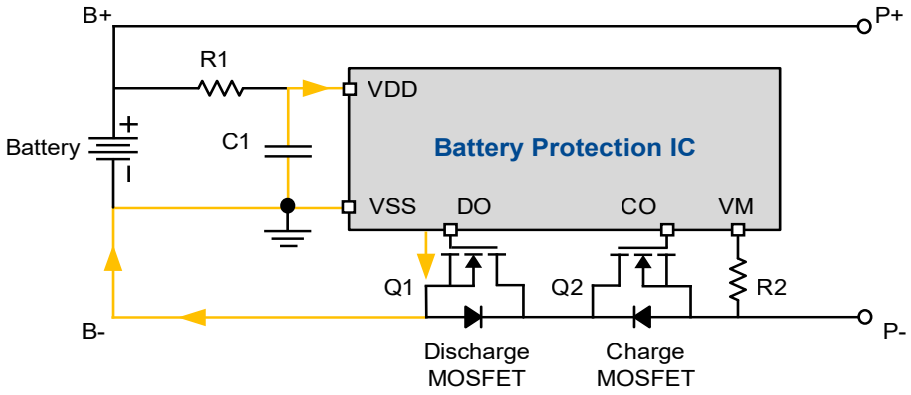


Figure 5. During the Charging, Q1 Drive Signal Loop Output by DO when Q2 is On

When Q2 and Q1 are in the on-state at the same time, the charging current path is: P+→B+→B-→Q1 channel→Q2 channel→P-, as shown in Figure 6.

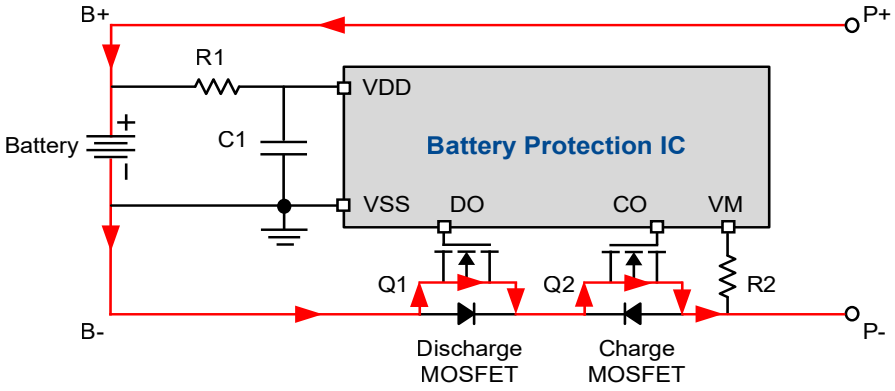


Figure 6. Charging Loop when Q2 and Q1 are On

Discharging

When discharging, the control IC provides the gate drive signal DO to the discharging power MOSFET(Q1), and the gate drive signal path of Q1 is: VDD→DO (Output of driver)→Q1 gate→Q1 Source→B- →VSS, as shown in Figure 7.

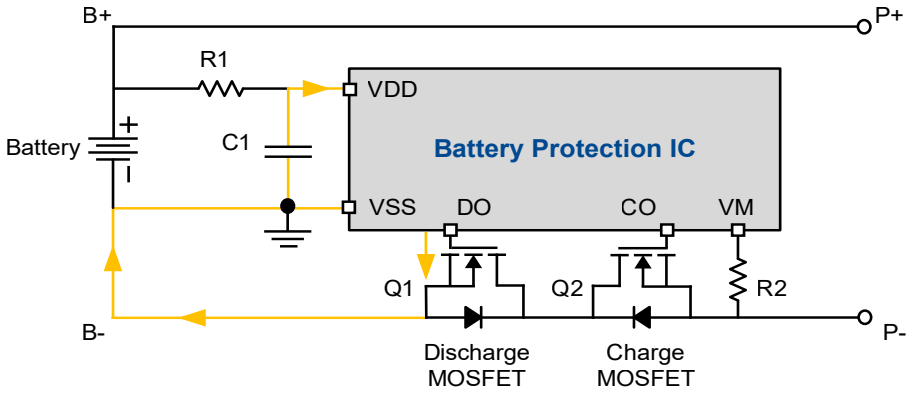


Figure 7. Discharge, Driving Signal Loop of Q1 Output by DO

When Q1 is on, the current path of discharge is: P-→Q2 internal parasitic diode→Q1 channel→B-→B+→P+. The battery can then be discharged, as shown in Figure 8.

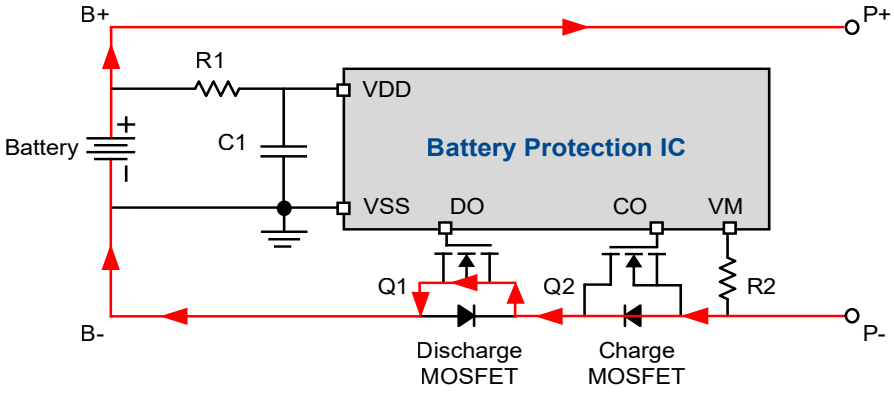


Figure 8. Discharge Loop when Q1 is On

In order to reduce the loss of Q2, when Q1 turns on, the control IC provides the gate drive signal CO to the charging power MOSFET Q2 so that Q2 is turned on. Due to the low conduction resistance of Q2, the conduction loss is far lower than that of the parasitic diode so as to improve the battery service time. The path of Q2 driving current is: VDD→CO→Q2 Gate→Q2 Source→Q2 internal parasitic diode→Q1 channel→B-→VSS, as shown in Figure 9.

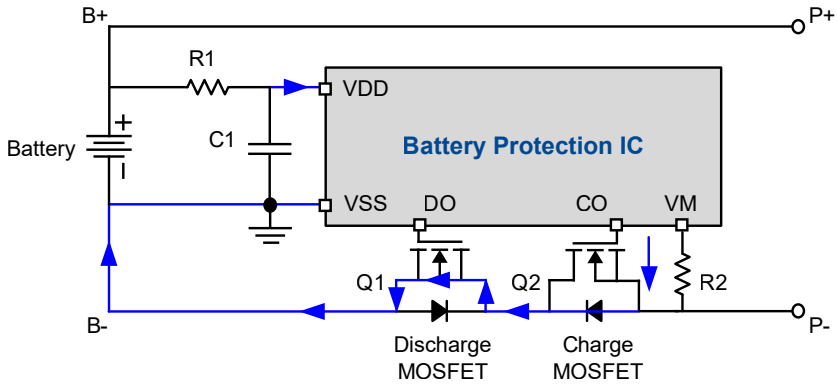


Figure 9. Discharge, Driving Signal Loop of Q2 Output by CO

Q1 and Q2 are in the on-state at the same time, and the path of the discharge current is: P-→Q2 channel→ Q1 channel→B-→B+→P+, as shown in Figure 10.

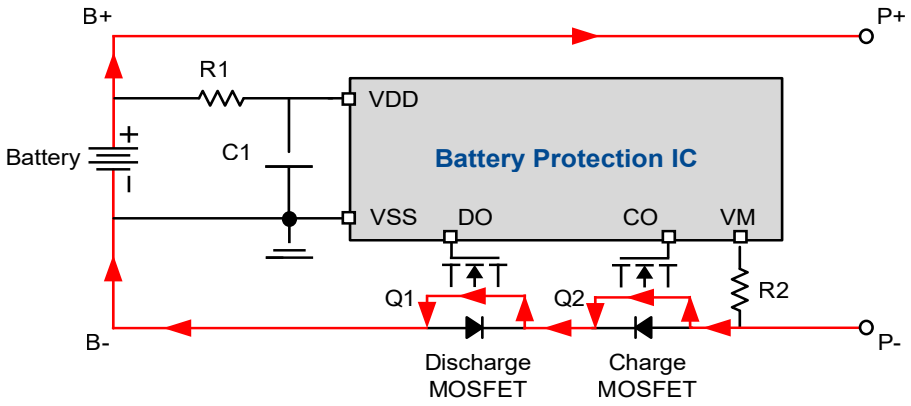


Figure 10. Discharge Loop on Q1 and Q2

Ground End, Source Back-to-Back

The source of the two N-channel power MOSFETs are connected back-to-back and placed on the ground, as shown in Figure 11. This structure is rarely used in PCM, but sometimes used in the load switches and hot-swap circuits of communication systems.

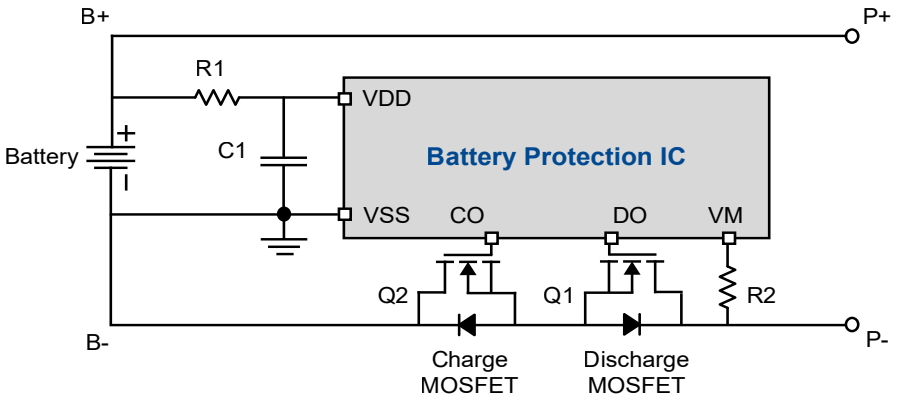


Figure 11. The Source of Power MOSFET are Connected Back-to-Back

Positive End, Drain Back-to-Back

The charging and discharging of the two N-channel power MOSFETs at the power supply end (high-side) where their drains are connected back-to-back, is a common PCM scheme (Figure 12). Q1 is the power MOSFET for battery discharge and Q2 is the power MOSFET for battery charge.

The two N-channel power MOSFETs are placed at the positive end, therefore, two charging pumps are needed to enable a floating drive.

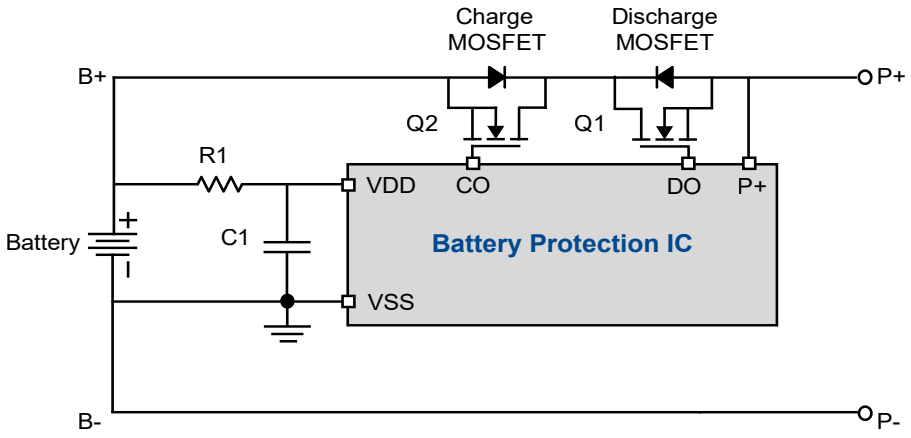


Figure 12. Power MOSFET at High-End, with Drain Connected Back-to-Back

Positive End, Source Back-to-Back

The charging and discharging of the two N-channel power MOSFETs placed at the power supply end (high-side) and their source are connected back to back, as shown in Figure 13. The two N-channel power MOSFETs are the common source, so a charging pump is required for driving. This structure is also used in load switches.

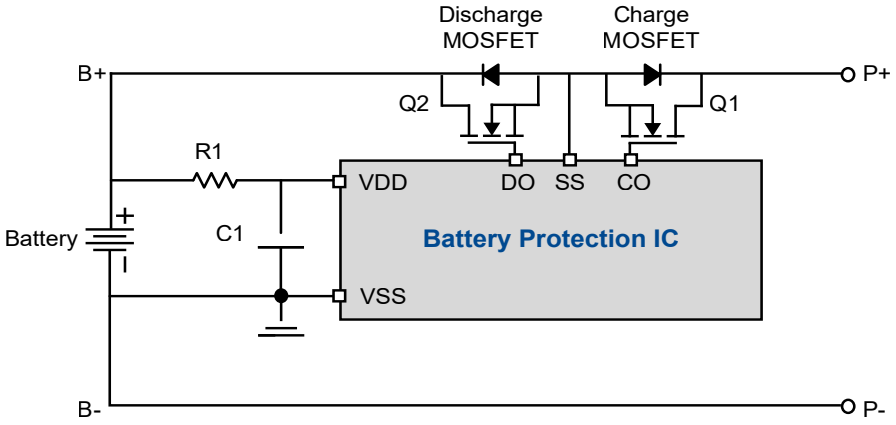


Figure 13. Power MOSFET at High End, with a Source Connected Back-to-Back

Multiple MOSFETs in Parallel with Large Current

At present, in order to improve the service time and standby time of the electronic system, the capacity of the battery is increasing, such as 3000 mAh to 5000 mAh, or even larger. In order to shorten the charging time and improve the charging speed, fast charging is usually adopted, that is, charging the battery through a larger charging current, such as 4A, 5A, 6A, or even as large as 8A. In this way, the power consumption of the PCM internal power MOSFET is very high, and the temperature is very high as well. In order to reduce the temperature rise and ensure the reliable operation of the power MOSFET, two or more MOSFETs can be used in parallel, as shown in Figure.14.

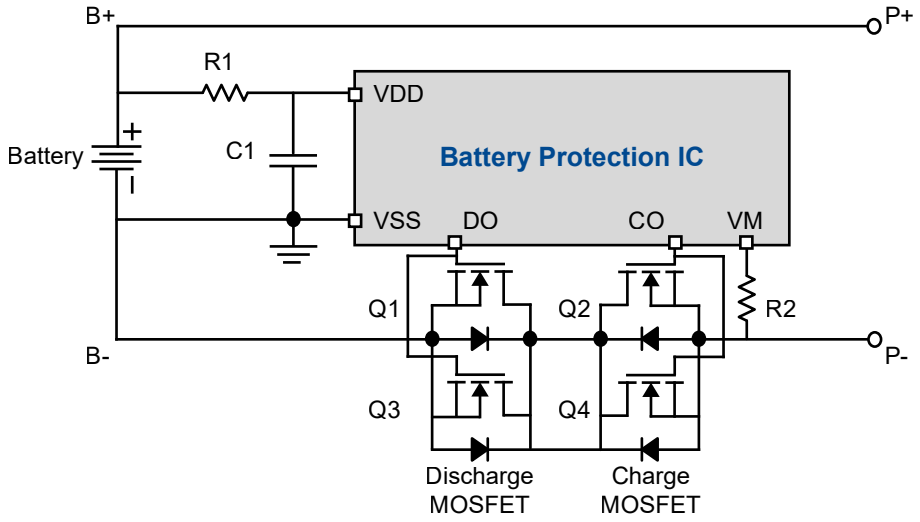


Figure 14. Multiple MOSFETs in Parallel with Large Current

Redundant Design

According to the requirements of the LPS safety regulations, if the power MOSFET inside the PCM is damaged or short when plugged into the charger, the input voltage is applied directly to the battery, which can be dangerous. In order to improve the safety of the system, another set of back-to-back power MOSFET can be connected in series, or other schemes can be used to form redundant design. When the primary protection fails, there is another protection, as shown in Figures 15 to 18.

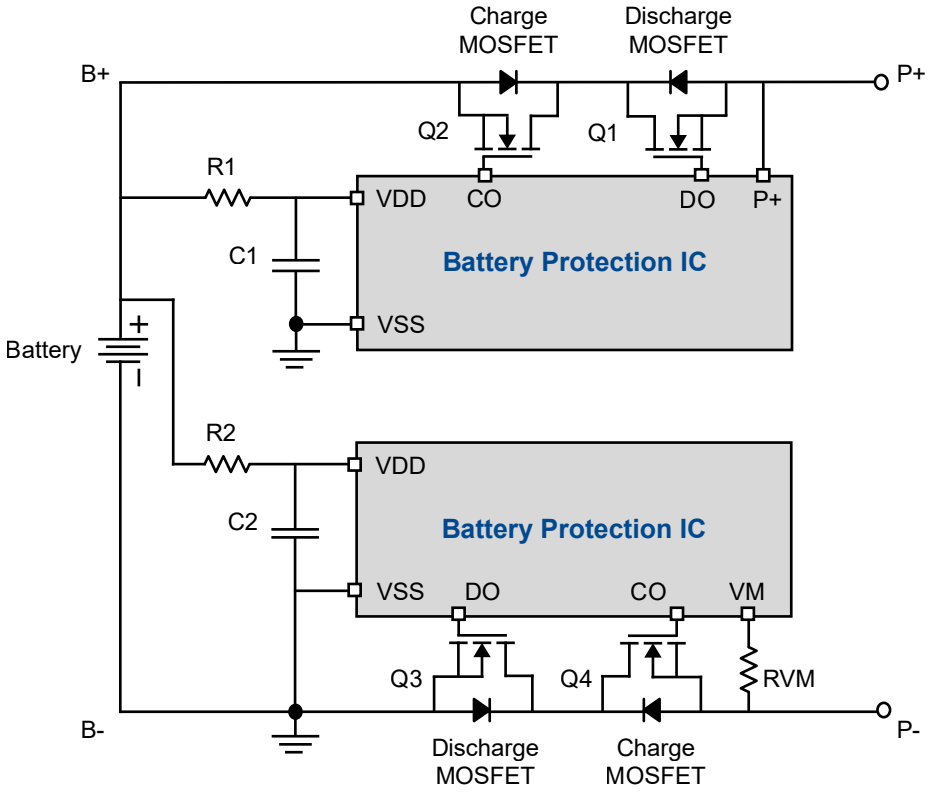


Figure 15. Two Sets of Power MOSFET, One at the High-End and the Other at the Low-End

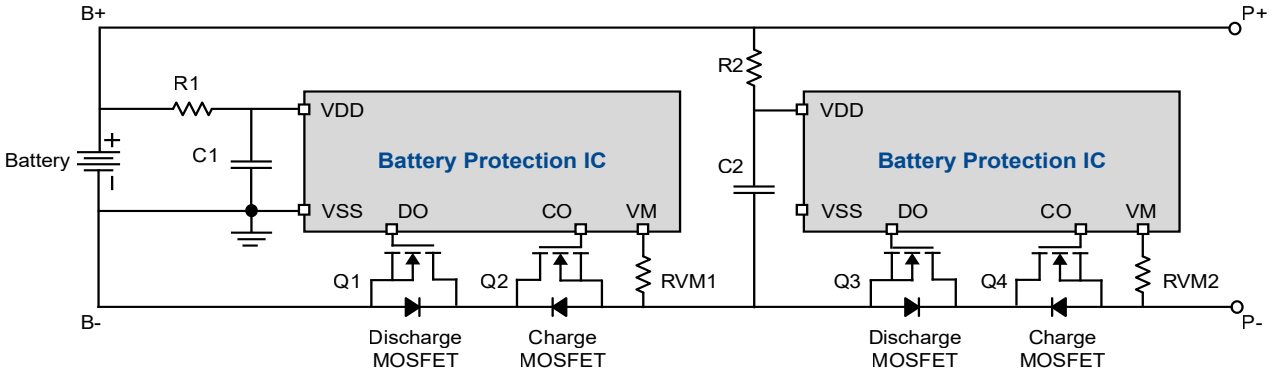


Figure 16. Two Sets of Power MOSFETs at the Low-End

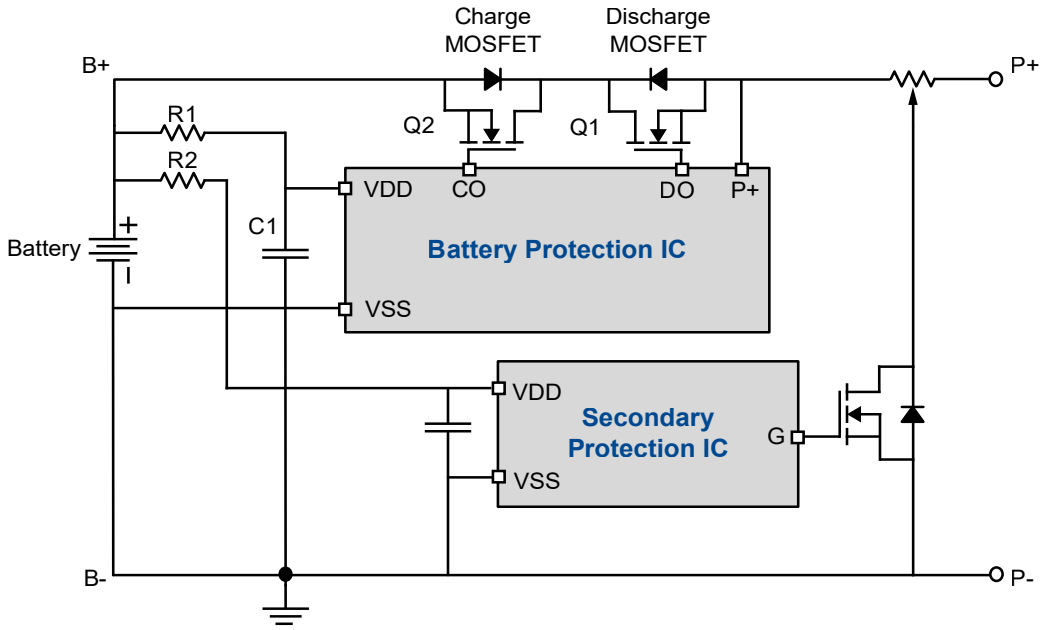


Figure 17. Power MOSFET Placed at the High-End with Electronic Fuse

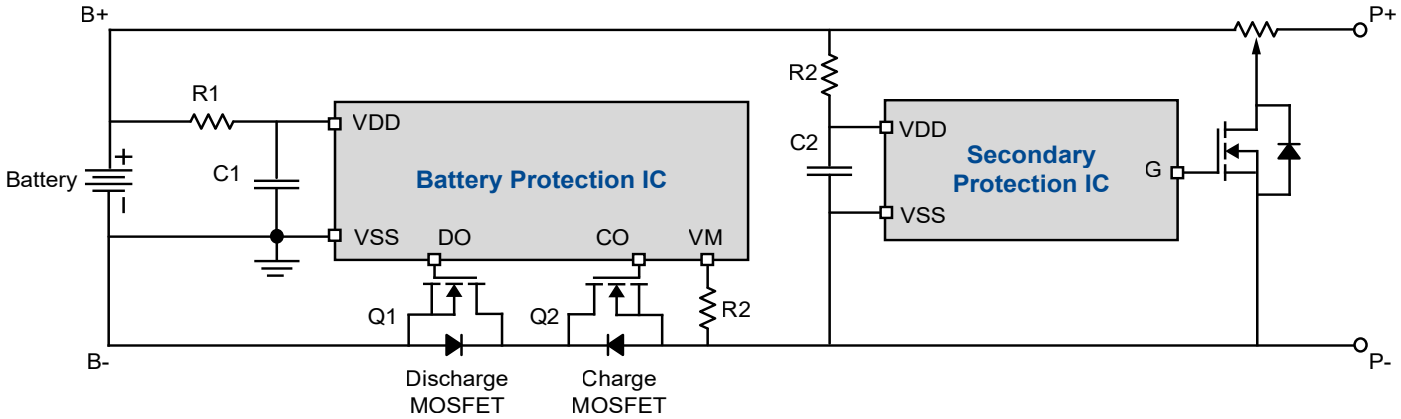


Figure 18. Power MOSFET Placed at the Low-End with Electronic Fuse

Performance Requirements of Power MOSFET

Ion battery capacity from the early 600 mAh, 1000 mAh, to now has reached 6000 mAh, 10000 mAh. In order to achieve faster-charging speed and shorter charging time, the fast charging technology of increasing current and charging with large current is usually adopted. Then, the large current charging puts forward higher technical requirements for the power MOSFET in the battery pack. In addition, there are some specific technical requirements for large-capacity lithium-ion batteries in the production line and in the using process. All of these factors pose strict technical design challenges for the charge and discharge management of power MOSFET in the large-capacity lithium-ion battery package.

High Power Density, Low Power Consumption, Good Heat Dissipation

The basic requirement of large-capacity lithium-ion battery pack design is to improve the capacity of the battery as much as possible under the condition of a certain volume and weight for higher power density. Therefore, the charge and discharge management circuit PCM, including the above power MOSFET, is also required to have a smaller size. Meanwhile, due to the large current during fast charging, the power MOSFET on the PCM is required to have the minimum on-resistance $R_{DS(ON)}$ under a certain size limitation, such as 1.2 mm * 1.2 mm. In theory, a smaller $R_{DS(ON)}$ requires a larger chip size. In order to achieve lower $R_{DS(ON)}$ in smaller chip sizes, the design is mainly optimized from the following two aspects.

(1) Wafer Technology

In order to achieve lower on-resistance $R_{DS(ON)}$ of power MOSFET, it is necessary to improve the MOSFET cell density. Other techniques are used to reduce resistance, such as thick metal and thin wafers. The N-channel power MOSFET can achieve lower on-resistance $R_{DS(ON)}$ in a reduced form factor.

(2) Packaging Technique

Power MOSFET packages usually use leads. In order to further reduce on-resistance, in PCM, the package wire resistance is completely removed by using a new chip-level CSP packaging technology. At the same time, the packaging technology of the chip level CSP has better thermal conductivity, thus reducing the temperature rise of the power MOSFET, which helps to improve its reliability.

The power MOSFET using CSP packaging technology without the external plastic shell and other materials protection will be affected by various thermal stress and mechanical stress in the process of PCM production, such as the welding process of PCB board, which could result in a high risk of die crack. Therefore, various technologies should be used, such as coating new materials on the surface of power MOSFET chips to ensure their ability to resist mechanical stress and thermal stress and to improve reliability.

Short Circuit Capability

Large-capacity lithium-ion battery in the application, especially in extreme conditions, such as the output load short, there is a very large current through the battery. When IC detected output over-current, it will delay for a period of time to make protection action. During the delay time, the operating current of MOSFET is very large, which requires the MOSFET to be robust for large current stress. As a result, all lithium-ion batteries are required to do short circuit tests.

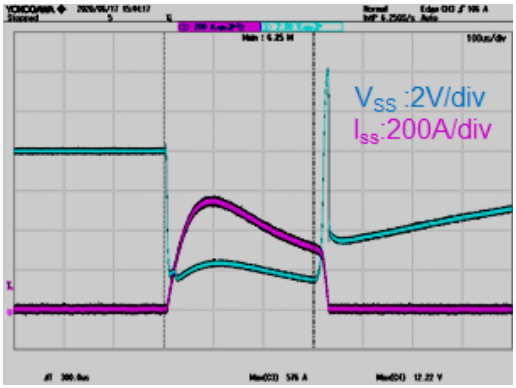


Figure 19. Pass of the Short Test

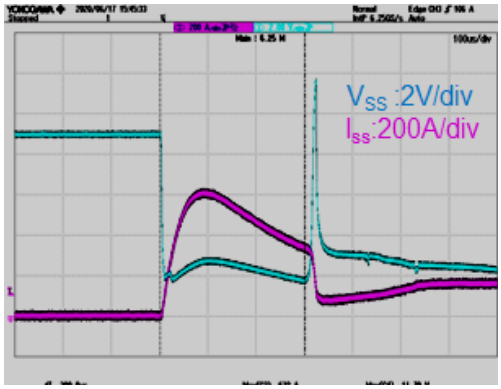


Figure 20. Fail of the Short Test

In theory, the larger the chip size, the stronger the robustness for short circuit current. However, with the trend of smaller form factors, there will be a limit of the capability. Thus, the application circuit design needs to keep in mind the requirements needed to ensure a robust design to resist the impact of a large short circuit current.

Avalanche Robustness

The MOSFET Avalanche capability is important when the output end of the battery pack is a short circuit, and the switch is off. The selection of the power MOSFET should include a sufficient avalanche capability determined by the application conditions.

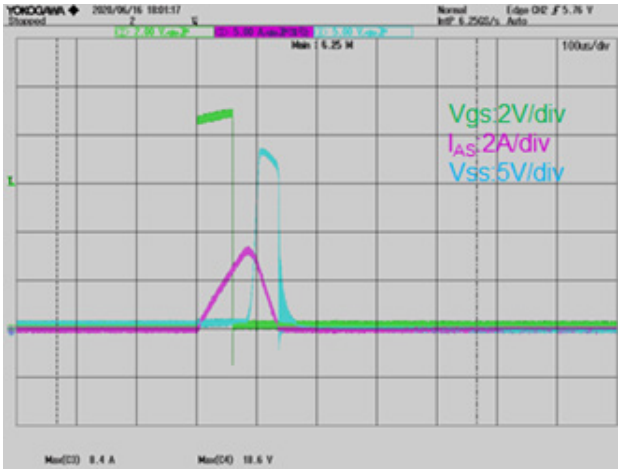


Figure 21. Pass of the Avalanche Test

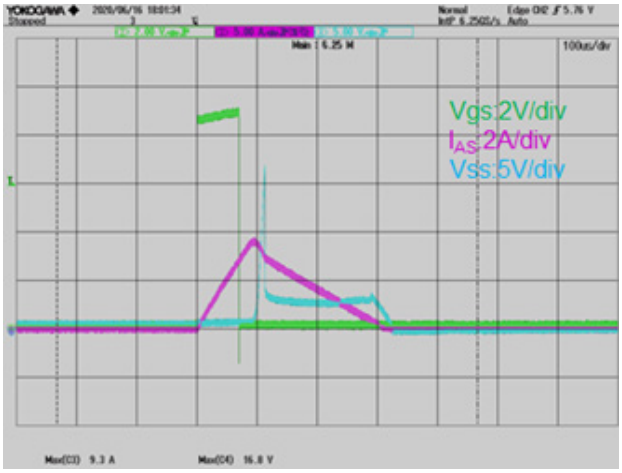


Figure 22. Fail of the Avalanche Test

dv/dt Protection

During a reverse connection test, the maximum per cell operation voltage is 4.4 V, the maximum charge voltage is also 4.4 V. When the charger reverse connects to the battery pack, the MOSFET suffered 8.8 V voltage stress. In the production process of large-capacity lithium-ion batteries, the external DC power supply will directly touch the two output ends of the battery pack during the test. For this reason, MOSFET suffered 8.8 V high dv/dt voltage stress.

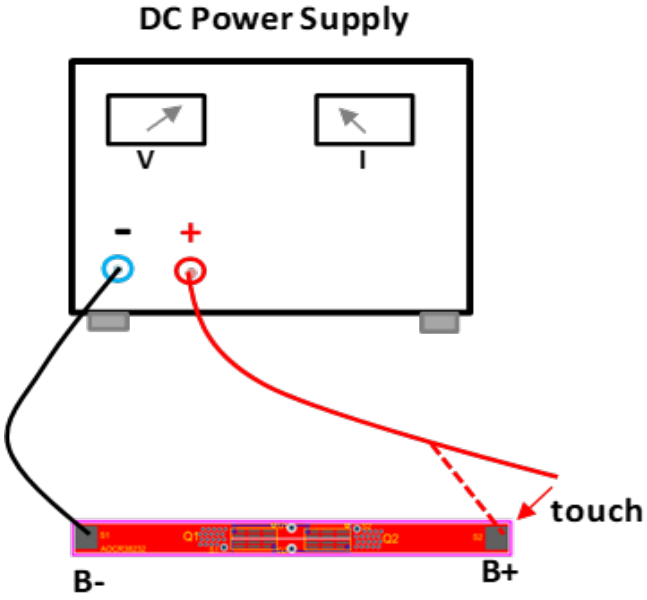


Figure 23. Touch Test Diagram

If the MOSFET experiences a high dv/dt across the drain to source, the parasitic capacitance CDS will have a charging current of I = CDS * dv/dt. If the current is large enough, it will trigger the parasitic npn bipolar to turn-on and the MOSFET can be easily damaged.

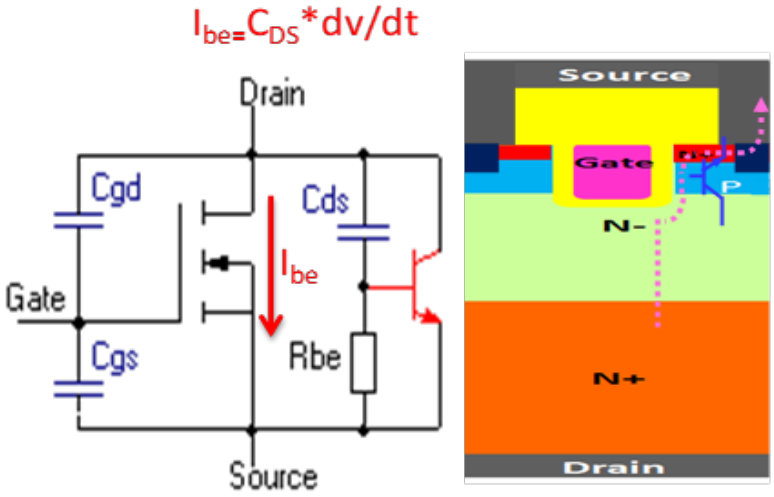


Figure 24. High dv/dt Bipolar Turn On Diagram

To avoid damage to the circuit, the higher the voltage directly touched, the stronger the robustness of the battery pack. This test is the actual measurement of the tolerance of MOSFET to dv/dt. Usually, the large dynamic dv/dt will also be generated in the process of the battery pack output short and protection shutdown. The excessive high dv/dt will cause dynamic avalanche damage to the power MOSFET. Therefore, it is necessary to optimize the structure of the power MOSFET to ensure that it has enough immunity for high direct touch voltage and high dv/dt.

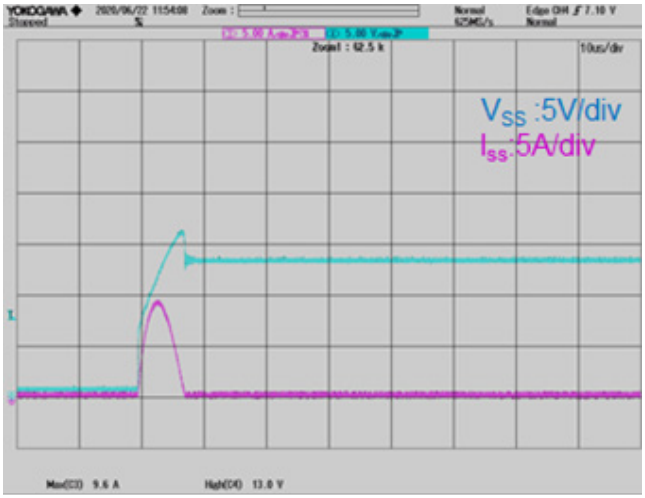


Figure 25. Pass of the 13 V Direct Touch Voltage Test

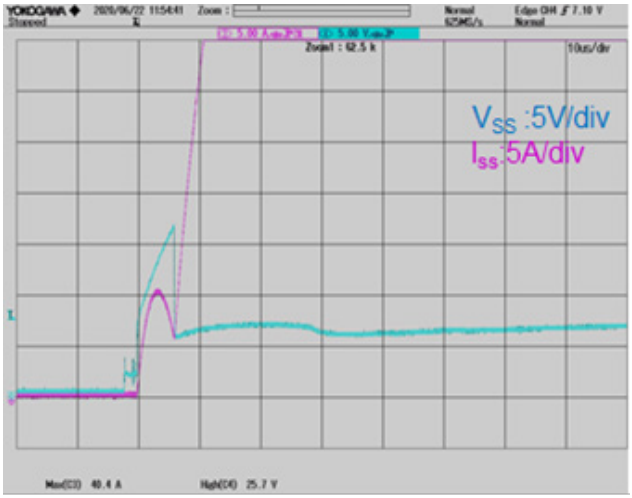


Figure 26. Fail of the 14 V Direct Touch Voltage Test

The below test result shows that competitor-B does not meet the minimum requirement of the reverse connection test: 8.8 V direct touch test. AOCA33104E passes the 17 V direct touch test and it shows stronger robustness in high dv/dt stress.

Table 1. Direct Touch Voltage Test Results

Part Number	Direct Touch Pass Voltage (V)
AOCA33104E_1#	17
AOCA33104E_2#	18
AOCA33104E_3#	17
CompetitorA_1	14
CompetitorA_2	14
CompetitorA_3	14
CompetitorB_1	7
CompetitorB_2	7
CompetitorB_3	7

Key Points of PCB and Thermal Design

The temperature of the MOSFET usually does not exceed 65°C in normal environment temperature. The PCM control board is generally assembled together with the battery, and the PCB size is a constraint and typically high thermal resistance. Thus, special considerations may be needed on the thermal design for the system.

For example, the charging voltage of the single-cell phone quick charger of 47 W is 5 V, and the maximum charging current is 9.4 A. The typical $R_{DS(ON)}$ of AOCR38232 is about 0.8 mΩ, and two pieces of AOCR38232 are needed in parallel to reduce the resistance further. The current path is symmetrical between the top and the bottom of the board to maintain the current balance. In this example, the distance between two MOSFETs is about 3 mm to avoid heating each other. Maximizing the copper area of the power path and adding some vias for dissipation on the copper pads near the MOSFET are good design tips to improve the heat dissipation capacity and to reduce the rising temperature of the MOSFET.

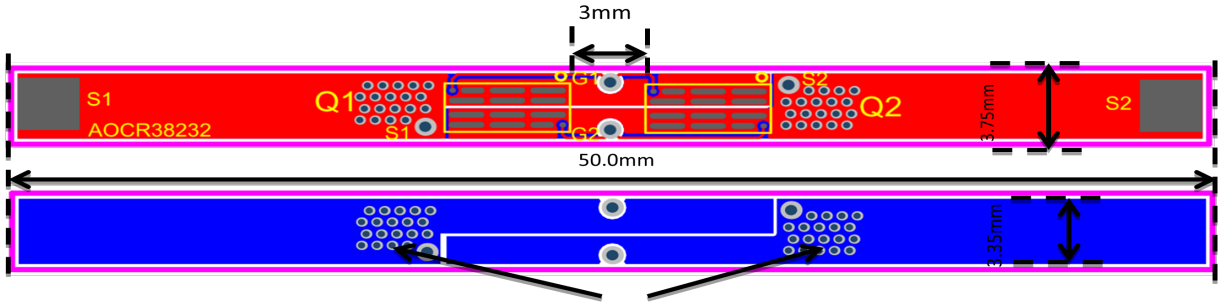


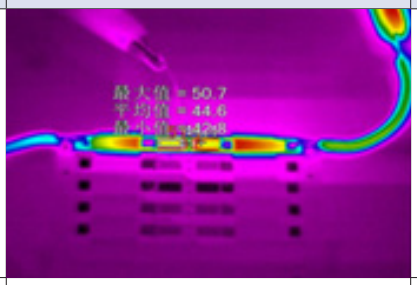
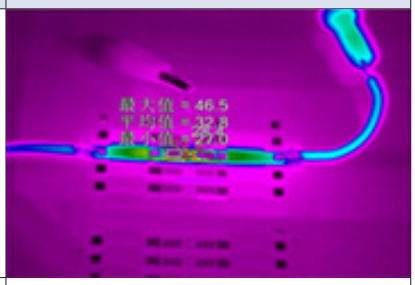
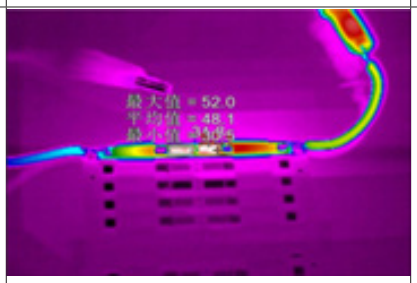
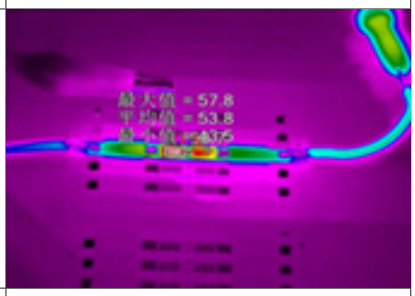
Figure 27. Heat Sink: Aperture 12 mil, Spacing 25 mil

When using an infrared (IR) thermometer to measure the surface temperature rise of the MOSFET, you will need to ensure proper usage of the IR thermometer since the surface emissivity can be different between different MOSFETs. Therefore, the optical refractive indexes are also different. Metal has a lower optical refractive index than silicon. If the thermal measurement shows a lower temperature with higher $R_{DS(ON)}$ compared with lower $R_{DS(ON)}$, under the same conditions. Intuitively these measured results are incorrect.

In order to get the most accurate measured temperature, the rise of MOSFET with an infrared thermometer, it is best to coat the surface with the recommended black paint for a high optical refractive index. In this way, a more accurate temperature rise could be obtained without taking different materials into consideration.

When black paint is used on the surface of AOCR38232, the measured temperature rise was only increased by 1.3 °C. Without any coating on the surface, the temperature rise was increased by 11.3 °C. The results are shown as follows.

Table 2. Temperature Rise with and without Coating

Part Number	9.4A for 10 Minutes	Part Number	9.4A for 10 Minutes
AOCR38232 without Coating		Competitor without Coating	
Max	50.7°C	Max	46.5°C
AOCR38232 with Coating		Competitor with Coating	
Max	52°C	Max	57.8°C
Difference With/Without	+1.3°C	Max	+11.3°C

Output Leakage Current

In the battery pack production process, even though the charge MOSFET and discharge MOSFET are both off, when the battery voltage imposes on the MOSFET, sometimes it still causes the output leakage current through the MOSFET. Usually, the leakage current is very small and has no effect on the system. However, if the leakage current is higher, up to 100 nA, which is still within the limits of the datasheet, this leakage current will have a certain voltage on the output impedance.

Usually, the output impedance is around 10 MΩ. The voltage is equal to the product of the output impedance and the leakage current. In the above conditions, the output voltage is 1 V, 100 nA * 10 MΩ. Using BQ20Z45, when the output voltage is between P+ and P- is higher than 0.8 V, the IC will judge that the charging voltage is imposed on the P+ end. The charge MOSFET is turned on by the pre-charging function of the IC attempting to charge the battery. As a result, the IC starts to operate, and the static power loss of the battery will be increased. In critical cases, the battery will run out of power.

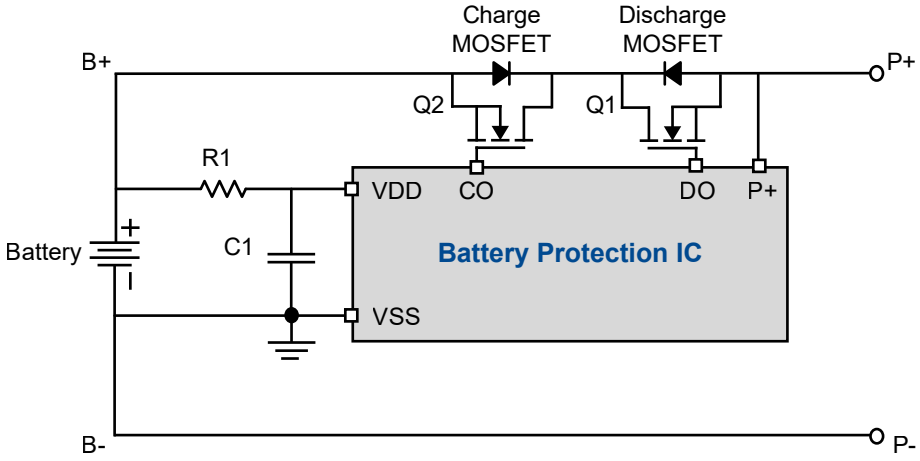


Figure 28. Battery Protection Board Circuit Diagram

Usually, IDSS of 30 V MOSFET is less than 1 µA in the datasheet. In a practical notebook battery application, the battery voltage is usually from 9 V to 13.2 V. It is unknown whether the leakage current IDSS of the discharge MOSFET is higher than 100 nA or not under the battery voltage of 13.2 V.

Solutions to Avoid Output Leakage Current

In an actual system, the output terminals of the battery are connected to the motherboard, which includes capacitors, resistors, and many other devices. These components could enable a certain leakage current. The measured impedance of the interfaces of the motherboard battery is generally less than 1 MΩ. The above leakage current through 1 MΩ impedance should not result in any issue in the system after the battery pack is connected.

There are two solutions to avoid output leakage current impact when the battery pack is not connected to the motherboard during any stage of manufacturing steps.

Solution: It is recommended to place a 1 MΩ resistor in parallel with the output terminals of the battery pack P+ and P-, as shown in Figure 28. The issue can be removed effectively after testing the actual application of customers.

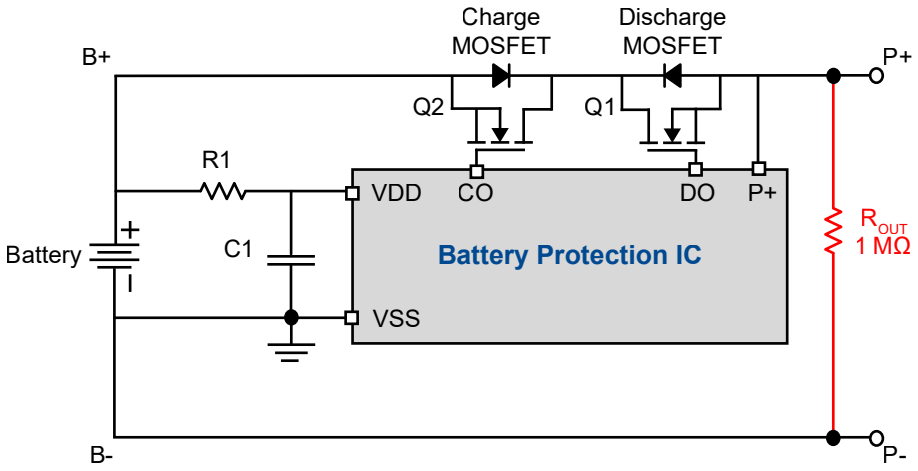


Figure 29. Parallel Output Resistor

After adding a 1 MΩ resistor, the P+ terminal voltage caused by the leakage current will drop to 0.46 V, and the MOSFET is not turned on by BQ20Z45 anymore.

Table 3. P+ Voltage vs. Output Resistance

Leakage Abnormal Board					
Parallel Resistance	None	8.2 M	6.2 M	2.7 M	1 M
P+ Voltage	5.5 V	1.03 V	0.92 V	0.81 V	0.46 V

The disadvantage of placing this resistor is that is causes the battery to lightly discharge. For example, if the leakage current through this resistor is 0.46 µA = 0.46 V/1 M. The total energy consumed by the resistor during ten years of battery pack storage time is equal to 0.46 µA * 24 hours * 365 days * 10 years = 40.3 mA * hours. It is only less than 1 percent of the normal 4100 mA * hour battery energy of the notebook. It is not a problem.

The output 1 MΩ discharge resistor can also be placed on the test station of battery pack manufacturing lines.

Solution B: It is recommended that the value of detecting the P+ terminal voltage for pre-charging function inside IC should be increased from 0.8 V to 2 V for a single battery and to 6 V for three battery cells in serial. The system could be normal even though the leakage current is larger.

LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. AOS does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS's products are provided subject to AOS's terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.