Buck-Boost Charger MOSFETs

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Introduction

The wide adoption of USB Type-C PD makes the notebook PC charger move to four MOSFET buck-boost charger topology (Figure 1) to allow for wide range input voltage (5-20V). After a suitable controller is selected, the specified Power MOSFETs in buck-boost charger are essential for achieving higher efficiency and high-power density design.

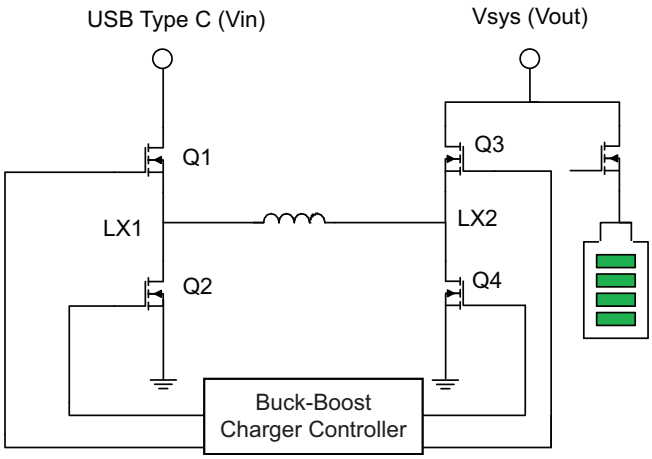

Figure 1. Buck-Boost Charger Topology

In this application note, we will only discuss the USB power delivery specification for an adapter supplying 5A / 100W and expect the reader to understand the basic operation of buck-boost topology. It is critical to select suitable MOSFETs regarding efficiency, thermal, and space limitation, to meet the system-level requirements. 30V MOSFETs can be used for input voltage below 20V.

Based on given wide input voltages, output voltages, and current, the designer must understand the tradeoff among the different loss mechanisms in the MOSFET. These MOSFET losses include: switching loss, conduction loss, and reverse recovery loss. Losses are minimized by selecting the best MOSFETs from its electrical characteristics.

Power Loss of MOSFET

We will consider the following modes: buck, boost, and buck-boost.

Buck Mode

The buck mode is the most common topology, and can generate the highest total power loss. Using Figure 2, when the charger works at buck mode, Q3 is always on. Q3 power loss is related to Rdson. Q4 is always off with no power loss. The designer should focus the MOSFET selection on the Buck mode.

The following equations are used to determine the power losses on each MOSFET in Figure 2.

Q1 loss: switching loss $\left(\frac{1}{2} I_{OUT} \cdot V_{IN} (t_r + t_f) f + \frac{1}{4} V_{IN} \cdot f \cdot I_{Lripple} \cdot (t_f - t_r)\right)$,

conduction loss $\left(I_{OUT}{}^2 \cdot R_{DSON} \cdot D + \frac{1}{12} \cdot I_{Lripple}{}^2 \cdot R_{DSON} \cdot D\right)$,

gate drive loss $\left(Q_g \cdot V_{gs} \cdot f\right)$,

Qoss loss $(\frac{1}{2} Q_{oss} \cdot V_{in} \cdot f)$,

Q_{2rr} loss $(Q_{2rr} \cdot V_{in} \cdot f)$

Q2 loss: conduction loss $(I_{OUT}^2 \cdot R_{DSON} \cdot (1-D + \frac{1}{12} \cdot I_{Lripple}^2 \cdot R_{DSON} \cdot (1-D))$,

body diode loss $(V_{SD} \cdot f \cdot I_{OUT} \cdot t_{total\_deadtime})$,

gate drive loss $(Q_g \cdot V_{gs} \cdot f)$,

Q3 loss: conduction loss $((I_{OUT}^2 + \frac{1}{12} \cdot I_{Lripple}^2) \cdot R_{DSON})$

Q4: off

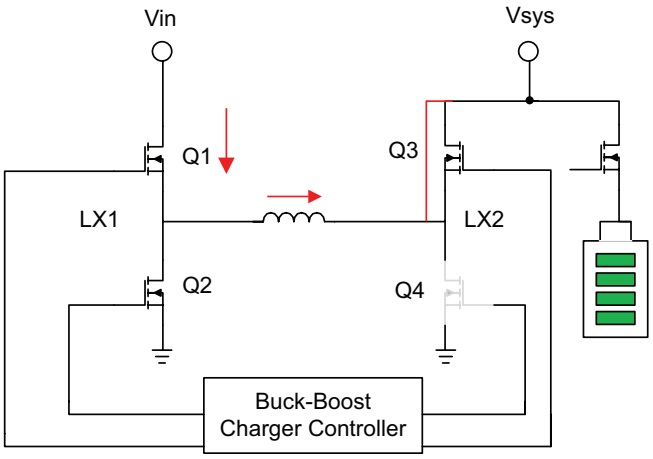

Figure 2. Buck Mode Charger Topology

Boost Mode

When the charger works in the boost mode, the output current is smaller compared to buck, therefore power dissipation is reduced. The designer can decide not need to optimize the MOSFET selection for the boost mode since the power losses are not as significant as in buck more operation.

Using Figure 3, Q1 is always on and power loss is from Rdson. Q2 is always off with no power loss.

Q1 loss: conduction loss $(\frac{I_{OUT}^2}{(1-D)^2} \cdot R_{DSON} + \frac{1}{12} \cdot I_{Lripple}^2 \cdot R_{DSON})$.

Q2: off.

Q3 loss: conduction loss $(\frac{I_{OUT}}{1-D} \cdot R_{DSON} + \frac{1}{12} \cdot I_{Lripple}^2 \cdot R_{DSON} \cdot (1-D))$,

body diode loss $(\sim V_{SD} \cdot f \cdot \frac{I_{OUT}}{1-D} \cdot t_{total\_deadtime})$,

gate drive loss $(Q_g \cdot V_{gs} \cdot f)$

Q4 loss: switching loss $(\frac{1}{2} \cdot (\frac{I_{OUT}}{1-D} + \frac{1}{12} \cdot I_{Lripple}) \cdot (V_{OUT} + V_{SFET}) \cdot t_r \cdot f + \frac{1}{2} \cdot (\frac{I_{OUT}}{1-D} - \frac{1}{2} \cdot I_{Lripple}) \cdot (V_{OUT} + V_{SFET}) \cdot t_r \cdot f)$,

conduction loss $(\frac{I_{OUT}^2}{(1-D)^2} \cdot R_{DSON} + \frac{1}{12} \cdot I_{Lripple}^2 \cdot R_{DSON}) \cdot D)$, Qoss loss $(\frac{1}{2} Q_{oss} \cdot (V_{OUT} + V_{SFET}) \cdot f)$, Q3rr loss

$(Q_{3rr} + V_{OUT} \cdot f)$

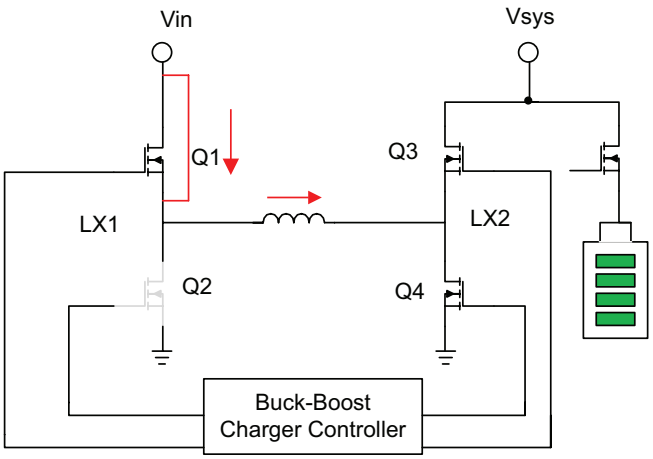

Figure 3. Boost Mode Charger Topology

Buck-Boost Mode

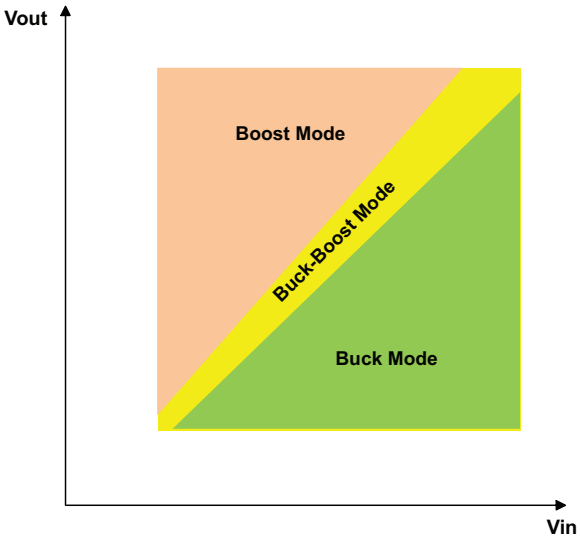

Figure 4. Operation Mode over Variation of Input and Output Voltage

When Vin and Vout voltages are close, referring to Figure 4, the charger operates in buck-boost mode. In buck or boost mode, only three of four MOSFETs are working, in buck-boost all four MOSFETs work and have to look at all the losses in each MOSFET and the efficiency of the charger should be lower than the expectation. Figure 5 and Figure 6 show two different operating schemes for buck-boost mode. The following shows calculation of MOSFET power losses of for scheme1.

Since Vin≈Vout, $I_{Lmax}-I_{Lmin}=I_{Lripple}=\frac{V_{OUT}}{L\cdot f}(1-D_{buck})\cong\frac{V_{IN}}{L\cdot f}\cdot D_{boost}$

Q1 loss: switching loss $(\frac{1}{2}Vin\,(I_{Lmin}\cdot t_r+I_{Lmax}\cdot t_f)f)$,

conduction loss $((\frac{(I_{Lmax}{}^2+I_{Lmin}{}^2+I_{Lmax}+I_{Lmin})}{3}\cdot D_{boost}+I_{Lmax}{}^2\cdot(D_{buck}-D_{boost}))\cdot R_{DSON}$,

gate drive loss $(Q_g\cdot V_{gs}\cdot f)$, Qoss loss $(\frac{1}{2}Q_{oss}\cdot V_{in}\cdot f)$,

Q2rr loss $(Q_{2rr}+V_{IN}\cdot f)$

Q2 loss: conduction loss $\left(\left(\frac{(I_{Lmax}^2+I_{Lmin}^2+I_{Lmax}\cdot I_{Lmin})}{3}\right)\cdot(1-D_{buck})\cdot R_{DSON}\right)$,

body diode loss $(V_{SD}\cdot f\cdot I_L\cdot t_{total\_deadtime})$,

gate drive loss $(Q_g\cdot V_{gs}\cdot f)$

Q3 loss: conduction loss $\left(\left(\frac{(I_{Lmax}^2+I_{Lmin}^2+I_{Lmax}\cdot I_{Lmin})}{3}\right)\cdot(1-D_{buck})+I_{Lmax}^2\cdot(D_{buck}-D_{boost})\right)\cdot R_{DSON})$,

body diode loss $(\sim V_{SD}\cdot f\cdot I_L\cdot t_{total\_deadtime})$,

gate drive loss $(Q_g\cdot V_{gs}\cdot f)$

Q4 loss: switching loss $\left(\frac{1}{2}\cdot I_{Lmax}\cdot(V_{OUT}+V_{SFET})\cdot t_f\cdot f+\frac{1}{2}\cdot I_{Lmin}\cdot(V_{OUT}+V_{SFET})\cdot t_f\cdot f\right)$,

conduction loss $\left(\left(\frac{(I_{Lmax}^2+I_{Lmin}^2+I_{Lmax}\cdot I_{Lmin})}{3}\right)\cdot D_{boost}\cdot R_{DSON}\right)$,

Qoss loss $\left(\frac{1}{2}Q_{oss}\cdot(V_{OUT}+V_{SFET})\cdot f\right)$,

Q3rr loss $(Q_{3rr}+V_{OUT}\cdot f)$

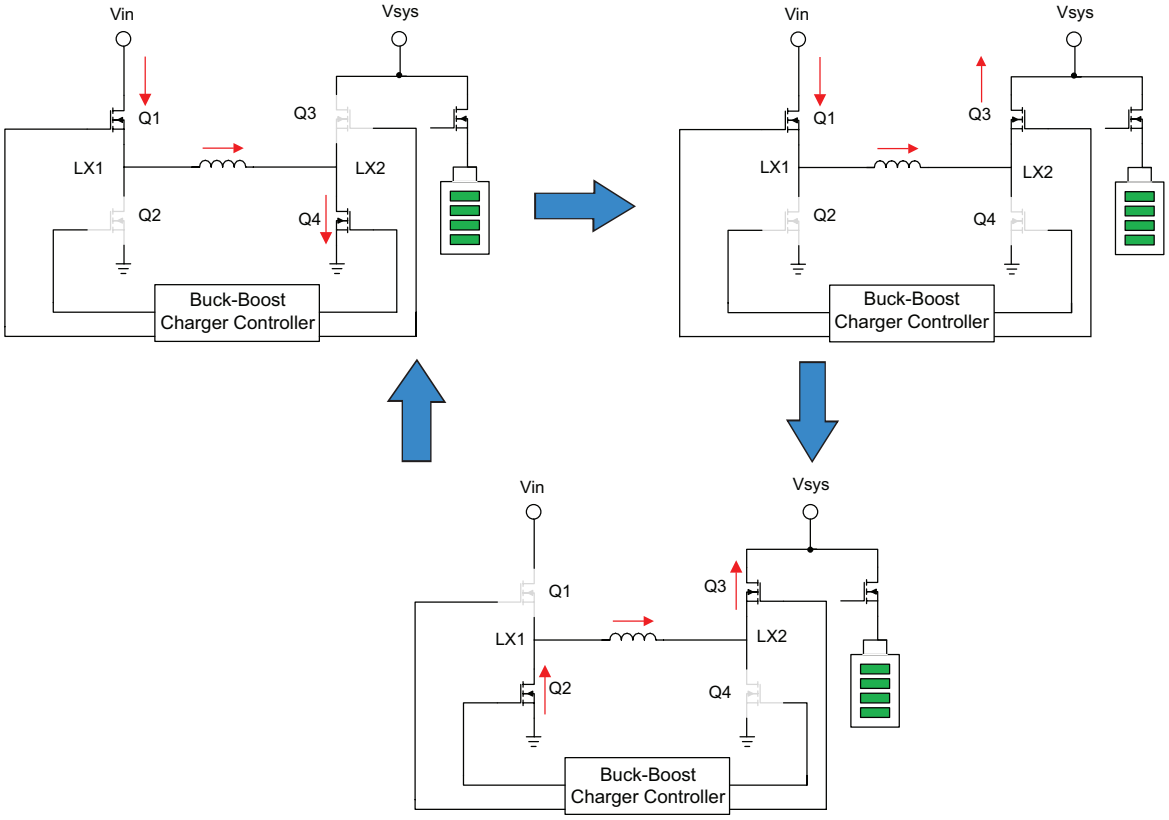

Figure 4a. Buck-Boost Mode Charger Topology

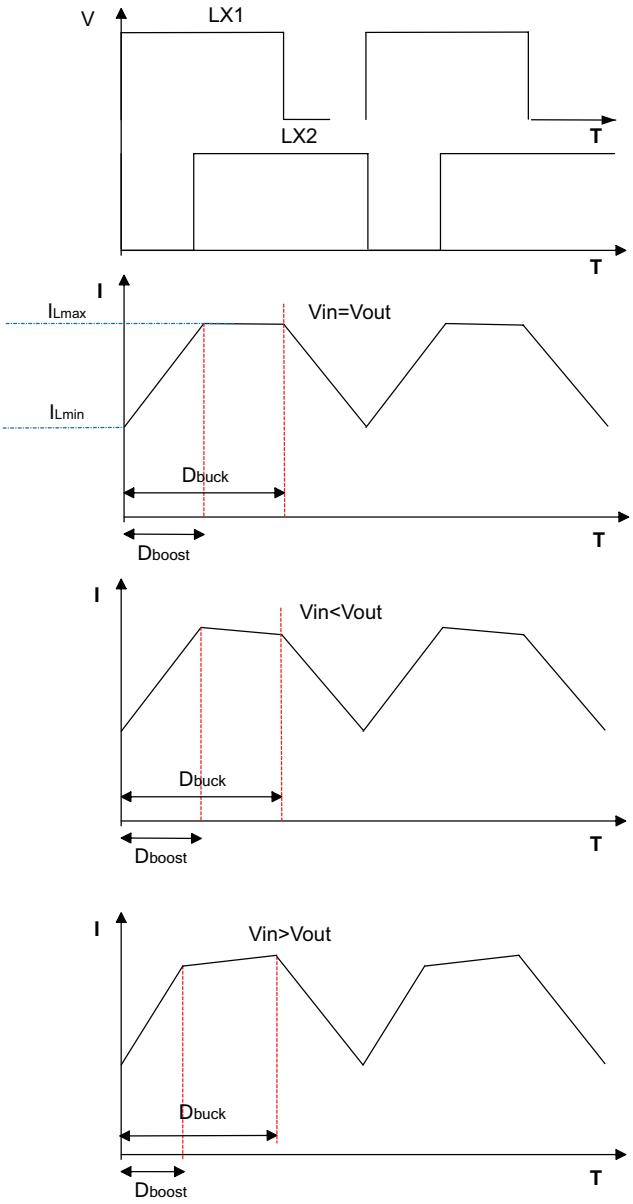

Figure 5. Buck-Boost Mode Inductor Current-Scheme 1

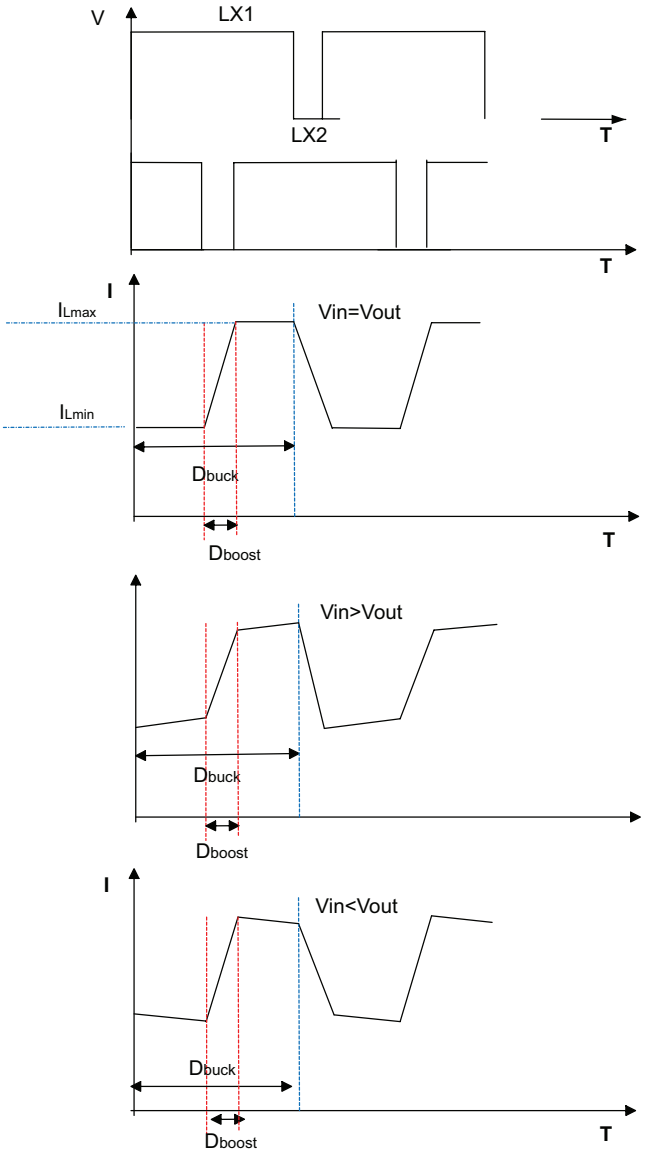

Figure 6. Buck-Boost Mode Inductor Current-Scheme 2

MOSFET Selection

Most of the time, the battery charger operates in buck mode. Therefore, losses associated from buck mode will be the major focus. The selection of a suitable MOSFET for buck-boost charger application will be reviewed. A comparison of AONP36336 and AOE6936 will be reviewed as a case study to understand which key parameters should be of concern when designing a buck-boost charger.

The operation conditions are 20V input to 13.2V output, with output current up to 10A, operating at 840kHz switching frequency. The package outline of AONP36336 is DFN3.3x3.3. AOE6936 is DFN5x6, which includes low-side with a source-down configuration. With the same external components and similar layout, we found AONP36336 outperformed AOE6936 in efficiency and thermal performance (Figure 7 and Table 2,3).

After analyzing each MOSFET loss (refer to table 1) with datasheet characteristics, we find that switching loss, conduction loss from Q1, and reverse recovery loss are key parameters that highlight the efficiency gap between these parts. In short, Qgd and Rdson from Q1 and Qrr from Q2 are key factors. The calculations closely match the measured result.

AONP36336 shows greater power density (smaller package) and is more suitable for the type-C buck-boost charger application. After fine-tuning the key MOSFET parameters, Figure 8 shows AONP36332 could provide better performance for 100W and above in buck-boost charger application (see Table 4). Both AONP36332 and AONP36336 have the same package and pinout, making them excellent choices for a buck-boost charger.

In conclusion, AONP36336 and AONP36332 provide high efficiency and higher-power density than existing Buck MOSFET solutions such as AOE6936, which are designed for lower output voltage application.

Parameter	AOE6936		AONP36336		AONP36332	
	H/S FET	L/S FET	H/S FET	L/S FET	H/S FET	L/S FET
Rdson (mOhm) @Vgs=4.5V max.	8	3	5.7	7.3	4.7	5.9
Ciss (pF)	1150	2270	1330	940	1520	1220
Coss (pF)	380	650	280	210	330	260
Crss (pF)	55	90	35	30	35	30
Rg (Ohm)	1.2	1.4	0.8	1.8	0.8	1.9
Qg (nC) @Vgs=4.5V	7.5	15	8	6	10	7.5
Qrr		30		14		15

Table 1. Key Parameters of MOSFET

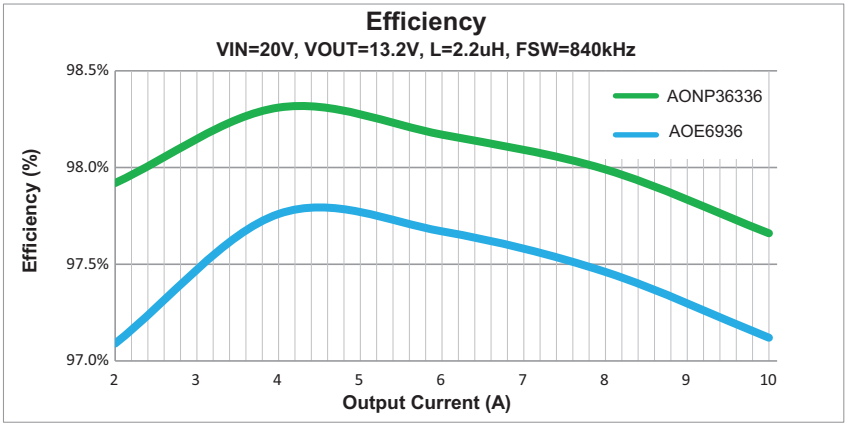

Figure 7. VIN=20V/VOUT=13.2V Efficiency Comparison Curve

Parameter	AONP36336	AOE6936
Vin=20V, Vout=13.2V, Iout=10A, 840kHz	0.32	0.5
HS switching Loss	0.38	0.53
HS conduction Loss	0.235	0.5
Qrr Loss	0.03	0.03
HS gate drive Loss	0.25	0.1
LS conduction Loss	0.235	0.235
LS diode loss	0.03	0.06
Calculated Loss (W)		
Buck MOSFET Total Loss	1.53	2.03
Boost MOSFET Total Loss	0.54	0.62
Actual Loss (W)		
Buck MOSFET Total Loss	1.552	2.106
Boost MOSFET Total Loss	0.460	0.600

Table 2. MOSFET Loss Breakdown

I_{OUT} (A)	T_C Degree (C)			
	AONP36336		AOE6936	
	BuckFET	BoostFET	BuckFET	BoostFET
2	35.3	31.6	44.1	36.4
4	41	33.7	51.6	41
6	49	38.4	62.2	47.4
8	58.5	44	76.6	57.8
10	72	53.4	94.6	71.6

Table 3. T_C Comparison between AONP36336 and AOE6936 at VIN=20V/VOUT=13.2V

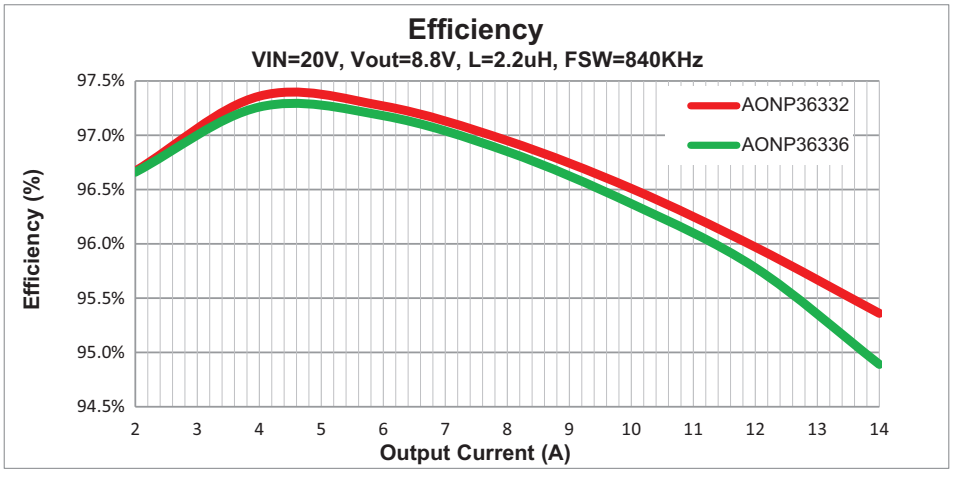

Figure 8. VIN=20V/VOUT=8.8V Efficiency Comparison Curve

I_{OUT} (A)	Power Loss (W)			
	AONP36336		AONP36332	
	BuckFET	BoostFET	BuckFET	BoostFET
2	0.52	0.016	0.53	0.014
4	0.7	0.068	0.7	0.06
6	0.92	0.16	0.95	0.132
8	1.22	0.288	1.26	57.8
10	1.63	0.46	1.65	0.4
12	2.16	0.696	2.15	0.6
14	3.12	1.023	2.77	0.841

Table 4. MOSFET Loss Comparison