dV/dt Ratings for Low Voltage and High Voltage Power MOSFET

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1. Abstract

To better understand and utilize AOS power MOSFETs, it is important to understand the design and ratings. Voltage ramp and diode recovery related dV/dt and avalanche breakdown (UIS) are explained and the inter-relationship of these three ratings are discussed in this article.

2. Introduction

dV/dt rating is an important parameter for the ruggedness of power MOSFET. It is usually a parameter shown in high voltage Power MOSFET (BVdss ≥ 500V) datasheets, but doesn't appear in most low voltage power MOSFET (BVdss ≤ 100V) datasheets including all low voltage datasheets made by AOS.

Both dV/dt (including voltage ramp type and diode recovery type) and UIS (Unclamped Inductive Switching) can cause MOSFET failure. In each of these situations, the device failure is caused by turn-on of the parasitic bipolar inherent in the MOSFET structure. For high voltage MOSFETs, the epitaxial region is much thicker than for low voltage MOSFETs, to allow it to support a higher off-state voltage. This region is conductivity modulated with electrons and holes when the body diode conducts, and there is more stored charge that needs to be removed during diode recovery in the high voltage MOSFET.

Therefore, in high voltage MOSFETs, diode recovery dV/dt may be accompanied by much higher current density. This creates the possibility of MOSFET failure, and is the reason for the dV/dt ratings in the datasheet. All AOS high voltage MOSFETs are 100% tested for UIS (avalanche current). This stresses the bipolar parasitic transistor in the same manner, and so a UIS test could also ensure that the device is able to withstand high dV/dt. However, the UIS current used in the high voltage MOSFET for 100% final testing is commonly lower than the current accompanying the dV/dt rating, because the UIS rating is linked to the forward current rating Id of the device. So, a separate dV/dt rating on the datasheet is a meaningful guarantee. On the other hand, for most low voltage MOSFETs, UIS is tested at a much higher current density so that it guarantees safe operation under all practical dV/dt conditions that can be reached in real applications. In other words, dV/dt ratings add no benefit to the datasheet.

2.1 Bipolar Turn-on:

The Power MOSFET structure contains an inherent parasitic N-P-N bipolar transistor formed between the two internal junctions. The turn-on of the bipolar transistor is suppressed by short-circuiting the junction between the N^+ source and P- base regions as shown in the cross section in Figure 1. In spite of this, The Emitter-base junction of the parasitic bipolar transistor can be turned on at location A because of the finite resistance R_{PB} of the P-base region.

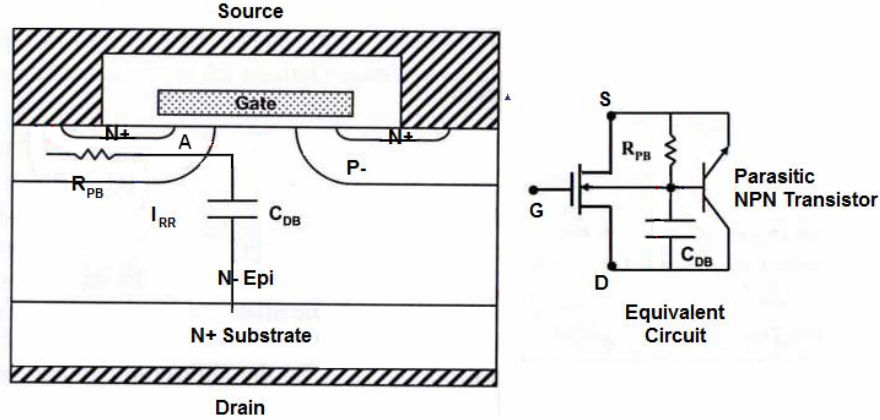

Figure 1: Cross section of power MOSFET and its Parasitic Transistor

In the presence of a high dV/dt at the drain terminal, during diode reverse recovery or during UIS, the P-base/N-drift (Epi) junction collects current which then flows into the contact via the P-base region. The voltage drop across the resistance R_{PB} forward biases the junction between the N^+ source region and the P-base region. If the voltage across this junction at point A exceeds the built-in potential, the parasitic bipolar transistor turns on. Under these conditions, the blocking voltage capability of the power MOSFET structure is degraded from BV_{CB0} the lower BV_{CE0}. Current filaments into the weak cell where the bipolar first turns on, leading to device destruction.

2.2 Voltage ramp type dV/dt vs. diode reverse recovery type dV/dt:

Voltage ramp type dV/dt:

When the MOSFET is off (gate-source shorted) and no current flow through its body diode, a voltage step with certain dV/dt is applied across Drain and Source. The result is a displacement current flow through the drain-base capacitance (C_{DB}), which can turn on the bipolar to result MOSFET failure.

$$i_D = C_{DB} \frac{dV}{dt}$$

The Diode reverse recovery type of dV/dt:

During diode reverse recovery, the MOSFET is off, the Vds voltage will ramp up at a certain dV/dt, but on top of displacement current i_D, at the same time diode reverse recovery current i_{RR} is flowing to remove the store the charge in the epi region. i_{RR} is not generated by dV/dt but accompanies it. The Diode Recovery Test Circuit & Waveforms are shown in Figure 2. The displacement current path and Body diode reverse recovery current path within the power MOSFET structure is shown in Figure 3.

$$i_{total} = i_D + i_{RR}$$

The peak of i_{total} is called i_{RM} .

Because it is the current flow into the contact to the P-base region that causes bipolar turn-on, we can easily draw a conclusion that for given value of dV/dt measured, diode reverse recovery type dV/dt accompanied with higher current density is more likely to fail a MOSFET by turning on its parasitic bipolar. That is to say, if a datasheet specifies a number for diode reverse recovery dV/dt, the value of the voltage ramp type of dV/dt is guaranteed.

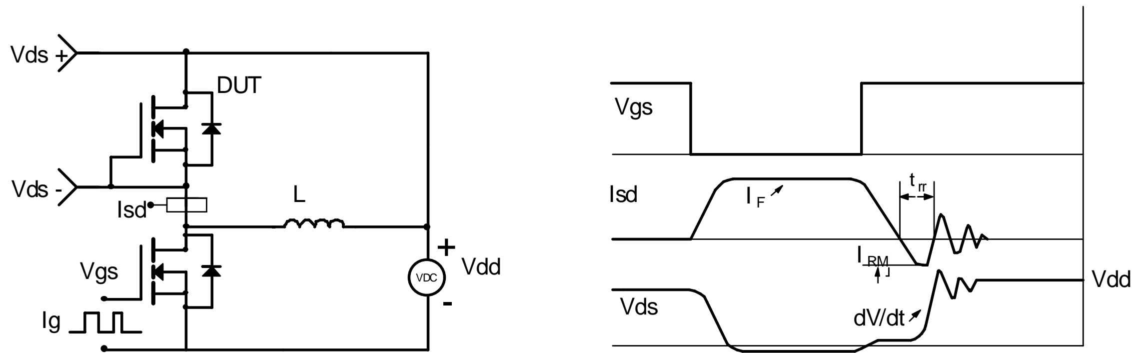

Figure 2: Diode Recovery Test Circuit & Waveforms

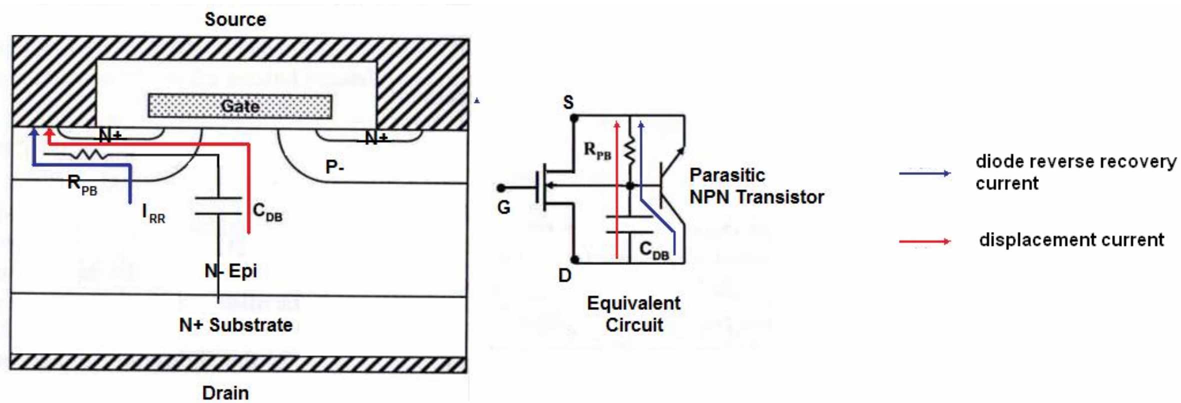

Figure 3: Displacement current path and Body diode reverse recovery current path within the power MOSFET structure

2.3 UIS vs. dV/dt:

When a voltage is applied to the power MOSFET well above its Vds rating, a critical electric field is reached at the p-base/n-epi junction. At this point, a large number of charge carriers are generated by a process of impact ionization. This current flows through the p-base region – the base of the parasitic bipolar. The current flow path is the same as that seen in diode recovery dV/dt tests, as depicted in Figure 4 below. When the voltage drop is sufficient to forward bias the parasitic bipolar junction transistor, it will turn on with potentially catastrophic results, as control of the switch is lost. Clearly, this failure mode is similar to dV/dt type of failure, and the root cause is high current flow through R_{PB} causing "Bipolar turn-on".

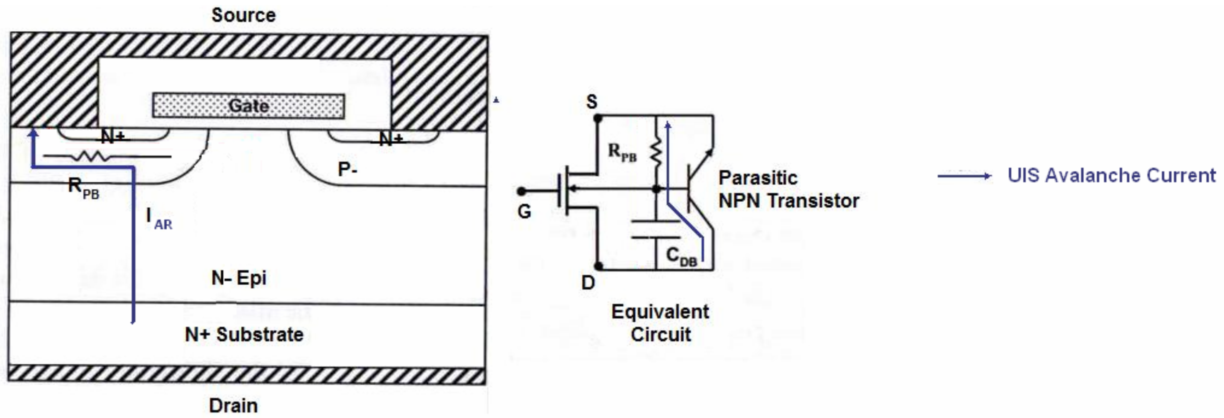

Figure 4: UIS avalanche current path within the power MOSFET structure

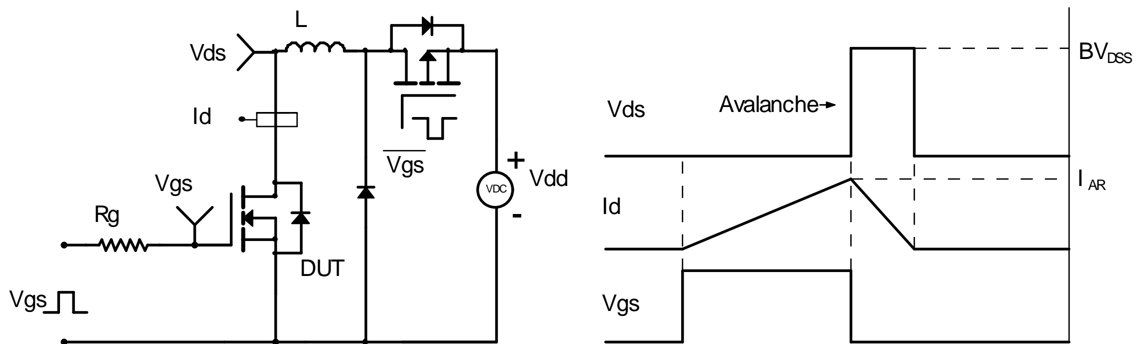

Figure 5: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

3. Real case study of diode recovery dV/dt:

From the background introduction above, we understand the inter-relationship between ramped dV/dt, diode recovery dV/dt and UIS avalanche. They all fail the MOSFET by "Bipolar turn-on" and root cause is the current flowing though R_{PB}. Now we return to the question raised at the beginning: Why is a dV/dt rating is not needed in low voltage Power MOSFET datasheets. The reasons will be demonstrated by comparing a 30V trench MOSFET and a high voltage 600V N-channel planar MOSFET as examples.

3.1 600V planar MOSFET:

600V planar MOSFET is popular for applications such as flyback converter, bridges and so on. Let's use AOT1N60 as an example. In the datasheet, the UIS current rating i_{AR} is 1.3A, Diode recovery dV/dt rating is 5V/ns.

Avalanche Current [C]	I_{AR}	1.0	A
Repetitive avalanche energy [C]	E_{AR}	15	mJ
Single pulsed avalanche energy [G]	E_{AS}	30	mJ
Peak diode recovery dv/dt	dv/dt	5	V/ns

Table 1: AOT1N60 datasheet ratings for UIS and dV/Dt

We can perform a simulation where the peak diode recovery current is made equal to UIS peak current I_{RM}=I_{AR}=1.3A. In this test, the dI/dt is adjusted during the diode recovery test such that I_{RM}=1.3A, as shown in Figure 6. A dI/dt of just 10A/us will produce this I_{RM}. The V_{SD} waveform shows the dV/dt associated with this stress is only 1V/ns. Clearly, and much higher diode dI/dt is needed to produce the 5V/ns dV/dt shown in the datasheet. Such a waveform is shown in Figure 7. It is clear from this waveform, that the dV/dt is 7.7V/ns and the I_{RM}=4A, which is much greater the UIS current rating. Therefore, the UIS test cannot guarantee the 5V/ns rating – and a separate rating must be provided.

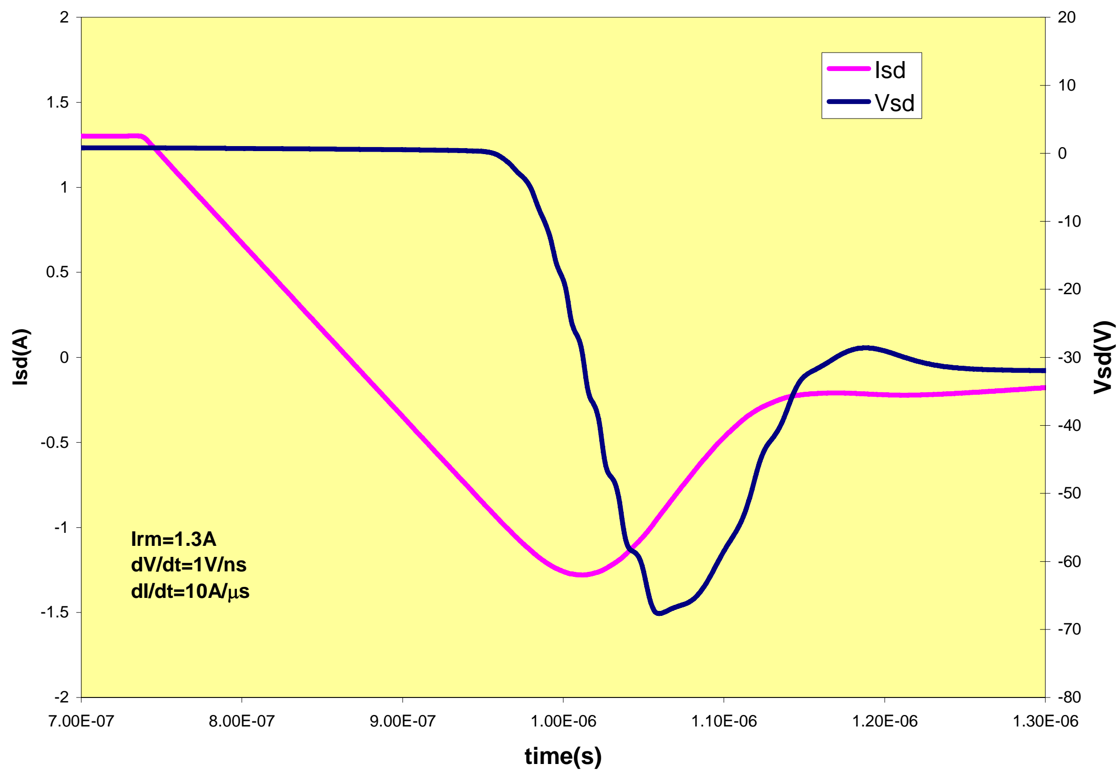

Figure 6: AOT1N60 diode reverse recovery waveforms with I_{RM}=1.3A

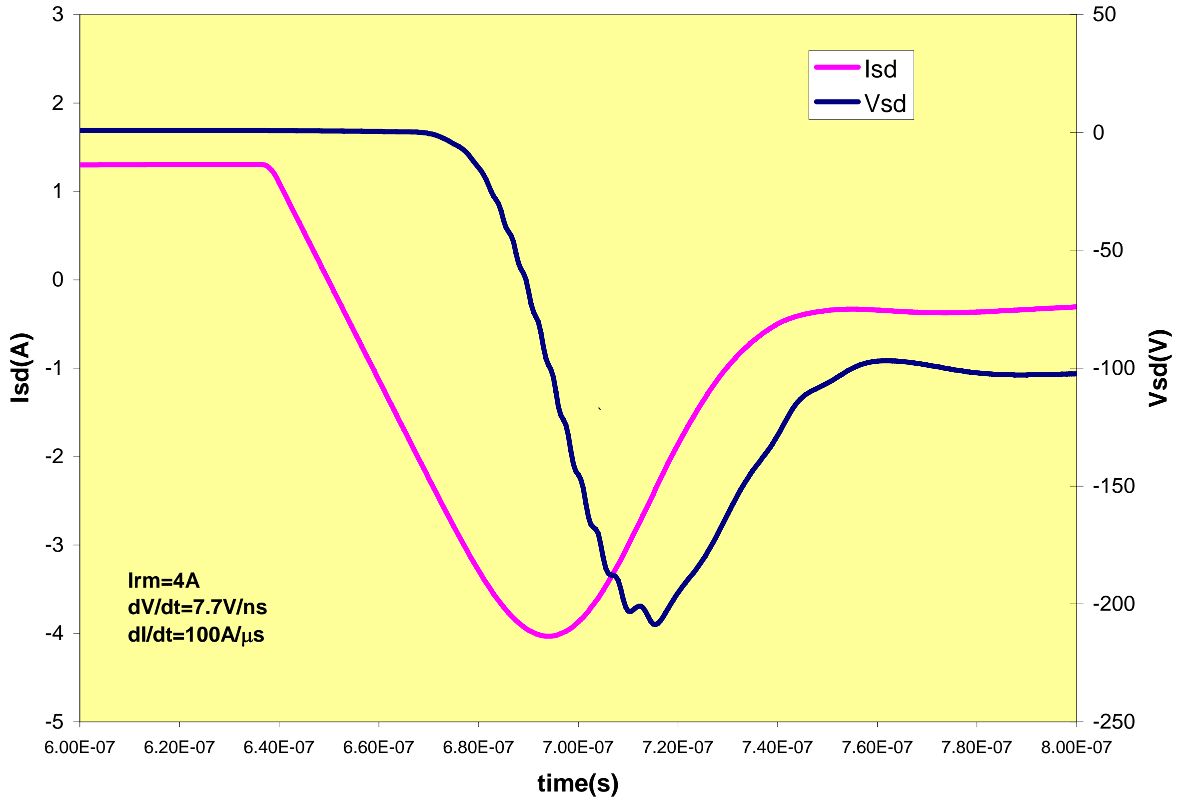

Figure 7: AOT1N60 diode reverse recovery waveforms with I_{RM}=4A

3.2 30V trench MOSFET:

30V trench MOSFETs are popular in applications such as DC to DC converters, load switches and so on. Let's use AO4468 as an example.

In the datasheet, the UIS current rating i_{AR} is 16A, and there is no diode recovery dV/dt rating.

Avalanche Current [B]	I_{AR}	16	A
Repetitive avalanche energy L=0.3mH [B]	E_{AR}	38	mJ

Table 2: AO4468 datasheet ratings for UIS

We use a diode recovery test condition for low voltage MOSFET with di/dt=500A/us. Waveforms are shown in Figure 8 for operation under these conditions. We get an I_{RM}=2.3A associated with a dV/dt=6V/ns. Due to thinner epi and much less stored charge compared to the 600V FET, the I_{RM} values seen by LV MOSFETs are clearly much less than UIS test current I_{AR} which is 16A.

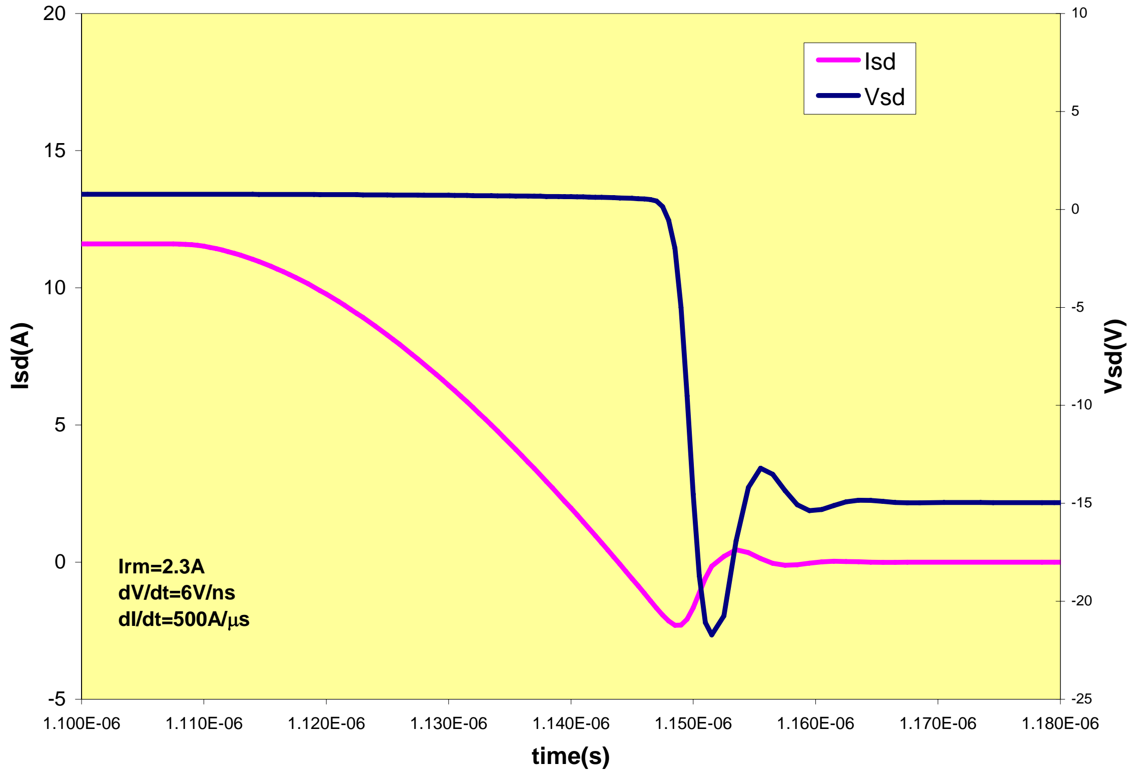

Figure 8: AO4468 diode reverse recovery waveforms with datasheet conditions
I_{RM}=2.3A

If the diode recovery test was performed at an extreme di/dt=8000A/us, we could produce an I_{RM}=15A and a dV/dt =40V/ns as shown in Figure 9. This dI/dt is impossible in practice, and so this dV/dt cannot be occur on low voltage FETs in practice. The UIS test commonly done on these FETs in fact guarantees this level of dV/dt immunity. Clearly, once the UIS rating is provided in the low voltage FET, the dV/dt rating is unnecessary.

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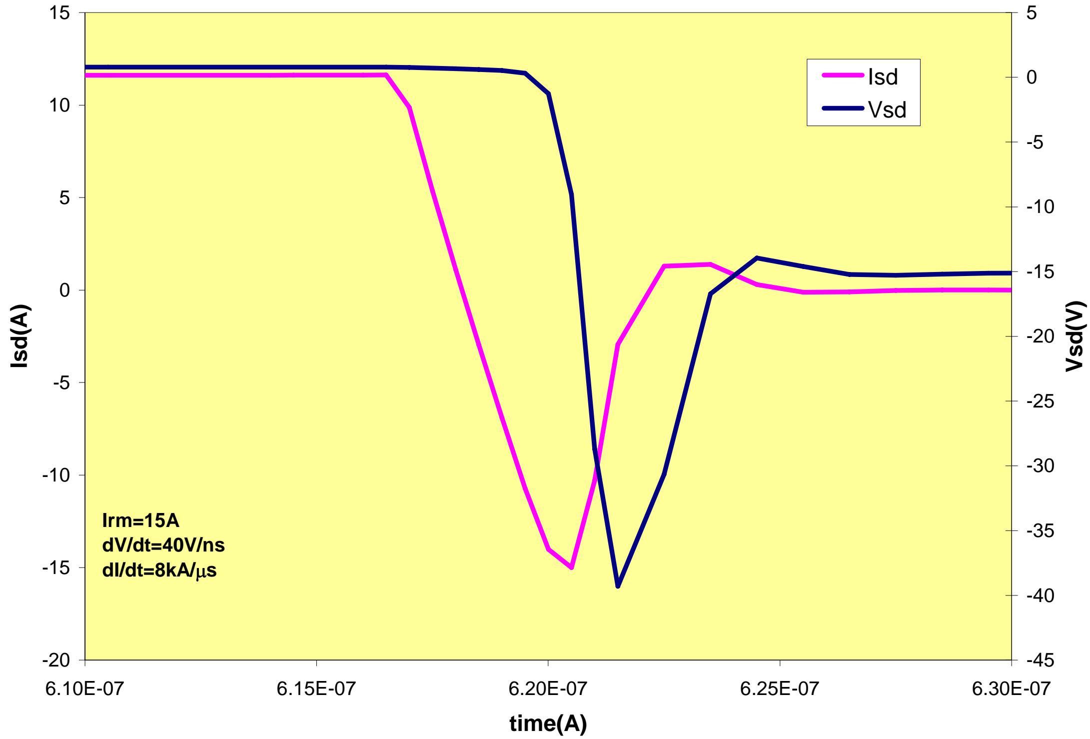

Figure 9: AO4468 diode reverse recovery waveforms with I_{RM}=15A

4. Conclusion

For low voltage MOSFET devices, our UIS rating can meaningfully guarantee >40V/ns (40kV/us) diode recovery dV/dt immunity. Any lower dV/dt rating shown in the datasheet is redundant and unnecessary.

For high voltage MOSFET devices, the lower current UIS rating can not guarantee sufficient diode recovery dV/dt immunity, so an additional dV/dt rating is usually needed to characterize MOSFET ruggedness.

5. References

- Stoltenburg, R.R. "Boundary of Power MOS UIS Avalanche Current Capability" IEEE Applied Power Electronics Conference Proceedings 359-64: (Mar 1989).
- Baliga, B. Jayant "Fundamentals of Power Semiconductor Devices" Springer, 2008

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6. Revision History

Date	Revision	Changes
3/26/2009	1	Initial release

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