

# BUCK Converter Control Cookbook

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A Buck converter consists of the power stage and feedback control circuit. The power stage includes power switch and output filter. It converts a higher input voltage to a lower output voltage. The feedback control circuit regulates the output voltage by modulating the power switch duty cycle.

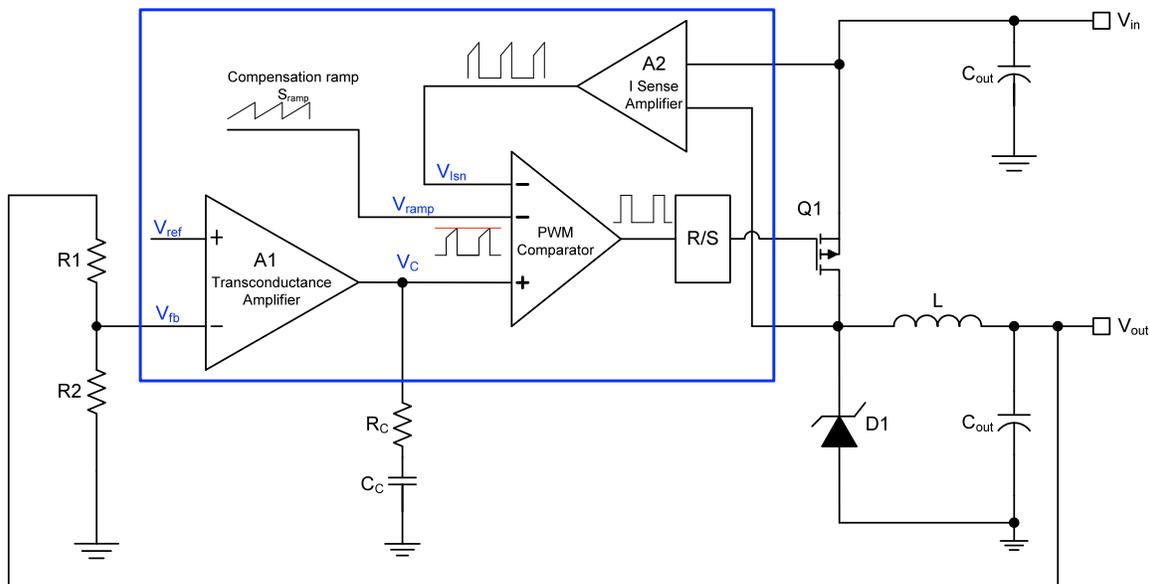
Stable operation of switching mode DC/DC converter requires an adequate loop gain and phase margin in frequency domain. This application note provides an overview of the control circuit small-signal modeling, power stage modeling and feedback compensation design.

## 1. Buck Power Stage Small-Signal Analysis

In this application note, the AOZ101X is used as an example to explain Peak Current Mode Control (PCMC) and its small signal analysis. PCMC makes the converter power stage resemble a voltage-controlled-current-source. It simplifies the feedback compensation design since the complex pole pair associated with output LC filter are removed from the loop compensation equation. PCMC also provides other benefits such as voltage feedback forward and inherent cycle-by-cycle current limit.

### 1.1 Simplified buck converter equivalent circuit

Figure 1 below shows a simplified schematic of buck converter and modulator with Peak-Current-Mode-Control scheme.



**Figure 1: PCMC buck converter block diagram**

The output voltage is fed back to error amplifier A1 and is compared against the internal reference voltage,  $V_{ref}$ , which is 0.8V for the AOZ101x. Any slight difference between the feedback voltage and reference voltage results in large swing in the error amplifier output voltage. The output voltage of error amplifier A1 is also called control voltage, which actually controls the switch current level and the output voltage.

The inductor ripple current is translated into a ramp voltage signal by the current sense amplifier A2, which amplifies the voltage drop across the high side switch. This ramp represents the inductor current plus compensation ramp signal together and is fed back to the PWM comparator, forming an inner current control loop.

At the beginning of each switching period, control voltage is higher than the current signal voltage. The output of the PWM comparator is high and the high-side switch is on. The input voltage applies to the output filter inductor,  $L$ . The inductor current increases at a constant slew rate decided by input voltage, output voltage, inductance and switching frequency. The inductor current ramp up slew rate is:

$$\frac{\Delta I_L}{\Delta t_{on}} = \frac{V_{in} - V_O}{L}$$

$\Delta I_L$  is the peak to peak inductor current ripple.  $\Delta t_{on}$  is the high-side switch turn on time.

The current signal voltage ramps up as the switch current increasing. When the current signal voltage,  $V_{Isn}$ , equals to the control voltage  $V_C$ , the PWM comparator output changes from high to low. The high-side switch turns off and inductor current starts to decay. The inductor current ramp down slew rate is:

$$\frac{\Delta I_L}{\Delta t_{off}} = \frac{V_O}{L}$$

$\Delta t_{off}$  is the high side switch turn off time.

As explained above, control voltage signal,  $V_C$ , is compared against current sense signal and determines the peak inductor current level. Higher  $V_C$  regulates peak inductor current to higher level. If  $V_C$  is zero, inductor current is regulated to zero.

If inductor is not saturated, there is a constant difference between average inductor current and peak inductor current.

$$I_{L\_peak} = I_{L\_average} + 0.5 \cdot \Delta I_L$$

Where  $I_{L\_peak}$  is the peak inductor current;  $I_{L\_average}$  is the average inductor current, it is also the output current.

$$\Delta I_L = \frac{V_O}{V_{in}} \cdot \frac{(V_{in} - V_O)}{L} \cdot T$$

The control voltage,  $V_C$ , controls peak inductor current. If the inductor ripple current  $\Delta I_L$  is small,  $V_C$  also controls average inductor current. So the output filter inductor and PWM comparator together can be simplified to a Voltage-Controlled-Current-Source. The simplified buck converter power stage circuit is shown in Figure 2 below.

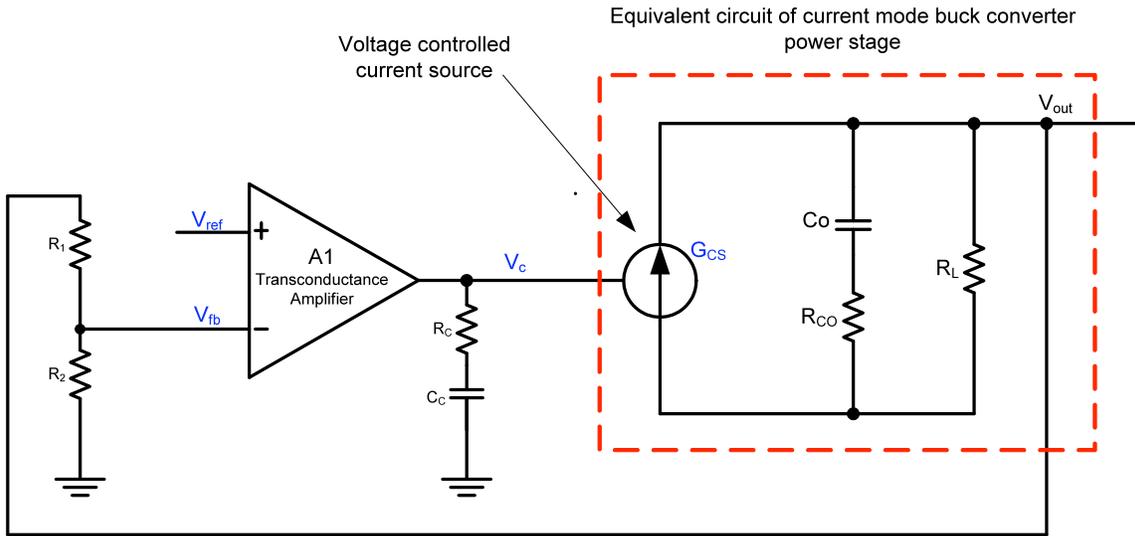


Figure 2: Equivalent circuit of buck converter with CMC

The current sense amplifier, A2, has a transconductance  $G_{CS}$ , which is defined as:

$$G_{CS} = \frac{I_L}{V_{Isn}}$$

Assuming the inductance is large enough and ripple can be ignored, the inductor current is same as the load current. Since the control voltage regulates the inductor current level, the  $V_{Isn}$  in equation above can be replaced by control voltage  $V_C$ . Then control voltage can be calculated using inductor current, output voltage and current sense circuit transconductance in the equation below.

$$V_C = \frac{I_L}{G_{CS}} = \frac{V_O}{R_L} \cdot \frac{1}{G_{CS}}$$

## 1.2 Power stage open loop transfer function

The power stage open loop transfer function is defined as the transfer function from control voltage to output voltage.

$$G_{open}(s) = \frac{V_O(s)}{V_C(s)}$$

From Figure 2 above,  $V_O$  can be calculated easily by multiplying output current and output impedance as below.

$$V_O(s) = i_L(s) \times \frac{R_L \times \left( \frac{1}{s \cdot C_o} + R_{CO} \right)}{R_L + \frac{1}{s \cdot C_o} + R_{CO}}$$

$C_o$  is the output capacitor.  $R_{CO}$  is the output capacitor ESR.  $R_L$  is the load resistance.

Combine the two equations above to get power stage open loop transfer function.

$$G_{open}(s) = \frac{V_O(s)}{V_C(s)} = G_{CS} \cdot R_L \cdot \frac{1 + s \cdot C_O \cdot R_{CO}}{s \cdot C_O \cdot (R_L + R_{CO}) + 1}$$

since  $R_L \gg ESR$ ,

$$G_{open}(s) = \frac{V_O(s)}{V_C(s)} = G_{CS} \cdot R_L \cdot \frac{1 + s \cdot C_O \cdot R_{CO}}{s \cdot C_O \cdot R_L + 1}$$

Now it can be found that power stage open loop transfer function has one pole and one zero.

The pole is called dominant pole or load pole:  $f_{p1} = \frac{1}{2 \cdot \pi \cdot C_O \cdot R_L}$

The zero is called ESR zero:  $f_{z1} = \frac{1}{2 \cdot \pi \cdot C_O \cdot R_{CO}}$

The power stage transfer function has DC gain:  $G_{DC\_open} = G_{CS} \cdot R_L$

Figure 3 below shows the bode plot of power stage open loop transfer function. The dash line and solid line show the bode plots when converter is under light load and heavy load respectively. As load increases, load resistance  $R_L$  decreases. The load pole moves from low frequency to high frequency. Also, the open loop transfer function DC gain is reduced as load current increases.

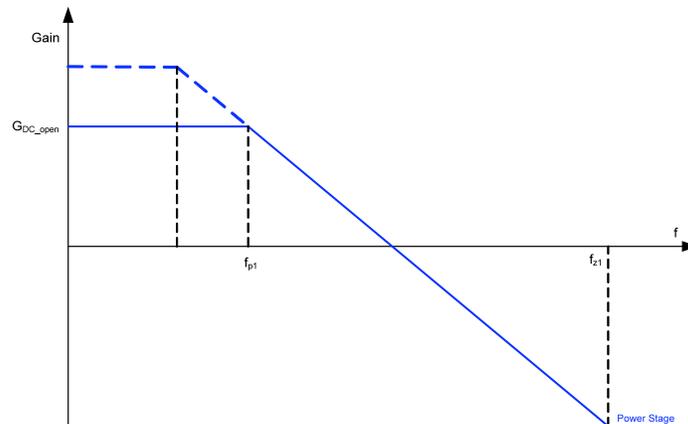


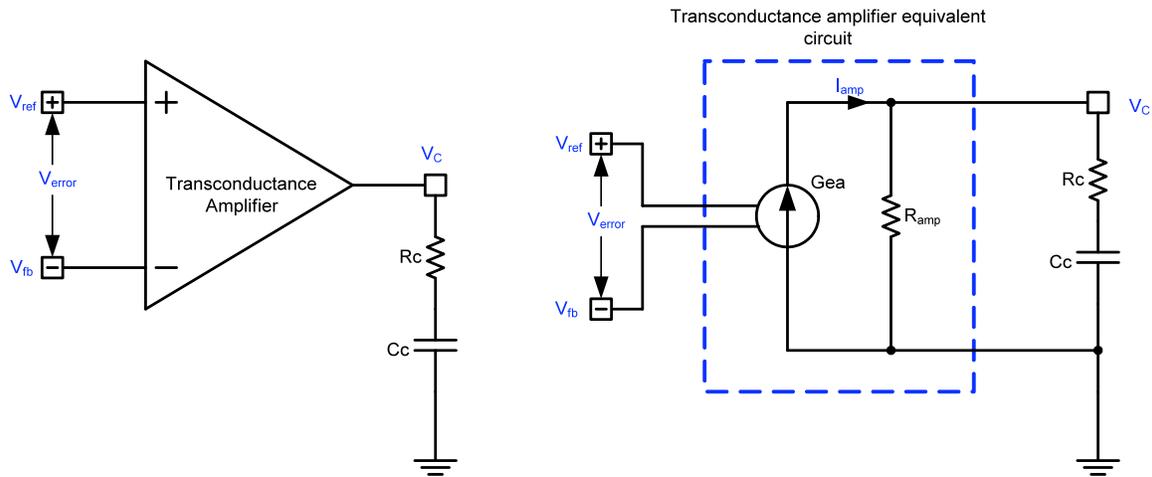
Figure 3: Bode plot of buck converter power stage

## 2. Compensation Circuit Small Signal Analysis and Feedback Design

AOZ101x buck regulator IC uses a high bandwidth transconductance amplifier as error amplifier A1. A transconductance amplifier is actually a Voltage-Controlled-Current-Source. It converts any error voltage at its input pins to a current flowing out of its output pin. The amplifier factor,  $G_{ea}$ , is called transconductance gain. It is defined as:

$$G_{ea} = \frac{I_{amp}}{V_{error}}$$

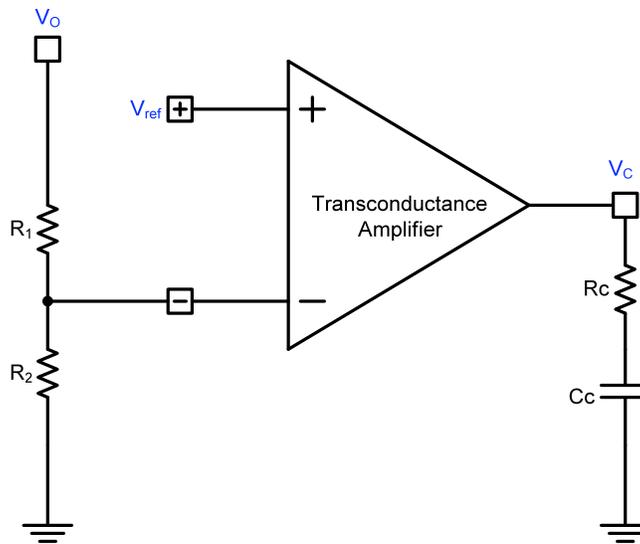
A transconductance amplifier block diagram and equivalent circuit are shown in Figure 4 below.



**Figure 4: Transconductance amplifier and equivalent circuit**

In Figure 4 above,  $R_{amp}$  represents the output impedance of transconductance amplifier. An ideal transconductance has infinite output impedance,  $R_{amp}$ . For the transconductance amplifier in AOZ101x series IC, the output impedance is above 2.5M $\Omega$ .  $R_c$  and  $C_c$  represent the external compensation RC network components.

From AC point of view, the non-inverting pin of amplifier is connected to a DC reference voltage, which is a virtual AC ground. Figure 5 below shows the simplified compensation circuit, which is part of the buck converter block diagram shown in Figure 2.



**Figure 5: Compensation circuit diagram**

The transfer function of the compensation circuit in Figure 5 is derived below.

$$G_{comp}(s) = \frac{V_C(s)}{V_O(s)} = \frac{R_2}{R_1 + R_2} \cdot G_{ea} \cdot R_{amp} \cdot \frac{R_C \cdot C_C \cdot s + 1}{(R_{amp} + R_C) \cdot C_C \cdot s + 1}$$

Where  $\frac{R_2}{R_1 + R_2}$  is the voltage feedback divider gain, and  $\frac{R_2}{R_1 + R_2} = \frac{V_{ref}}{V_O}$

Since  $R_{amp} \gg R_C$ . The equation above can be simplified as below.

$$G_{comp}(s) = \frac{V_{ref}}{V_O} \cdot G_{ea} \cdot \frac{R_C \cdot C_C \cdot s + 1}{1} \cdot \frac{R_{amp}}{R_{amp} \cdot C_C \cdot s + 1} \dots\dots\dots(2.1)$$

From the equation above, it can be seen that the compensator circuit has one pole and one zero.

The compensation pole is:  $f_{p2} = \frac{1}{2 \cdot \pi \cdot R_{amp} \cdot C_L}$

Since the Ramp is fairly large, this is located at very low frequency range.

The compensation zero is also called ESR zero:  $f_{z2} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C}$

Another parameter of transconductance amplifier is transconductance amplifier voltage gain,  $G_{vea}$ . It is defined as the transconductance amplifier output voltage over input voltage when amplifier output is open. It is easy to understand that:

$$G_{vea} = \frac{V_O}{V_{in}} = \frac{I_O \cdot R_{amp}}{V_{in}}$$

So  $R_{amp} = \frac{G_{vea}}{G_{ea}}$

The compensation pole can also be expressed by:  $f_{p2} = \frac{G_{ea}}{2 \cdot \pi \cdot G_{vea} \cdot C_C}$

$f_{p2}$  is a very low frequency pole because  $R_{amp}$  is very large. The low frequency pole  $f_{p2}$  can be approximated by an integrator.

$$\frac{R_{amp}}{R_{amp} \cdot C_C \cdot s + 1} \approx \frac{1}{C_C \cdot s}$$

The example below shows how close this approximation is. For example,  $R_{amp}=2.5M\Omega$ ,  $C_C=1000pF$ , Figure 6 below

compares the bode plot of transfer function of  $T_1(s) = \frac{R_{amp}}{R_{amp} \cdot C_C \cdot s + 1}$  and  $T_2(s) = \frac{1}{C_C \cdot s}$ .

As shown in Figure 6, the difference between the two transfer function only exists at very low frequency range.

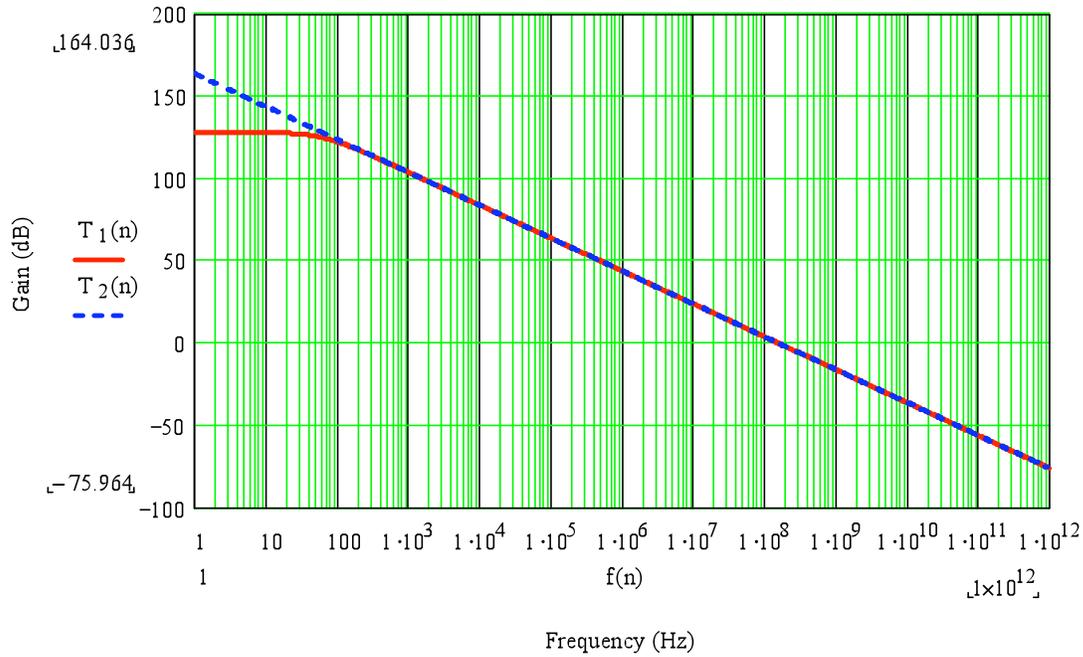


Figure 6: Bode plot of  $T_1(s)$  and  $T_2(s)$

The larger the  $R_{amp}$  is, the less is the difference between  $T_1(s)$  and  $T_2(s)$ . Finally, the transfer function of the compensation circuit in Figure 5 can be approximated to equation below.

$$G_{comp}(s) = G_{ea} \cdot \frac{R_C \cdot C_C \cdot s + 1}{C_C \cdot s} \cdot \frac{V_{ref}}{V_O}$$

The bode plot of the transfer function above is shown in Figure 7 below.

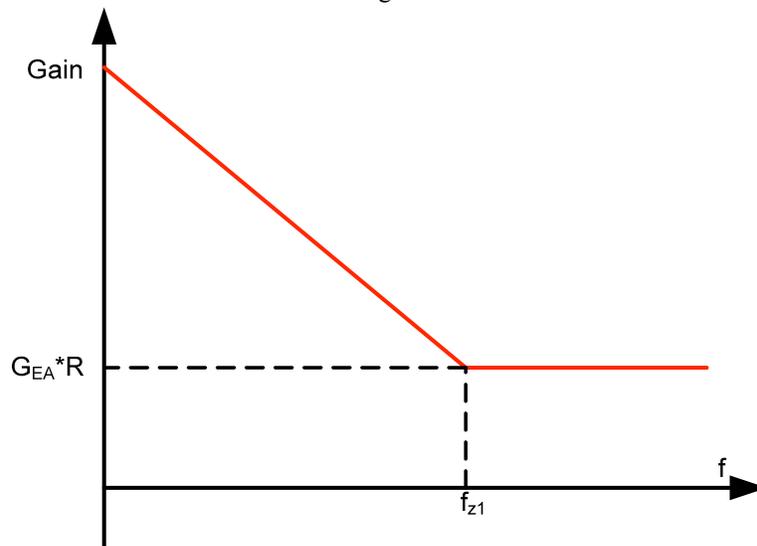


Figure 7: Bode plot of simplified compensation circuit

The compensation circuit has one zero and one integrator. The zero is:  $f_{z2} = \frac{1}{2 \cdot \pi \cdot C_C \cdot R_C}$

At frequency  $f_{z2}$  and above, the compensator transfer function gain is:  $\frac{V_{ref}}{V_O} \cdot G_{ea} \cdot R_C$

### 3. Close Loop Transfer Function

AOZ101x converter employs a very simple one integrator (or one pole) and one zero compensation network. The integrator helps to increase close loop gain at low frequency range. The zero is placed where the power stage dominant pole is at heavy load. This zero gives a 90 degree phase boost around the close loop gains cross over frequency to ensure an adequate close loop phase margin.

So the total close loop transfer function is:

$$G_{close}(s) = G_{open}(s) \cdot G_{comp}(s)$$

$$G_{close}(s) = G_{CS} \cdot R_L \cdot \frac{1 + s \cdot C_O \cdot R_{CO}}{s \cdot C_O \cdot R_L + 1} \cdot \frac{V_{ref}}{V_O} \cdot G_{ea} \cdot \frac{R_C \cdot C_C \cdot s + 1}{C_C \cdot s}$$

At the frequency  $f_{P1}$  (or  $f_{z2}$ ), the close loop gain is:

$$G_{close\_loop\_fp1} = G_{CS} \cdot R_L \cdot \frac{V_{ref}}{V_O} \cdot G_{ea} \cdot R_C$$

If the desired close loop transfer function cross over frequency is  $f_{CC}$ . Based on mathematics and basic bode plot principle, there is:

$$\frac{f_{CC}}{f_{P1}} = G_{CS} \cdot R_L \cdot \frac{V_{ref}}{V_O} \cdot G_{ea} \cdot R_C$$

User can determine the desired close loop cross over frequency,  $f_{CC}$ , using the equation above. Most parameters in equation above are fixed for a buck converter except the compensation resistor  $R_C$ . To realize the desired close loop frequency response, the compensation resistor,  $R_C$ , can be calculated using equation below.

$$R_C = f_{CC} \cdot \frac{V_O}{V_{ref}} \cdot \frac{2 \cdot \pi \cdot C_O}{G_{CS} \cdot G_{ea}}$$

In the RC compensation network, the compensation resistor  $R_C$  determines the close loop cross over frequency when converter power stage is fixed. The compensation capacitor  $C_C$  determines the compensation zero. To ensure enough phase margin, the compensation zero should be placed at where the power stage dominate pole is under full load condition.

$$C_C = \frac{1}{2 \cdot \pi \cdot R_C \cdot f_{P1}} = \frac{R_L \cdot C_O}{R_C}$$

Figure 8 below illustrates the bode plot of power stage open loop transfer function, compensation circuit and close loop transfer function. It can be seen that feedback design process is actually to shape the bode plot of close loop transfer function to desired position.

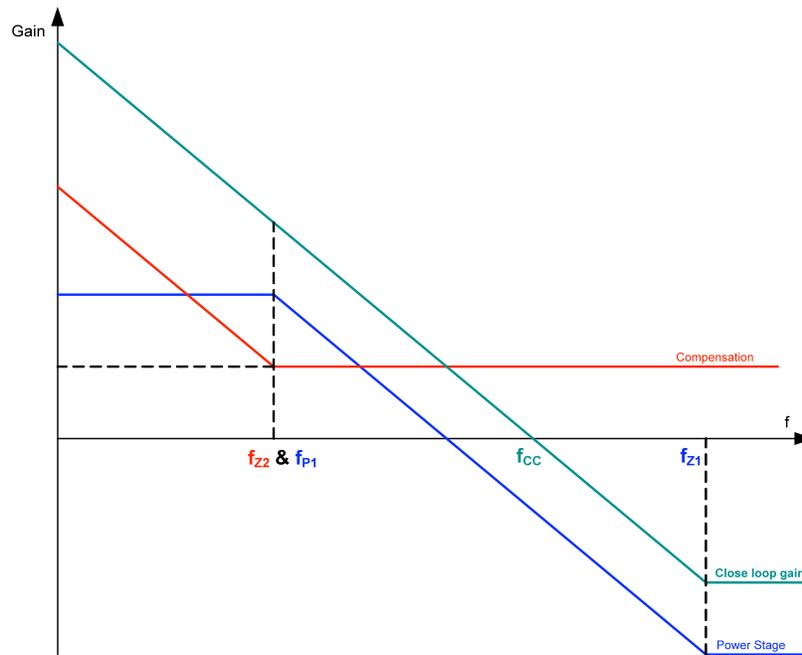


Figure 8. Close loop transfer function bode plot

## Appendix I: Bode Plots

In the design of a converter control system, it is necessary to work with frequency-dependent transfer function and bode plot. The bode plot is a method to display the complex value of circuit gain and phase. The gain magnitude in dB is plotted against log frequency. Phase angle is also plotted against same log frequency. Bode plot provides good visibility into the gain/phase characteristics of power supply control loop. The bode plot of control loop elements are simplified to straight lines. Calculation of bode plot is simplified to adding the gain and phase. The phase angle of the gain at any frequency depends on the rate change of gain magnitude vs. frequency. For a system like power converters, the system stability depends on phase margin, or its close loop gain slope.

The bode plots of some basic circuit elements used in this application note are reviewed below.

### 1. Integrator

Integrator,  $\frac{1}{s}$ , has gain slope of -20dB/decade. Its unity gain frequency is  $f=1$ . The phase shift is  $-90^\circ$ . A proportional integrator,  $\frac{k}{s}$ , also has slope of 20db/decade. But its unity gain frequency is  $f=k$ . Their bode plots are shown in Figure 1 below.

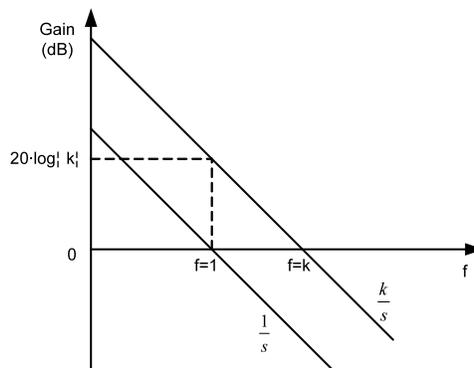


Figure 1: Bode plot of integrator

### 2. Single pole

Single pole,  $\frac{1}{a \cdot s + 1}$ , has flat gain slope at frequency lower than  $f_p=1/a$ . At frequency higher than  $f_p$ , its gain slope is -20dB/decade. Its unity gain frequency is  $f_p$ . Phase shift at  $f_p$  is  $-45^\circ$  and  $-90^\circ$  in total. A proportional single pole,  $\frac{k}{a \cdot s + 1}$ , has higher unity gain frequency at  $k \cdot f_p$ . Their bode plot are shown in Figure 2 below.

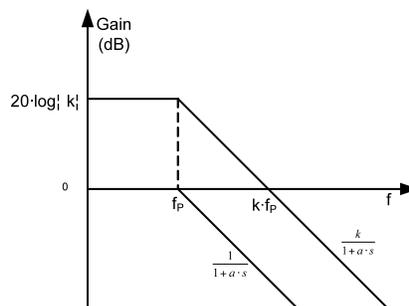
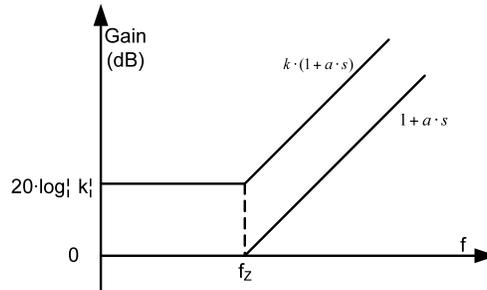


Figure 2: Bode plot of single pole

**3. Single zero**

Single zero,  $1 + a \cdot s$ , has flat gain slope at frequency lower than  $f_p=1/a$ . At frequency higher than  $f_p$ , its gain slope is 20dB/decade. Its unity gain frequency is  $f_z$ . Phase shift at  $f_z$  is  $45^\circ$  and  $90^\circ$  in total.



**Figure 3: Bode plot of single zero**