ESD Protection for Super Speed USB 3.0 Ports

John Ng, Senior Applications Engineer

Overview

USB 3.0 is an enhanced version of the USB 2.0, with up to 5Gbps data rate. USB 3.0 has 10 times the performance over USB 2.0. Legacy device continue to work when plugged into new host connector albeit at USB 2.0 speeds. USB 3.0 maintains this backward compatibility by adding an addition pairs of SuperSpeed differential data lines, SSRX+/- and SSTX+/- with the existing pair of USB 2.0 data line, D+ and D-. The SSRX and SSTX is the differential data line that we are focus in the PCB layout and ESD protection.

For USB 3.0 SuperSpeed following RF characteristics have to be met:

- The total budget for the parasitic capacitance @ Source/Load CRx is 1.1pF. (Including driver, receiver, and ESD devices…)
- Differential Impedance = 90Ω +/-7Ω between Source/Load.

A carefully designed PCB layout in combination with rugged ESD protection is vital for a robust operating system.

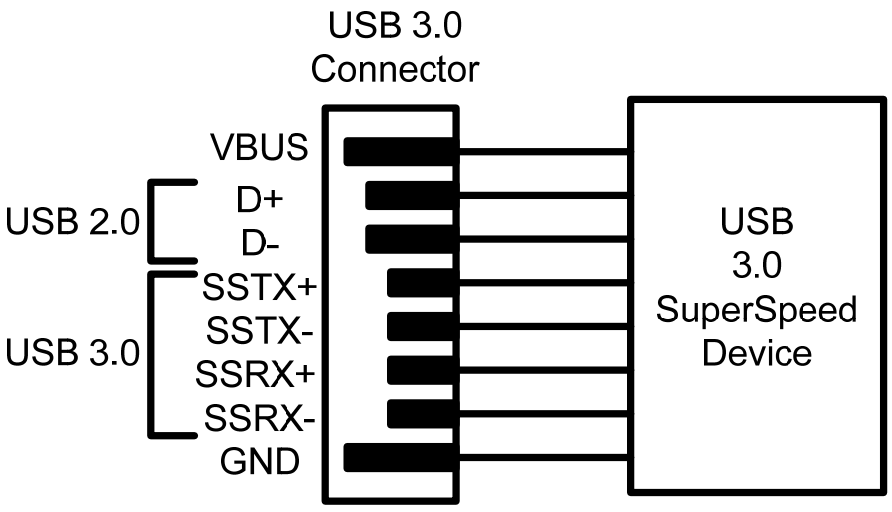

Figure 1.

ESD Protection

Great attention must be paid to the layout design details to minimize TDR impedance mismatch, crosstalk between SuperSpeed USB pairs and Crosstalk between SuperSpeed USB 3.0 and D+/- pairs of USB 2.0. The SuperSpeed differential characteristic impedance for the differential pair is recommended to be within 90Ω +/-7Ω. It should be measured with a TDR in a differential mode using a 200ps (10%-90%) rise time. It is important for the ESD protection device to have little influence on the data transmission and data integrity implemented on a straight forward PCB layout. By having a straight forward layout you can minimize the Source/Load impedance matching.

The AOZ8804 ultra small DFN-10 package 1mm X 2.2mm X 0.5mm can be use to protect two pairs of differential pair data lines. And the AOZ8802 DFN-6 package 1.6mm X 1.0mm X 0.5 can be use to protect the USB 2.0 D+ and D- data line. Figure 2. The AOZ8802/4 is used to meet the ESD immunity requirements of the IEC61000-4-2, level 4 +/-15kV air discharge, +/-8kV contact discharge.

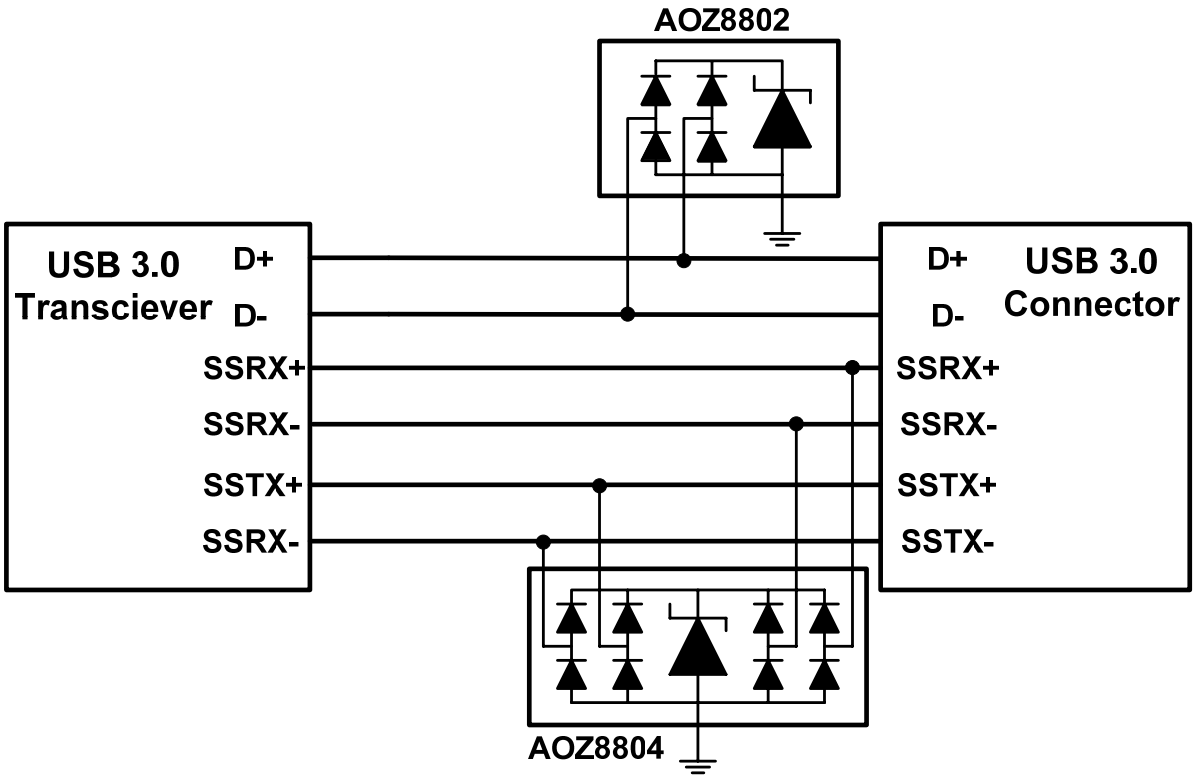

Figure 2.

In addition to the ultra small DFN-6 and the DFN-10 package the AOZ8802/4 is design with the ease of layout in mind. Figure 3 & 4 shows the AOZ8802/4 flow through layout design that would minimize layout errors associated impedance matching and cross talk.

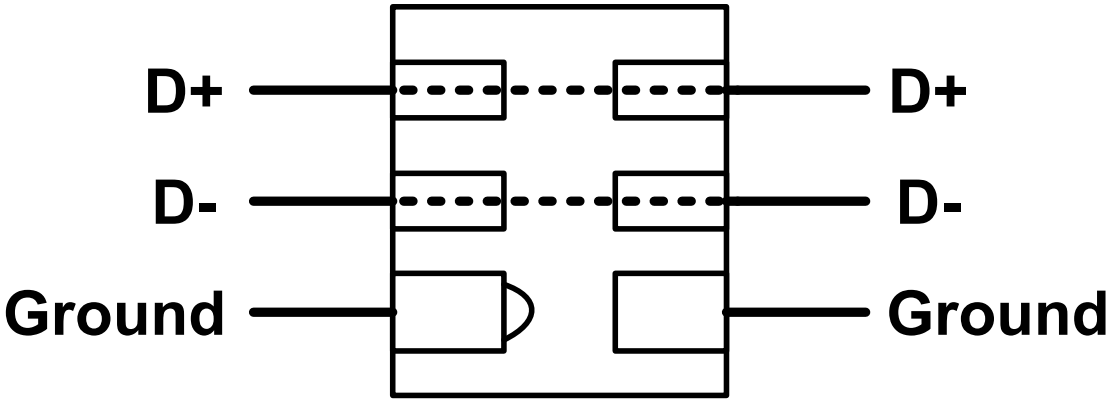

Figure 3. DFN-6

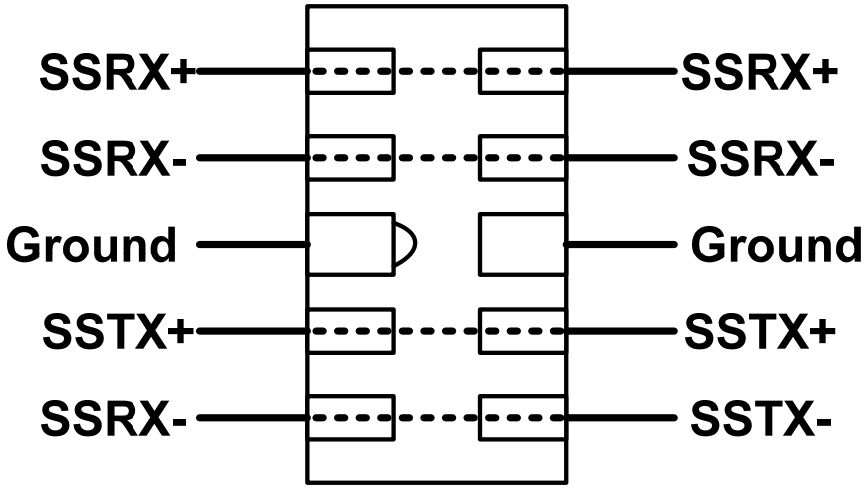

Figure 4. DFN-10

Based on the AOZ8802/4 DFN package design a very straight forward layout can be achieved. The AOZ8802/4 can be placed directly over the data line without any deviation from the 90Ω differential pair. To make the design perfect the added capacitance of the device will have to be compensated by the use of "Skinny Traces" The skinny traces is a narrow stripe line acting to lower the parasitic capacitance on the differential stripe line. The differential impedance of the USB 3.0 transmission line becomes well centered to 90Ω. The AOZ8802/4 does not have any influence on the data transmission and data integrity. A layout EM field simulator is recommended before fabrication to insure a perfect stripe line. Also, good general practice of placing the TVS device as close to the connector will further improve the performance.

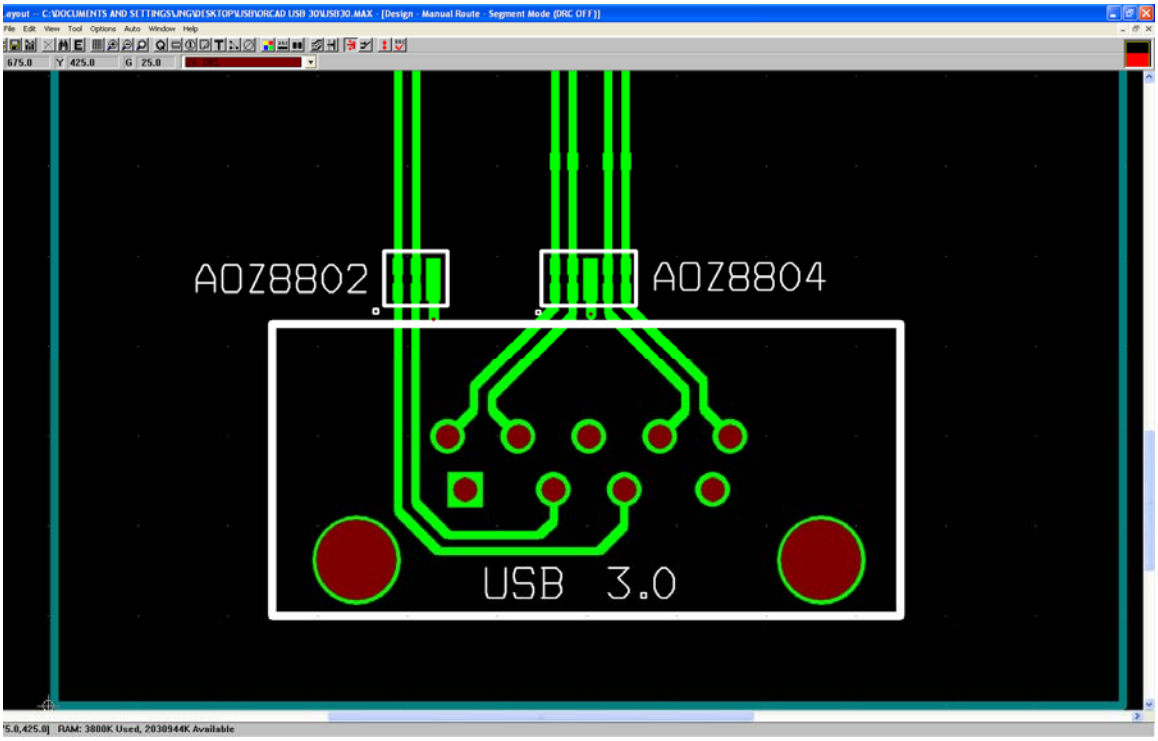

Figure 5. PCB Layout

Table 1. USB 3.0 Evaluation Board Specification

Number of Layers	4
Copper Trace Thickness	1.4 mils
Dielectric Constant	4.6
Overall Board Thickness	62 mils
Dielectric thickness between top and ground layer	10 mils

Summary

With careful layout and placement of the device, the AOZ8802/4 can protect the USB 2.0/3.0 data line effectively and safely. With the AOZ8802/4 ultra low capacitance channels in place the device is able to meet the USB 3.0 signal protocol and ESD immunity requirements of the IEC61000-4-2, level 4,+/-15kV air discharge, +/-8kV contact discharge

Figure 6. AOZ8802/4 Voltage Clamping Response Waveform at 8kV Contact Discharge. (10X attenuator on scope)