

## General Description

The AGD8136A / AGD8236A are 600V 6-channel gate driver ICs to control IGBTs and power MOS-transistors in 3-phase inverter systems. Due to specially designed common mode filter, it has an excellent ruggedness on transient voltage variation.



SOP-28L

(Body: 18 x 7.5 x 2.5 mm)



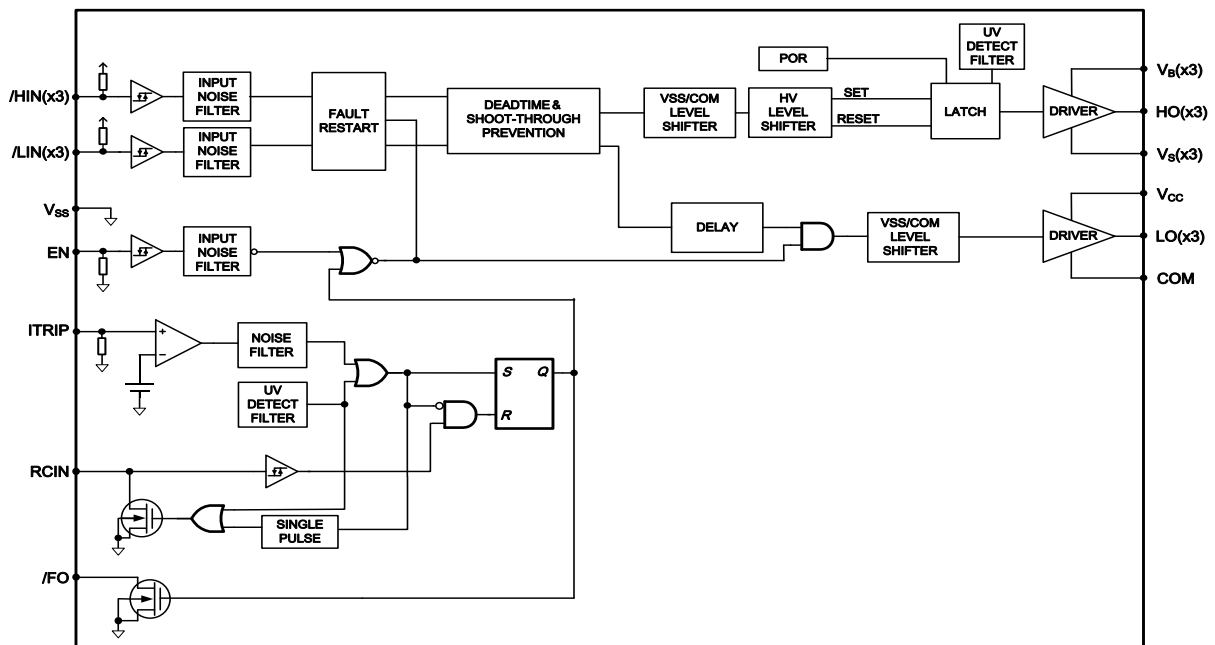
## Features

- Maximum blocking voltage +600V
- Output current: +200mA / -350mA (Typ.)
- Matched propagation delay for all channels
- Shoot-through (cross-conduction) protection
- Under-voltage lockout protection (UVLO)
- Over-current protection (OCP)
- Fault output corresponding to UV (Vcc supply) and OCP
- Shut-down of all channels during fault conditions
- Adjustable fault output duration time
- 3.3V / 5V CMOS and TTL input logic compatible
- Input logic: Schmitt trigger receiver circuit (Active Low)

## Applications

- 3-phase motor drives
- Home appliances
- IGBT and power MOS gate drivers for general purpose

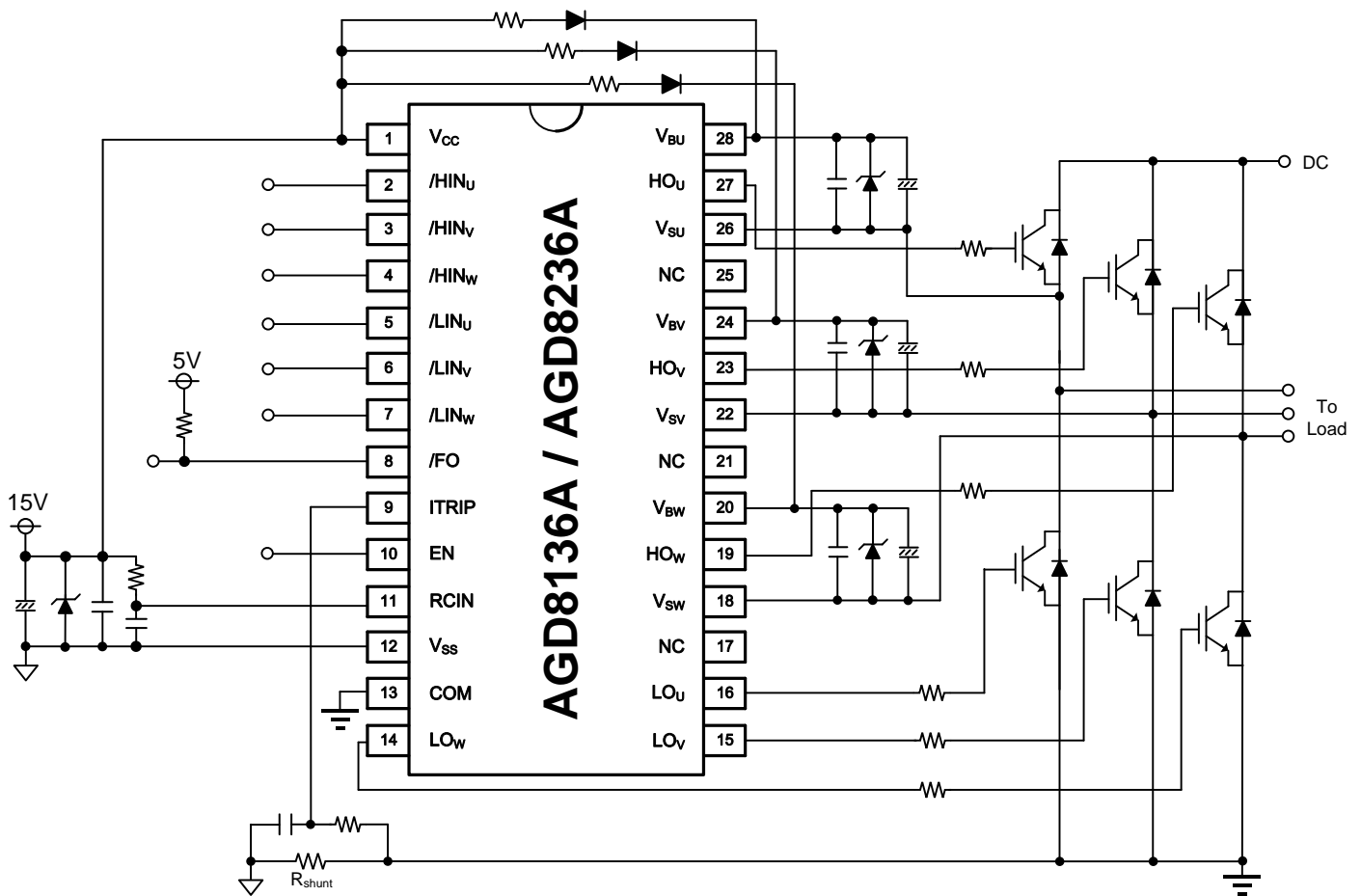
## Internal Block Diagram



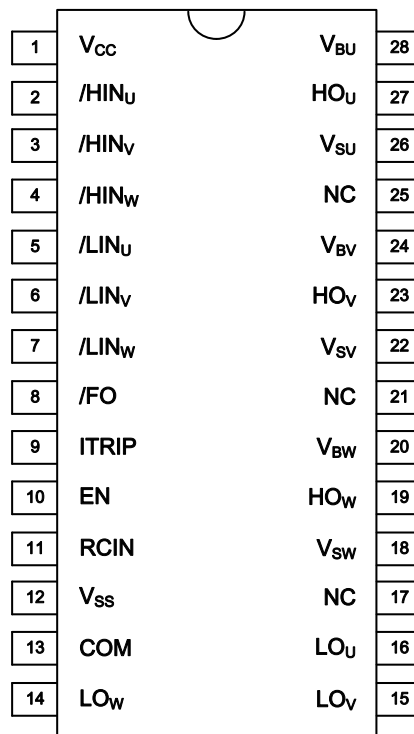
### Ordering Information

Part Number	Temperature Range	Package
AGD8136A	-40°C to 125°C	SOP-28L
AGD8236A	-40°C to 125°C	SOP-28L

### Typical Application Circuit



## Pin Configuration



**SOP-28L**  
**(Top View)**

## Pin Description

Pin Number	Pin Name	Pin Function
1	V <sub>CC</sub>	Low-Side Supply Voltage
2	/HIN <sub>U</sub>	High-Side Logic Input (U-Phase)
3	/HIN <sub>V</sub>	High-Side Logic Input (V-Phase)
4	/HIN <sub>W</sub>	High-Side Logic Input (W-Phase)
5	/LIN <sub>U</sub>	Low-Side Logic Input (U-Phase)
6	/LIN <sub>V</sub>	Low-Side Logic Input (V-Phase)
7	/LIN <sub>W</sub>	Low-Side Logic Input (W-Phase)
8	/FO	Fault Output with Open Drain (Indicates Over-Current and V <sub>CC</sub> UVLO)
9	ITRIP	Analog Input for Over-Current Shutdown
10	EN	Enable I/O Functionality (Positive Logic)
11	RCIN	External RC-Network Input used to define Fault Output Duration Time
12	V <sub>SS</sub>	Logic Ground
13	COM	Power Ground
14	LO <sub>W</sub>	Low-Side Driver Output (W-Phase)
15	LO <sub>V</sub>	Low-Side Driver Output (V-Phase)
16	LO <sub>U</sub>	Low-Side Driver Output (U-Phase)

**Pin Description (continued)**

Pin Number	Pin Name	Pin Function
17	NC	No Connection
18	V <sub>SW</sub>	High-Side Floating Supply Offset Voltage (W-Phase)
19	HO <sub>W</sub>	High-Side Driver Output (W-Phase)
20	V <sub>BW</sub>	High-Side Floating Supply Voltage (W-Phase)
21	NC	No Connection
22	V <sub>SV</sub>	High-Side Floating Supply Offset Voltage (V-Phase)
23	HO <sub>V</sub>	High-Side Driver Output (V-Phase)
24	V <sub>BV</sub>	High-Side Floating Supply Voltage (V-Phase)
25	NC	No Connection
26	V <sub>SU</sub>	High-Side Floating Supply Offset Voltage (U-Phase)
27	HO <sub>U</sub>	High-Side Driver Output (U-Phase)
28	V <sub>BU</sub>	High-Side Floating Supply Voltage (U-Phase)

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute values referenced to  $V_{SS}$  unless otherwise stated in the table.

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Low-Side Supply Voltage	-0.3	20 <sup>(1)</sup>	V
$V_{IN}$	Logic Input Voltage (/LIN, /HIN)	$V_{SS}-0.3$	$V_{SS}+5.2$	
$V_{ITRIP}$	ITRIP Input Voltage	$V_{SS}-0.3$	$V_{SS}+5.2$	
$V_{EN}$	Enable Input Voltage	$V_{SS}-0.3$	$V_{SS}+5.2$	
$V_{RCIN}$	RCIN Input Voltage	$V_{SS}-0.3$	$V_{CC}+0.3$	
$V_B$	High-Side Floating Supply Voltage	-0.3	620	
$V_S$	High-Side Floating Supply Offset Voltage	$V_B-20$ <sup>(1)</sup>	$V_B+0.3$	
$V_{HO}$	High-Side Driver Output Voltage	$V_S-0.3$	$V_B+0.3$	
$V_{LO}$	Low-Side Driver Output Voltage	COM-0.3	$V_{CC}+0.3$	
$V_{FO}$	Fault Output Voltage	$V_{SS}-0.3$	$V_{CC}+0.3$	
COM	Power Ground	$V_{CC}-25$	$V_{CC}+0.3$	
$dV_S/dt$	$V_S$ Offset Voltage Slew Rate <sup>(2)</sup>	-	50	V/ns
$PW_{HIN}$	High-Side Input Pulse Width	500	-	ns
$P_D$	Package Power Dissipation @ $T_A \leq 25^\circ\text{C}$	-	1.6	W
$R_{th(j-a)}$	Thermal Resistance, Junction to Ambient	-	78	$^\circ\text{C}/\text{W}$
$T_J$	Junction Temperature	-	150	$^\circ\text{C}$
$T_S$	Storage Temperature	-55	150	
$T_L$	Lead Temperature (Soldering, 10 seconds)	-	300	
ESD	Human Body Model	2		kV

**Note:**

1. An internal 20V zener diode is integrated to clamp each supply voltage.
2. Not subject of production test, verified by characterization.

## Recommended Operation Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions. All voltage parameters are absolute voltages referenced to  $V_{SS}$  unless otherwise specified. The offset rating is tested with supplies of  $(V_{CC} - COM) = (V_B - V_S) = 15\text{ V}$ .

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$	Low-Side Supply Voltage	AGD8136A	10	20	V
		AGD8236A	13.2	20	
$V_{IN}$	Logic Input Voltage (/LIN, /HIN)	$V_{SS}$	$V_{SS}+5$		
$V_{EN}$	Enable Input Voltage	$V_{SS}$	$V_{SS}+5$		
$V_B$	High-Side Floating Supply Voltage	AGD8136A	$V_S+10$	$V_S+20$	
		AGD8236A	$V_S+13.2$	$V_S+20$	
$V_S$	High-Side Floating Supply Offset Voltage <sup>(3)</sup>	COM-6	600		
$V_S(t)$	Transient High-Side Floating Supply Voltage <sup>(4)</sup>	-50	600		
$V_{HO}$	High-Side Driver Output Voltage	$V_S$	$V_B$		
$V_{LO}$	Low-Side Driver Output Voltage	COM	$V_{CC}$		
COM	Power Ground	-5	5		
$V_{FO}$	Fault Output Voltage	$V_{SS}$	$V_{CC}$		
$V_{RCIN}$	RCIN Input Voltage	$V_{SS}$	$V_{CC}$		
$V_{ITRIP}$	ITRIP Input Voltage	$V_{SS}$	$V_{SS}+5$		
$T_A$	Ambient Temperature	-40	125	°C	

### Note:

- Logic operation for  $V_S$  of -6V to 600V. Logic state held for  $V_S$  of -6V to  $-V_{BS}$ .
- Operational for transient negative  $V_S$  of  $V_{SS}-50\text{V}$  with a 50ns pulse width, which is guaranteed by design.

## Static Electrical Characteristics

$V_{CC} = V_{BS} = 15\text{V}$ .  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$UV_{CC+}$	$V_{CC}$ Under-Voltage Positive Going Threshold	AGD8136A	8.0	8.9	9.8	V
		AGD8236A	10.8	11.9	13.0	
$UV_{CC-}$	$V_{CC}$ Under-Voltage Negative Going Threshold	AGD8136A	7.4	8.2	9.0	
		AGD8236A	10.3	11.4	12.5	
$UV_{CChys}$	$V_{CC}$ Under-Voltage Hysteresis	AGD8136A	-	0.7	-	
		AGD8236A	-	0.5	-	
$UV_{BS+}$	$V_{BS}$ Under-Voltage Positive Going Threshold	AGD8136A	8.0	8.9	9.8	
		AGD8236A	10.0	11.0	12.0	
$UV_{BS-}$	$V_{BS}$ Under-Voltage Negative Going Threshold	AGD8136A	7.4	8.2	9.0	
		AGD8236A	9.0	10.0	11.0	
$UV_{BSHys}$	$V_{BS}$ Under-Voltage Hysteresis	AGD8136A	-	0.7	-	
		AGD8236A	-	1.0	-	
$I_{LK}$	High-Side Floating Supply Leakage Current (per 1-Phase)	$V_B = V_S = 600\text{V}$	-	-	50	μA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current (per 1-Phase)	V <sub>IN</sub> =5V	-	70	120	
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> Supply Current (per 1-Phase)	(all inputs are in the off state)	-	1	2	mA
V <sub>OH</sub>	High Level Output Voltage Drop, V <sub>BIAS</sub> - V <sub>O</sub>	I <sub>O</sub> =20mA, V <sub>IN</sub> =0V	-	0.9	1.4	V
V <sub>OL</sub>	Low Level Output Voltage Drop, V <sub>O</sub>	I <sub>O</sub> =20mA, V <sub>IN</sub> =5V	-	0.4	0.6	
I <sub>O+</sub>	Output High Current with Capacitive Load	C <sub>L</sub> =10nF	120	200	-	mA
I <sub>Opk+</sub>	Peak Output High Short Circuit Pulsed Current	V <sub>O</sub> =0V, PW≤10μs (Single Pulse)	-	220	-	
I <sub>O-</sub>	Output Low Current with Capacitive Load	C <sub>L</sub> =10nF	220	350	-	
I <sub>Opk-</sub>	Peak Output Low Short Circuit Pulsed Current	V <sub>O</sub> =15V, PW≤10μs (Single Pulse)	-	375	-	
V <sub>IH</sub>	High Level Input Voltage		2.5	-	-	V
V <sub>IL</sub>	Low Level Input Voltage		-	-	0.8	
V <sub>CLAMP</sub>	Input Clamp Voltage (/LIN, /HIN, ITRIP, EN)	I <sub>IN</sub> =100μA	5.2	5.6	5.9	
I <sub>HIN+</sub>	Input Bias Current	V <sub>HIN</sub> =5V	-	110	150	μA
I <sub>HIN-</sub>	Input Bias Current	V <sub>HIN</sub> =0V	-	150	200	
I <sub>LIN+</sub>	Input Bias Current	V <sub>LIN</sub> =5V	-	110	150	
I <sub>LIN-</sub>	Input Bias Current	V <sub>LIN</sub> =0V	-	150	200	
V <sub>RCIN,TH</sub>	RCIN Positive Going Threshold		-	8	-	V
I <sub>RCIN</sub>	RCIN Input Bias Current	V <sub>RCIN</sub> =0V or 15V	-	-	1	μA
R <sub>RCIN,ON</sub>	RCIN Low On-Resistance	I=1.5mA	-	50	100	Ω
V <sub>IT,TH+</sub>	ITRIP Positive Going Threshold		0.42	0.46	0.5	V
V <sub>IT,TH-</sub>	ITRIP Negative Going Threshold		-	0.4	-	
V <sub>IT,Hys</sub>	ITRIP Hysteresis		-	0.06	-	
I <sub>ITRIP+</sub>	High ITRIP Input Bias Current	V <sub>ITRIP</sub> =4V	-	5	40	μA
I <sub>ITRIP-</sub>	Low ITRIP Input Bias Current	V <sub>ITRIP</sub> =0V	-	-	1	
V <sub>EN,TH+</sub>	EN Positive Going Threshold		-	-	2.5	V
V <sub>EN,TH-</sub>	EN Negative Going Threshold		0.8	-	-	
I <sub>EN+</sub>	High EN Input Bias Current	V <sub>EN</sub> =5V	-	5	40	μA
I <sub>EN-</sub>	Low EN Input Bias Current	V <sub>EN</sub> =0V	-	-	1	
R <sub>FO,ON</sub>	Fault Low On-Resistance	I=1.5mA	-	50	100	Ω

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$  or  $V_{BS}$ ) = 15V,  $C_L$  = 1000pF and  $T_A$  = 25°C unless otherwise specified.

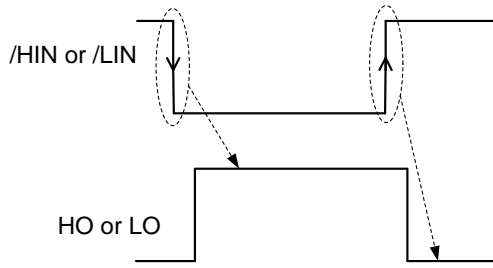
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{ON}$	Turn-On Propagation Delay	$V_{IN}=0V$ or $5V$	400	530	750	ns
$t_{OFF}$	Turn-Off Propagation Delay		400	530	750	
$t_R$	Turn-On Rise Time		-	125	190	
$t_F$	Turn-Off Fall Time		-	50	75	
$t_{IN,FLT}$	Input Filter Time (/LIN, /HIN) <sup>(5)</sup>		200	350	510	
$t_{EN}$	EN Low to Output Shutdown Propagation Delay	$V_{IN}=0V$ $V_{EN}=5V \rightarrow 0V$	250	460	650	
$t_{EN,FLT}$	EN Input Filter Time		100	200	-	
$t_{FOd}$	Fault Output Duration Time (RCIN: C = 1nF, R = 2MΩ)	$V_{ITRIP}=1V$	1.3	1.65	-	ms
$t_{ITRIP}$	ITRIP to Output Shutdown Propagation Delay	Low Side	420	620	970	ns
		High Side	600	800	1150	
$t_{IT,FLT}$	ITRIP Filter Time	$V_{ITRIP}=5V$ , $V_{IN}=0V$ , $V_{FO}=5V$ (10kΩ pull-up)	-	400	-	
$t_{FO}$	ITRIP to FO Propagation Delay		400	600	950	
DT	Dead Time <sup>(6)</sup>	$V_{IN}=0V$ or $5V$ without External Dead Time	100	275	420	
MT	Matching Delay Time ( $t_{ON}$ , $t_{OFF}$ ) <sup>(7)</sup>	$ t_{ON(HO)} - t_{ON(LO)} $ or $ t_{OFF(HO)} - t_{OFF(LO)} $	-	-	100	
PM	Output Pulse Width Matching <sup>(8)</sup>	Input Pulse Width=10μs	-	-	150	

### Note:

- The minimum width of the input pulse is recommended to exceed 500ns to ensure the filtering time of the input filter.
- Please refer to 'Dead Time' definition of 'Function Diagram'.
- This parameter, MT and MDT applies to all of the channels.
- PM is defined as |(input pulse width) – (output pulse width)|.



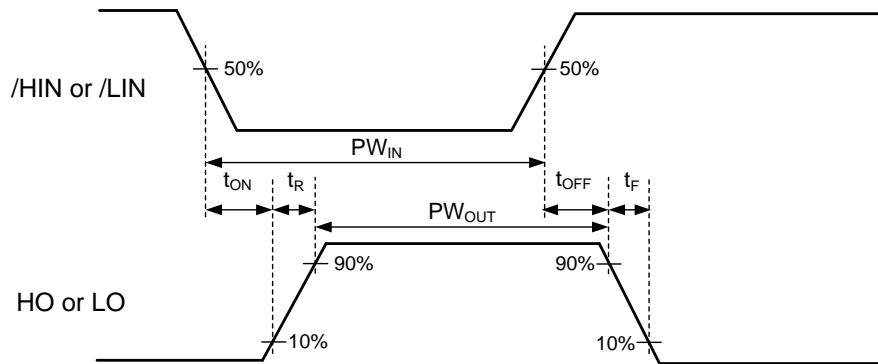
### Output Activation



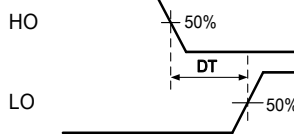
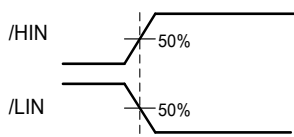
EN	/HIN	/LIN	HO	LO
L	L or H	L or H	L	L
H	H	L	L	H
	L	H	H	L

Note: Output signal (HO or LO) is triggered by the edge of input signal.

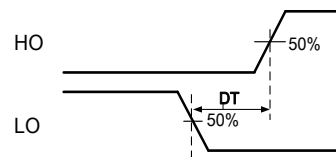
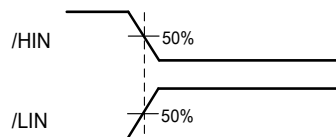
### Input / Output Timing Diagram



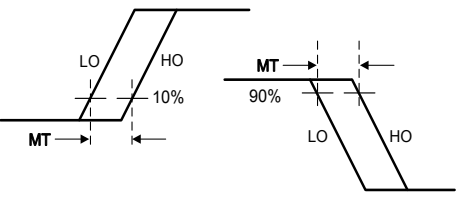
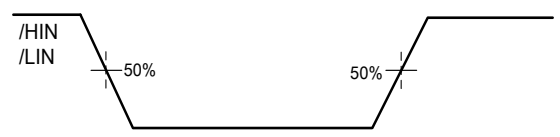
### Dead Time Activation



</HIN off and /LIN on>



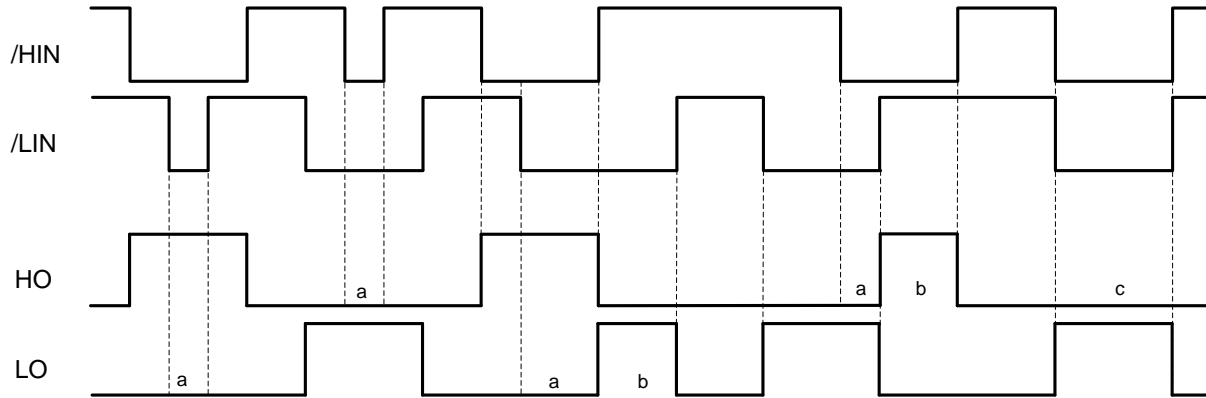
</HIN on and /LIN off>



<Delay Matching Waveform Definition>

## Function Timing Diagram

### A. Illustration of Shoot-Through (Cross-Conduction) Protection Logic

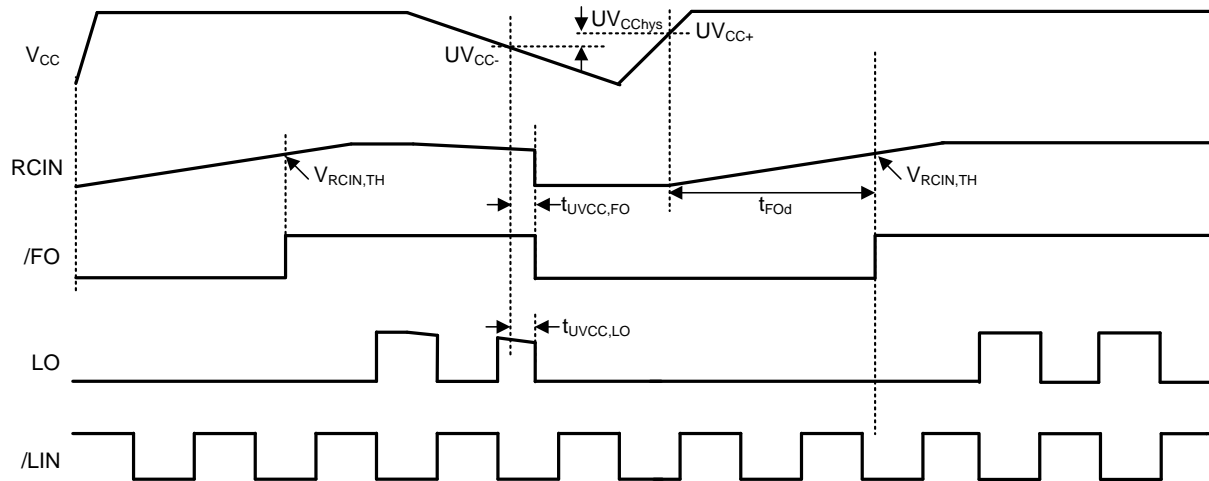


**Note:**

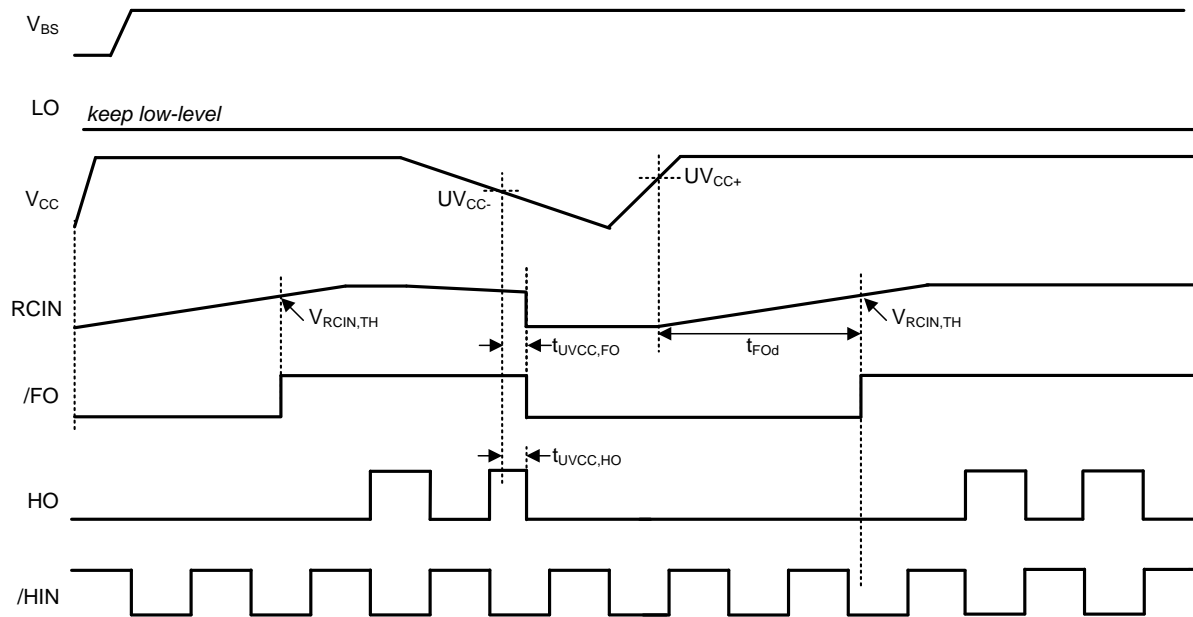
- a. When one output (high or low side) is turned on, the other side turn-on input is ignored.
- b. If both outputs are changed simultaneously, the turn-on activation is done by the internal dead time of 275ns typ. (For more information, please refer to below 'Dead Time' section.)
- c. When high-side (/HIN) and low-side (/LIN) have turn-on inputs at the same time, low-side (/LIN) has the priority.

### B. $V_{CC}$ ( $V_{BS}$ ) Supply Under-Voltage (UV) Lockout Timing Diagram

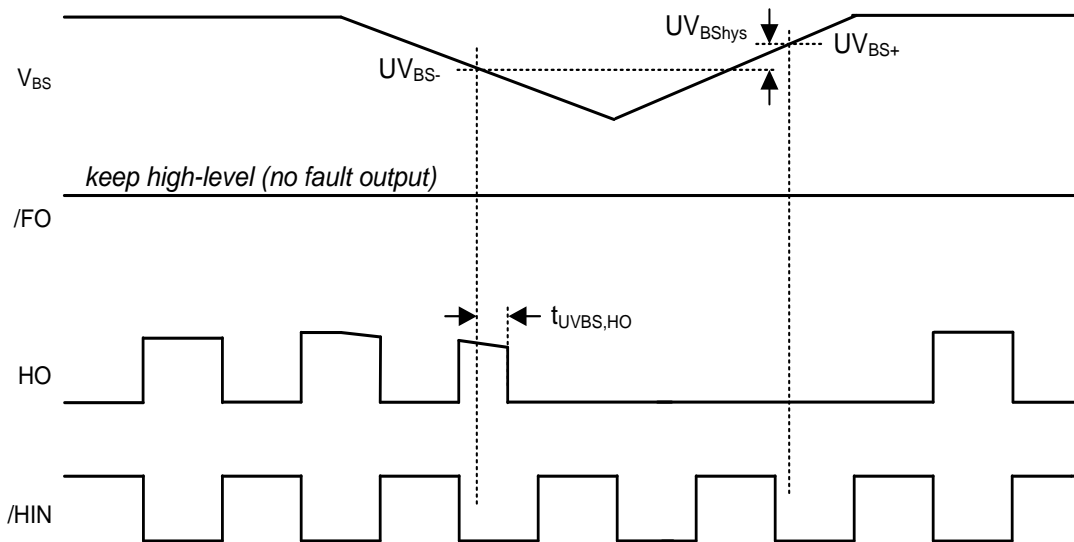
#### a. LO operation by $V_{CC}$ under-voltage protection



b. HO operation by  $V_{CC}$  under-voltage protection

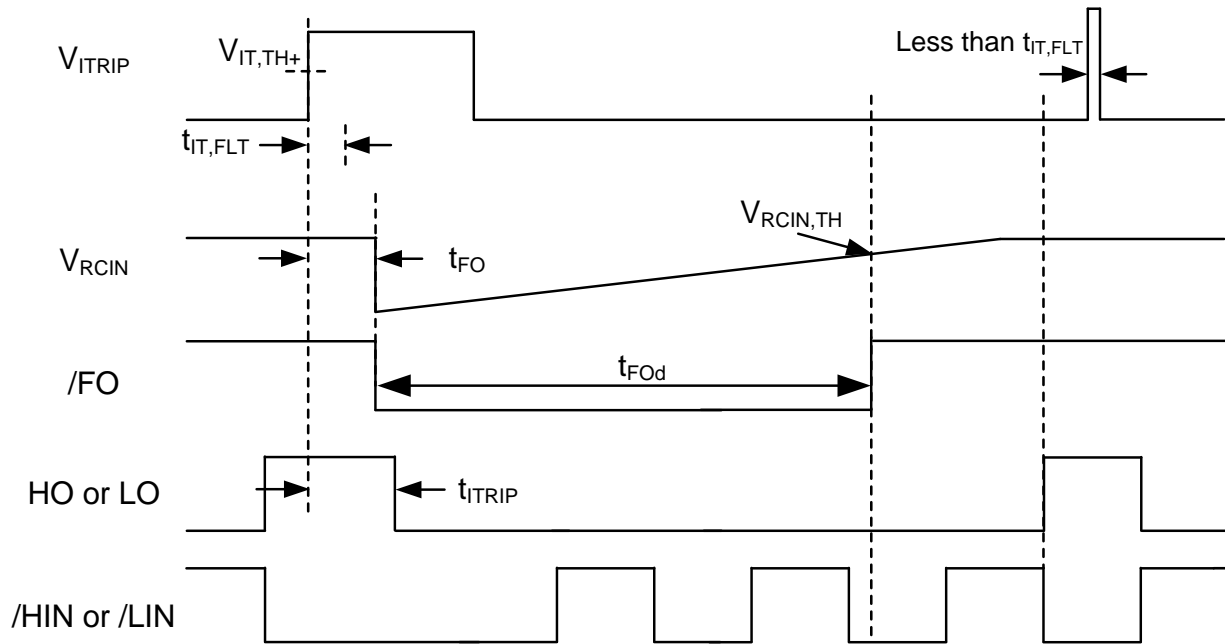


c.  $V_{BS}$  supply under-voltage (UV) lockout timing diagram

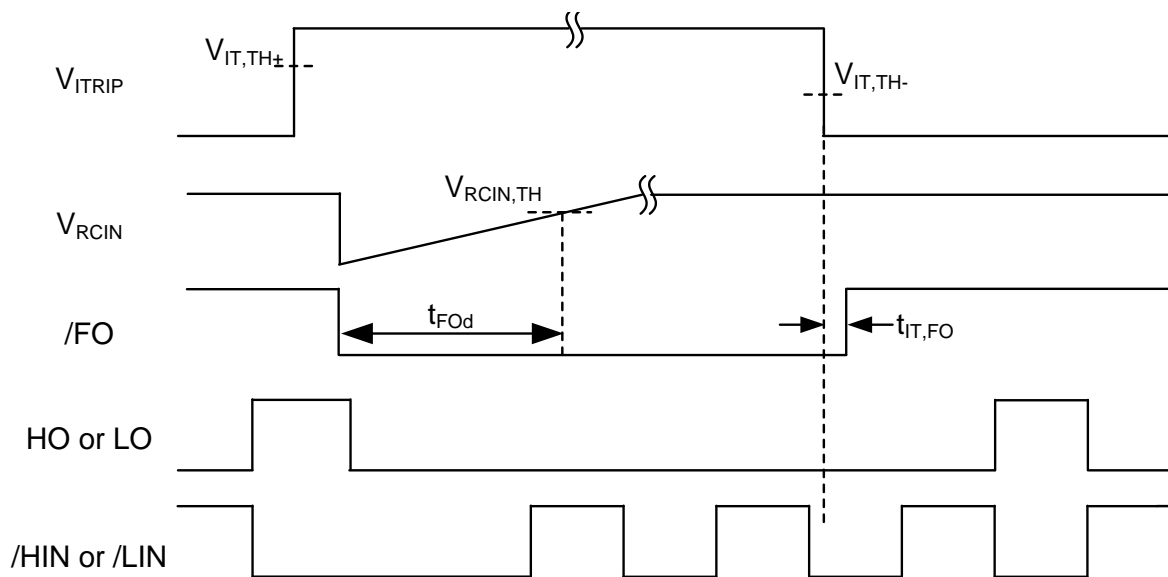


C. Over-Current Protection

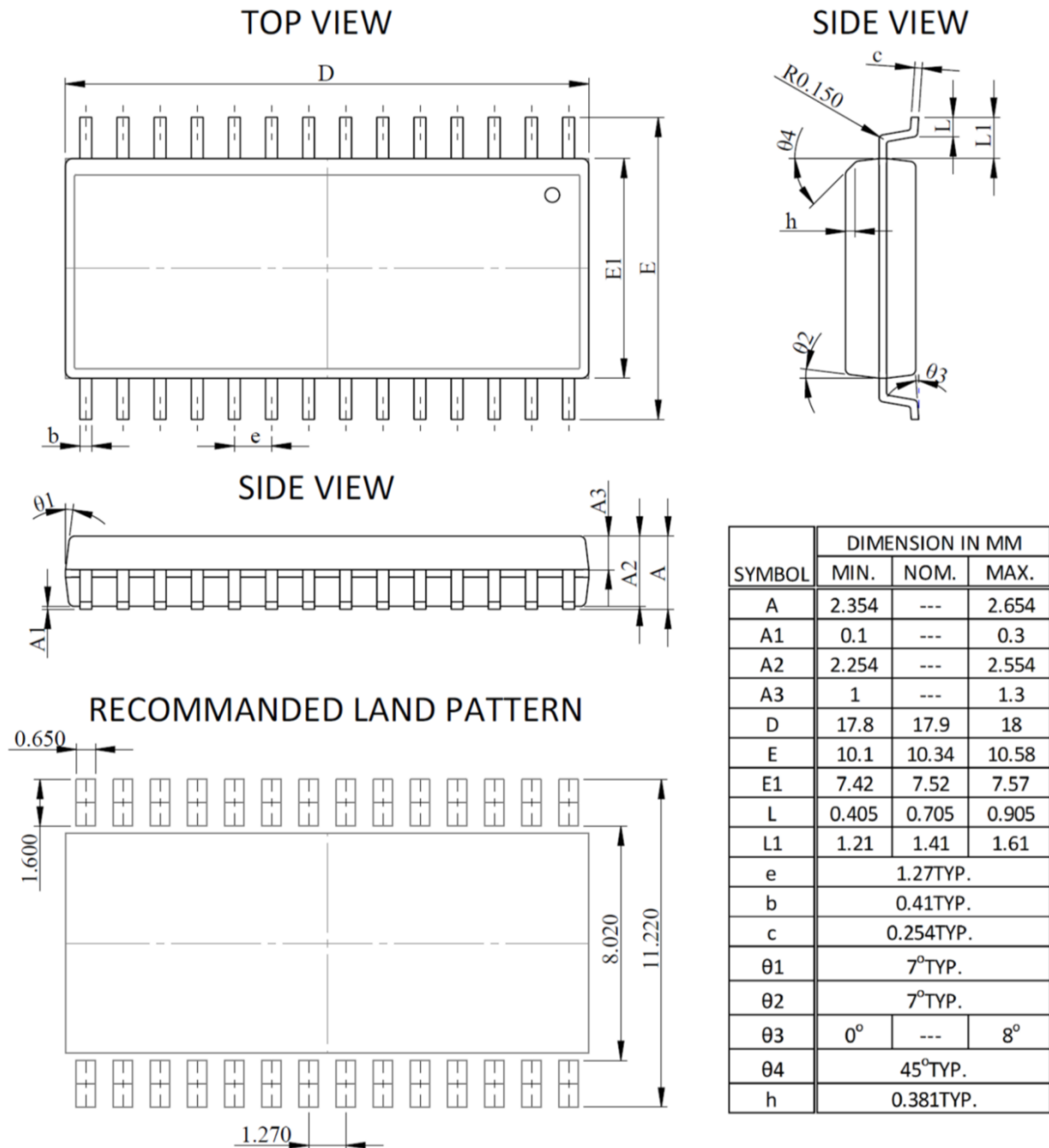
a. When ITRIP voltage rises higher than positive going threshold for  $t < t_{FOd}$



b. When ITRIP voltage keeps longer than  $t_{FOd}$



Package Dimensions, SOP-28L



NOTES

1. CONTROLLING DIMENSION : MM.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.

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