



General Description

- Proprietary α MOS5™ technology
- Low $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

Applications

- Flyback for SMPS
- Charger, Adapter, lighting

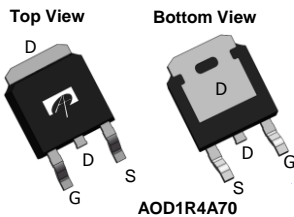
Product Summary

$V_{DS} @ T_{j,max}$	800V
I_{DM}	15A
$R_{DS(ON),max}$	< 1.4 Ω
$Q_{g,typ}$	8nC
$E_{OSS} @ 400V$	1 μ J

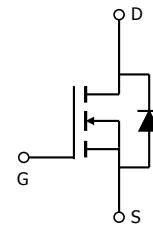
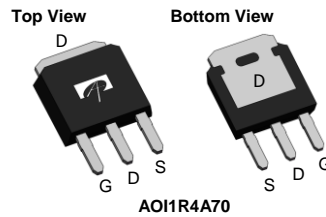
100% UIS Tested
100% R_g Tested



TO252



TO-251A



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD1R4A70	TO252	Tape & Reel	2500
AOI1R4A70	TO251A	Tube	3500

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	700	V
Gate-Source Voltage	V_{GS}	± 20	V
Gate-Source Voltage (dynamic) AC($f > 1\text{Hz}$)	V_{GS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	3.8
		$T_C=100^\circ\text{C}$	2.4
Pulsed Drain Current ^C	I_{DM}	15	A
Avalanche Current ^C $L=1\text{mH}$	I_{AR}	1.1	A
Repetitive avalanche energy ^C	E_{AR}	0.6	mJ
Single pulsed avalanche energy ^H	E_{AS}	2.7	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Peak diode recovery dv/dt		20	
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	48
		Derate above 25°C	0.4
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	45	55	$^\circ\text{C}/\text{W}$
Maximum Case-to-sink ^A	$R_{\theta CS}$	-	0.5	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	2	2.6	$^\circ\text{C}/\text{W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	700	-	-	V
		I _D =250μA, V _{GS} =0V, T _J =150°C	-	800	-	
BV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D =250μA, V _{GS} =0V	-	0.59	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =700V, V _{GS} =0V	-	-	1	μA
		V _{DS} =560V, T _J =125°C	-	-	10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	2.9	3.5	4.1	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =1A	-	1.16	1.4	Ω
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =1A	-	1.8	-	S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V	-	0.8	1.2	V
I _S	Maximum Body-Diode Continuous Current		-	-	3.8	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C		-	-	15	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	-	354	-	pF
C _{oss}	Output Capacitance		-	12	-	pF
C _{o(er)}	Effective output capacitance, energy related ^H	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz	-	11.2	-	pF
C _{o(tr)}	Effective output capacitance, time related ^I		-	46.9	-	pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	-	1.3	-	pF
R _g	Gate resistance	f=1MHz	-	7.3	-	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =1.9A	-	8	-	nC
Q _{gs}	Gate Source Charge		-	2	-	nC
Q _{gd}	Gate Drain Charge		-	2	-	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =400V, I _D =1.9A, R _G =5Ω	-	15	-	ns
t _r	Turn-On Rise Time		-	7.5	-	ns
t _{D(off)}	Turn-Off DelayTime		-	32	-	ns
t _f	Turn-Off Fall Time		-	13.5	-	ns
t _{rr}	Body Diode Reverse Recovery Time		-	176	-	ns
I _{rm}	Peak Reverse Recovery Current	I _F =1.9A, di/dt=100A/μs, V _{DS} =400V	-	11	-	A
Q _{rr}	Body Diode Reverse Recovery Charge		-	1.4	-	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C.

G. These tests are performed with the device mounted on 1 in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

H. L=60mH, I_{AS}=0.3 A, R_G=25Ω, Starting T_J=25° C.

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

APPLICATIONS OR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

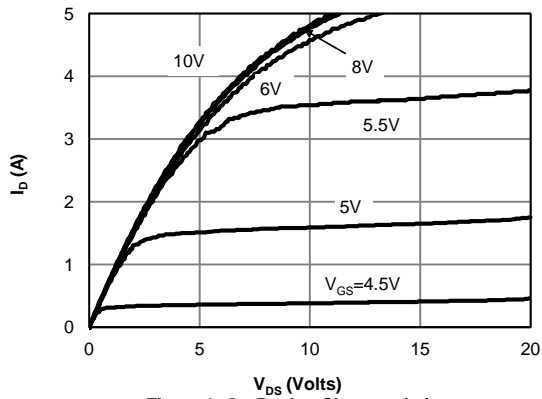


Figure 1: On-Region Characteristics

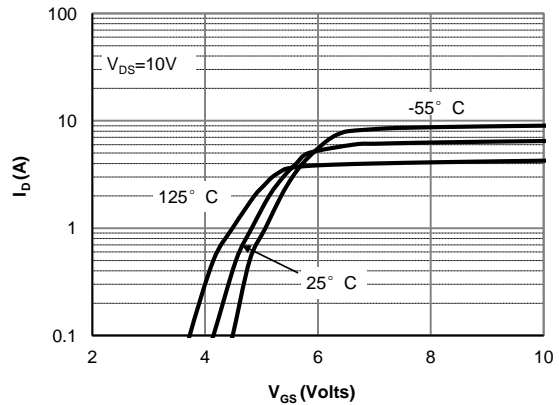


Figure 2: Transfer Characteristics

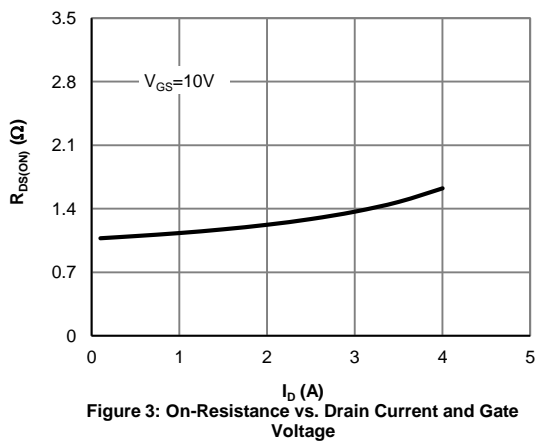


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

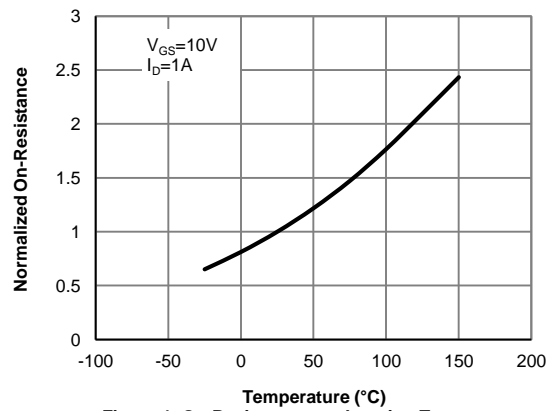


Figure 4: On-Resistance vs. Junction Temperature

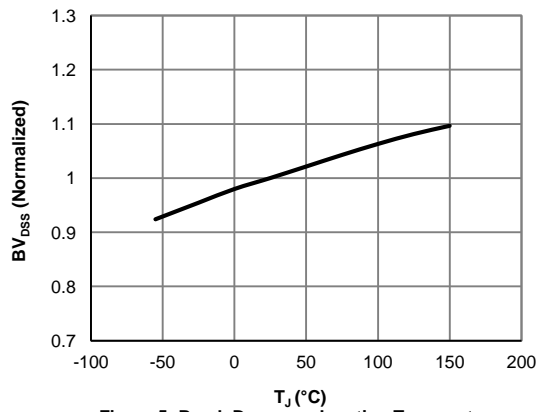


Figure 5: Break Down vs. Junction Temperature

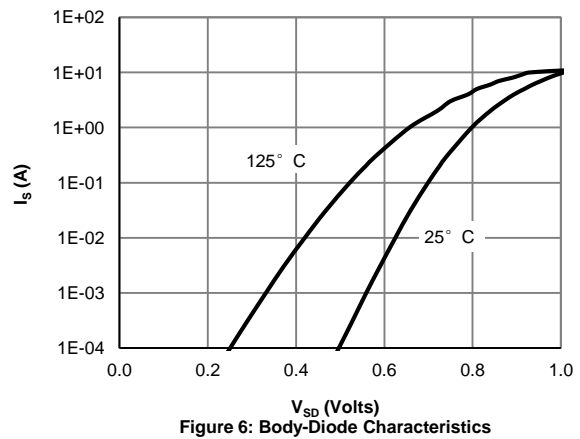


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

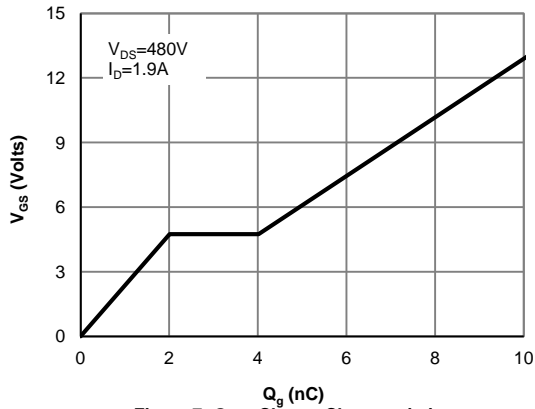


Figure 7: Gate-Charge Characteristics

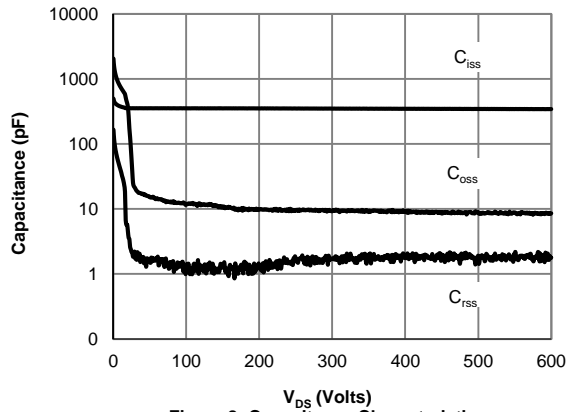


Figure 8: Capacitance Characteristics

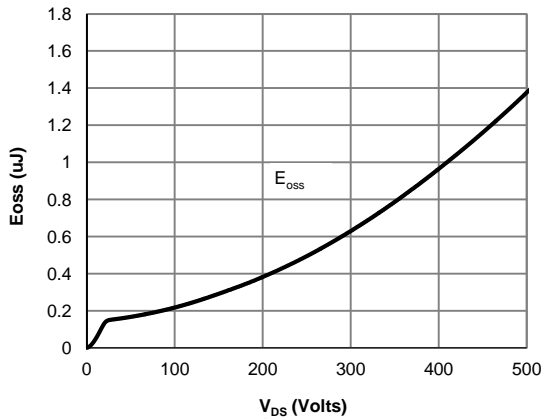


Figure 9: Coss stored Energy

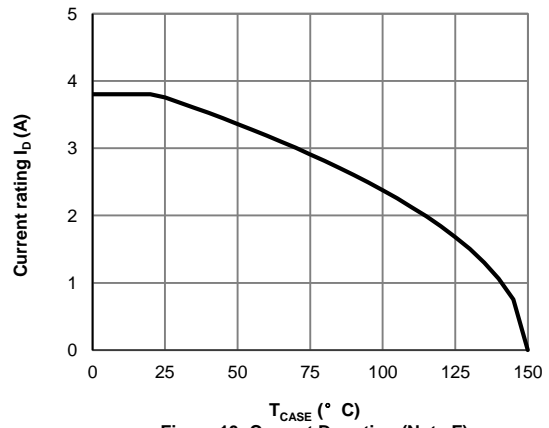


Figure 10: Current De-rating (Note F)

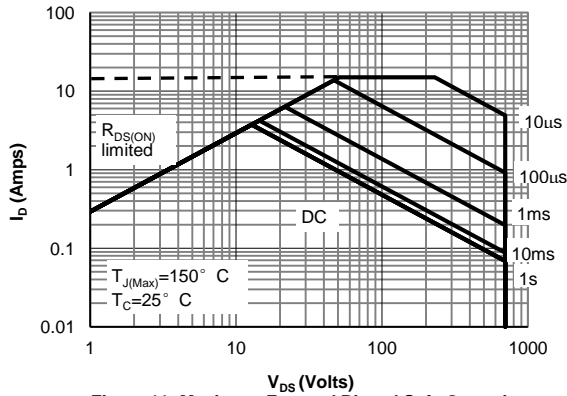


Figure 11: Maximum Forward Biased Safe Operating Area for AOD(I)1R4A70 (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

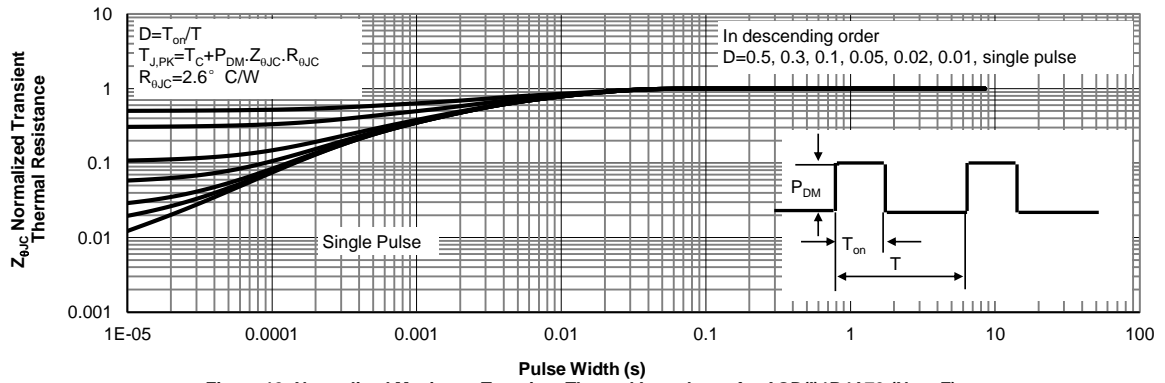
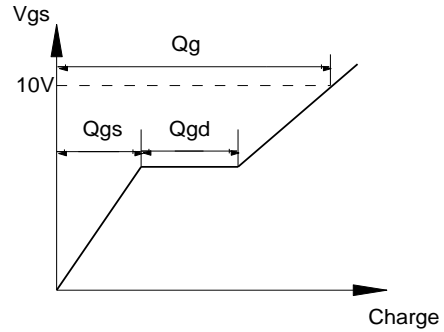
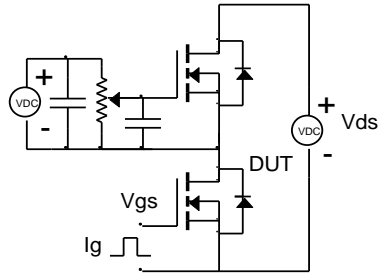
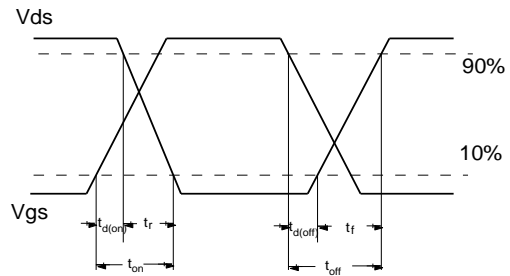
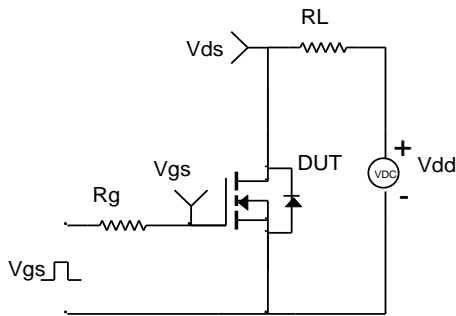


Figure 12: Normalized Maximum Transient Thermal Impedance for AOD(I)1R4A70 (Note F)

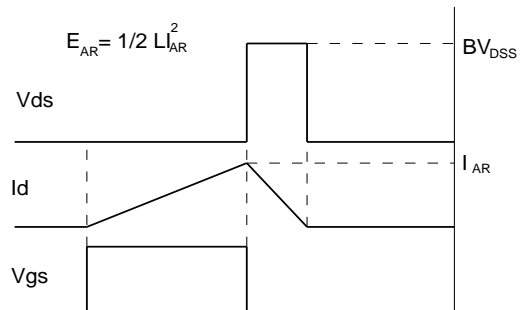
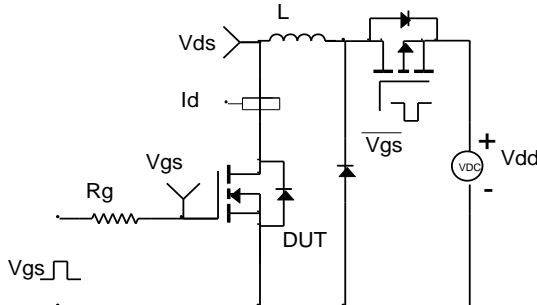
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

