

### General Description

- Proprietary  $\alpha$ MOS5™ technology
- Low  $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

### Applications

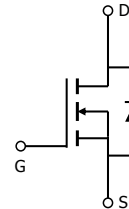
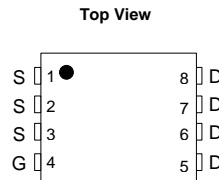
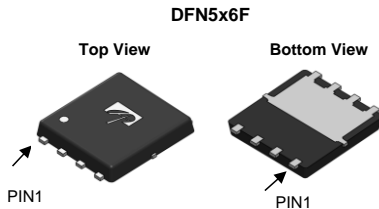
- PFC and PWM stages (Flyback, LLC) of Adapter, PC Silverbox, Server, Gaming Power Supply, Industrial, TV, Lighting

### Product Summary

$V_{DS} @ T_{j,max}$	800V
$I_{DM}$	46A
$R_{DS(ON),max}$	< 0.42 $\Omega$
$Q_{g,typ}$	21.5nC

$E_{oss} @ 400V$	2.8 $\mu$ J
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100% UIS Tested  
 100%  $R_g$  Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS420A70	DFN5x6F	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	700	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Gate-Source Voltage (dynamic) AC( $f > 1\text{Hz}$ )	$V_{GS}$	$\pm 30$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	12
		$T_C=100^\circ\text{C}$	7.5
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	46	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.6
Avalanche Current <sup>C</sup> $L=1\text{mH}$	$I_{AR}$	3.4	A
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	5.8	mJ
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	50	mJ
MOSFET dv/dt ruggedness	dv/dt	100	V/ns
Diode reverse recovery	dv/dt	$V_{DS}=0$ to 400V, $I_F \leq 6\text{A}$ , $T_J=25^\circ\text{C}$	20
		di/dt	500
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	183
		Derate above 25 $^\circ\text{C}$	1.5
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	4.2
		$T_A=70^\circ\text{C}$	2.7
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient <sup>A</sup> $t \leq 10\text{s}$	$R_{\theta JA}$	25	30	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup> Steady-State		45	55	$^\circ\text{C/W}$
Maximum Junction-to-Case Steady-State	$R_{\theta JC}$	0.42	0.68	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	700			V
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C		800		
BV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V		0.6		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =700V, V <sub>GS</sub> =0V			1	μA
		V <sub>DS</sub> =560V, T <sub>J</sub> =125°C			10	
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	3.4	4	4.6	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =6A		0.38	0.42	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =6A		8.6		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =6A, V <sub>GS</sub> =0V		0.86	1.2	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				12	A
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current <sup>C</sup>				46	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz		1360		pF
C <sub>oss</sub>	Output Capacitance			34		pF
C <sub>o(er)</sub>	Effective output capacitance, energy related <sup>I</sup>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0 to 480V, f=1MHz		32		pF
C <sub>o(tr)</sub>	Effective output capacitance, time related <sup>J</sup>			147		pF
C <sub>riss</sub>	Reverse Transfer Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz		1.7		pF
R <sub>g</sub>	Gate resistance	f=1MHz		2		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =480V, I <sub>D</sub> =6A		21.5		nC
Q <sub>gs</sub>	Gate Source Charge			10		nC
Q <sub>gd</sub>	Gate Drain Charge			6		nC
T <sub>d(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =400V, I <sub>D</sub> =6A, R <sub>G</sub> =5Ω		24.5		ns
T <sub>r</sub>	Turn-On Rise Time			17		ns
T <sub>d(off)</sub>	Turn-Off DelayTime			34.5		ns
T <sub>f</sub>	Turn-Off Fall Time			13		ns
T <sub>rr</sub>	Body Diode Reverse Recovery Time			310		ns
I <sub>rrm</sub>	Peak Reverse Recovery Current	I <sub>F</sub> =6A, dI/dt=100A/μs, V <sub>DS</sub> =400V		24.5		A
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge			4.8		μC

A. The value of R<sub>qJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>qJA</sub> t<sub>s</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>qJA</sub> is the sum of the thermal impedance from junction to case R<sub>qJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating

G. L=60mH, I<sub>AS</sub>=1.3A, R<sub>G</sub>=25Ω, Starting T<sub>J</sub>=25° C.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

I. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

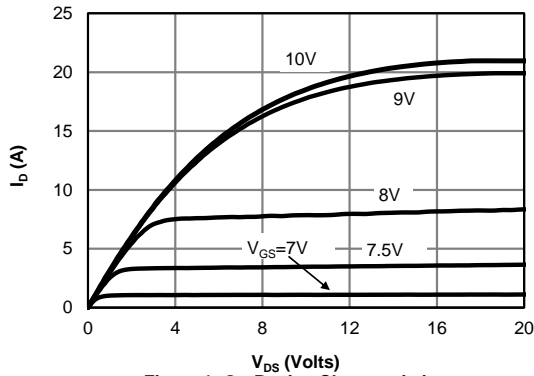
J. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

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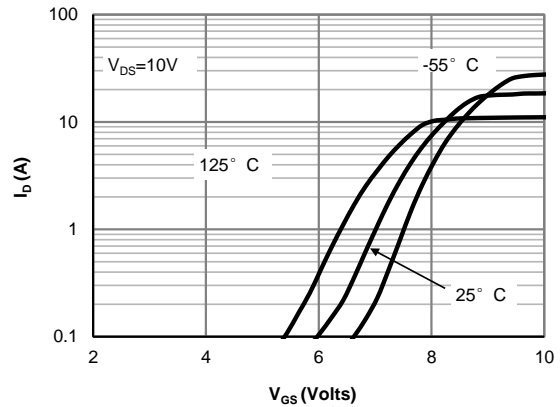
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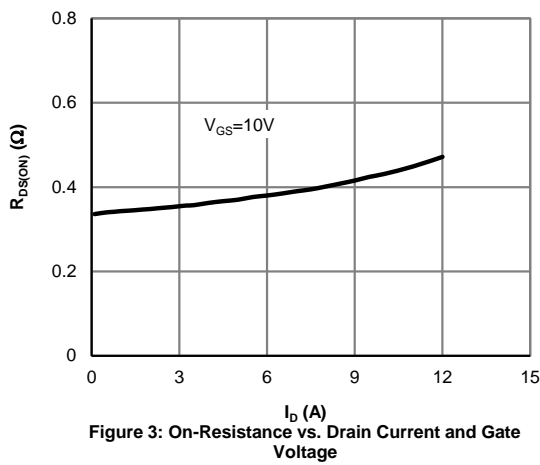
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



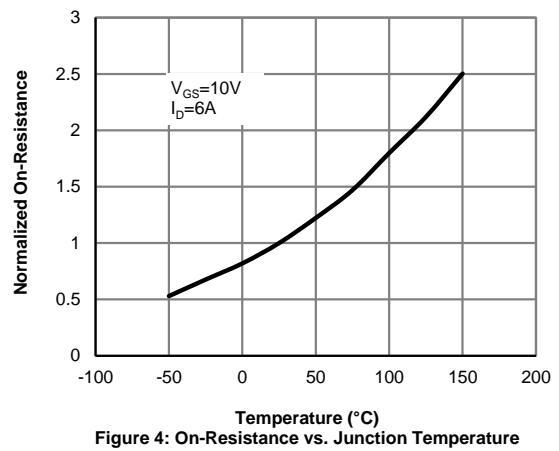
**Figure 1: On-Region Characteristics**



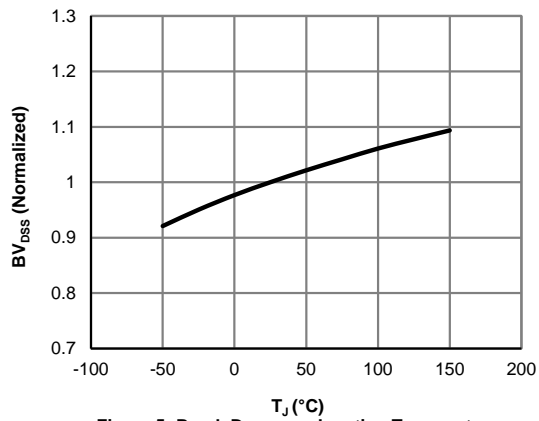
**Figure 2: Transfer Characteristics**



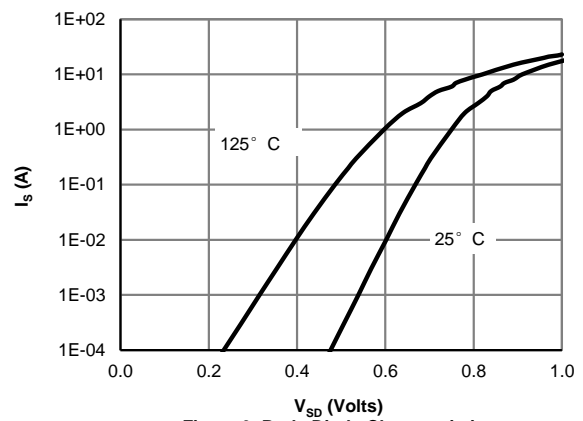
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

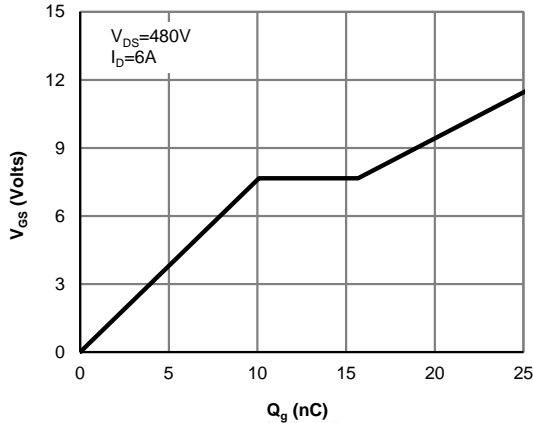


**Figure 5: Break Down vs. Junction Temperature**

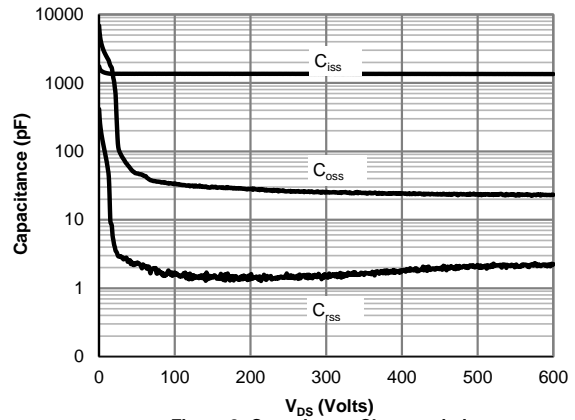


**Figure 6: Body-Diode Characteristics**

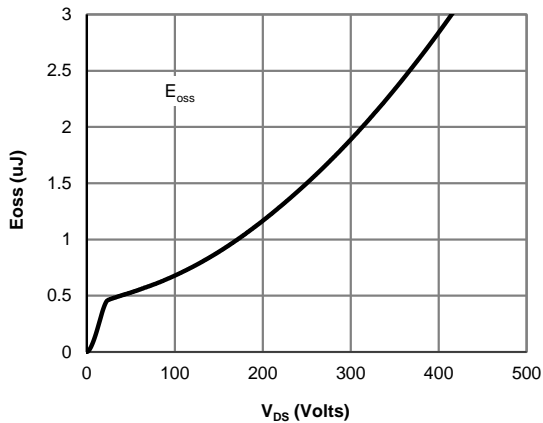
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



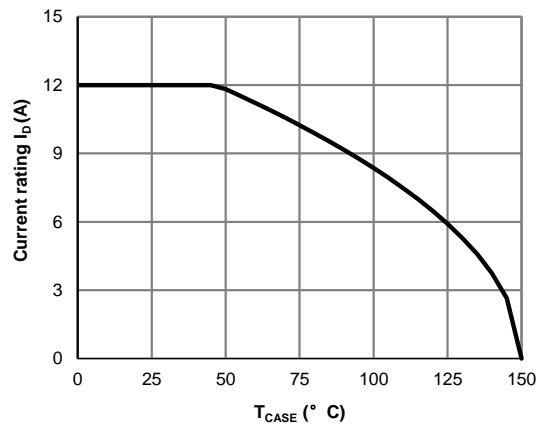
**Figure 7: Gate-Charge Characteristics**



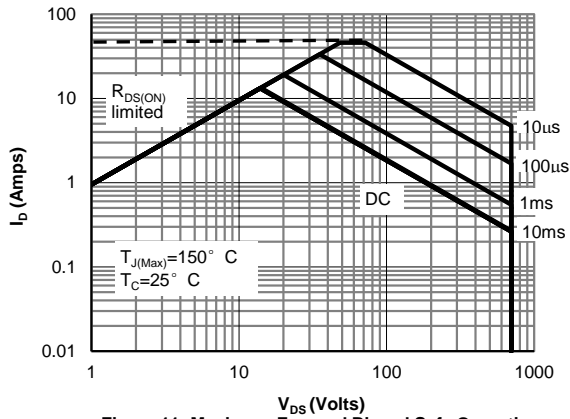
**Figure 8: Capacitance Characteristics**



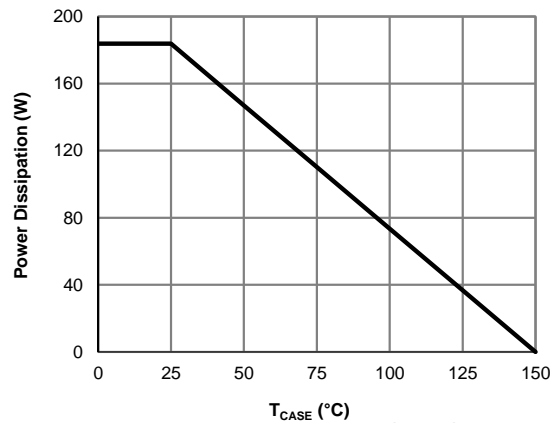
**Figure 9: Coss stored Energy**



**Figure 10: Current De-rating (Note F)**

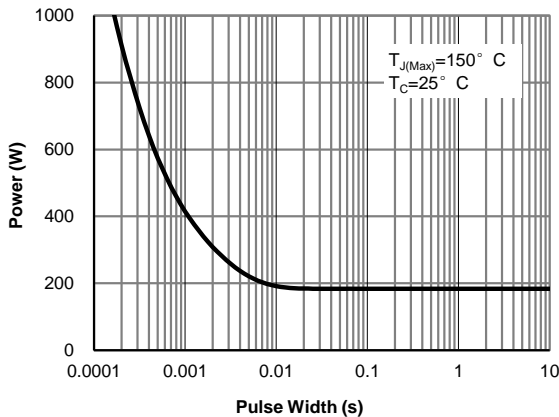


**Figure 11: Maximum Forward Biased Safe Operating Area (Note F)**

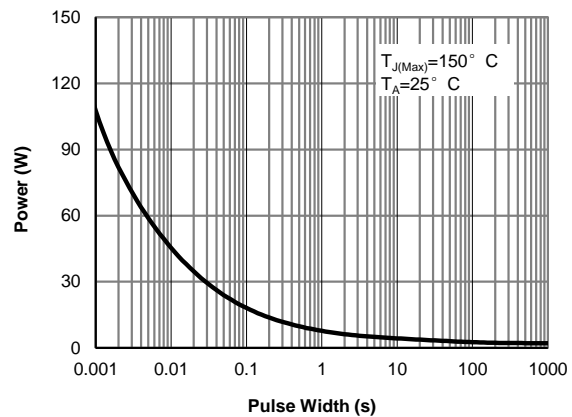


**Figure 12: Power De-rating (Note B)**

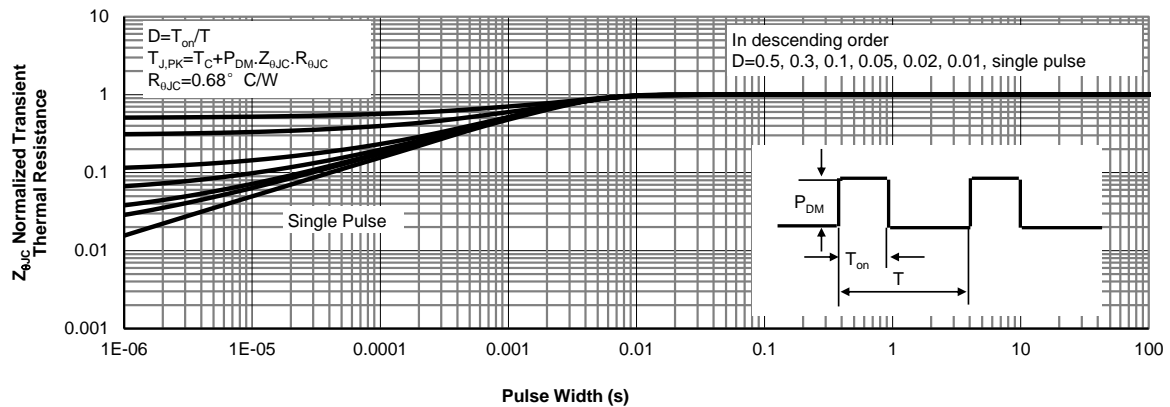
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



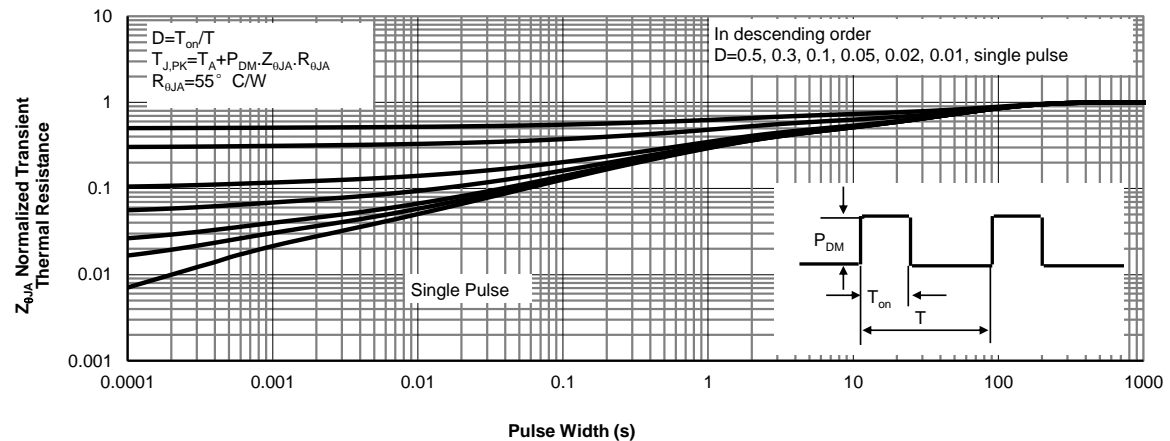
**Figure 13: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)**

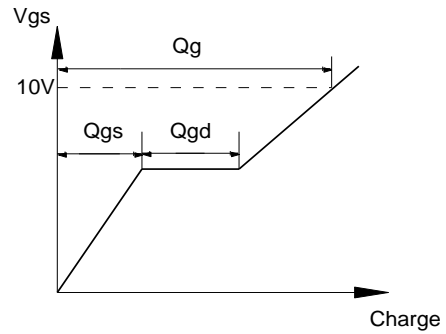
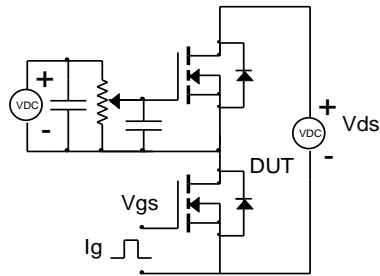


**Figure 15: Normalized Maximum Transient Thermal Impedance (Note F)**

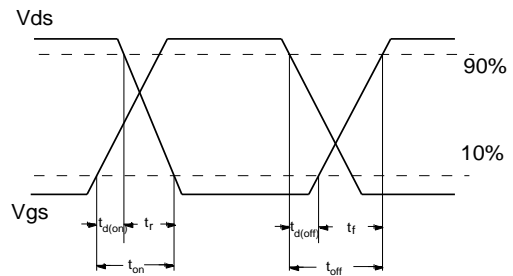
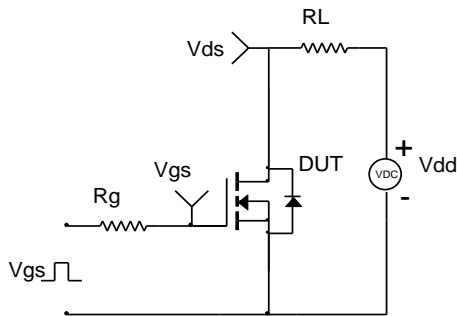


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)**

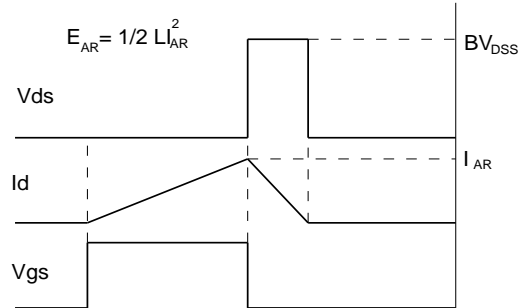
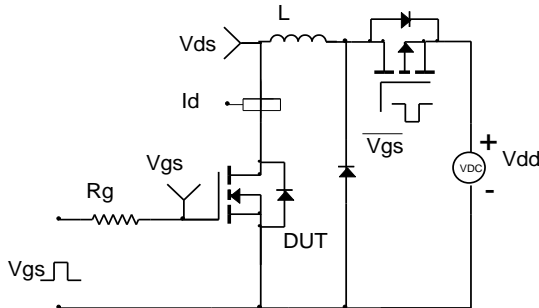
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

