
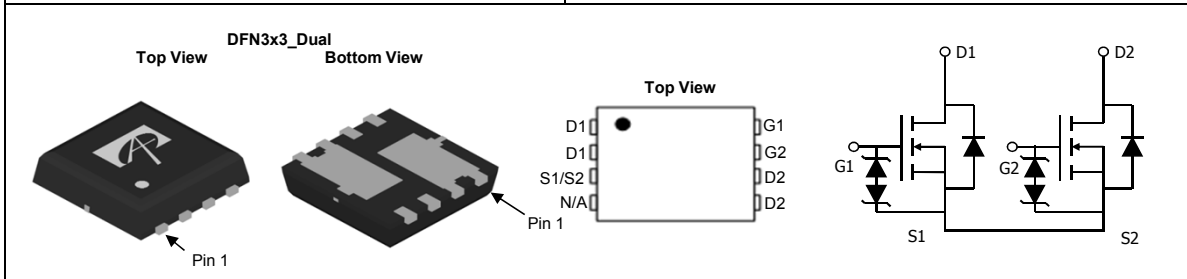


General Description <ul style="list-style-type: none"> Trench Power MOSFET technology Low $R_{D1D2(ON)}$ Logic Level Driving Pb-Free lead Plating, RoHS and Halogen-Free Compliant Applications <ul style="list-style-type: none"> USB PD Load switch 	Product Summary <table border="0" style="width: 100%;"> <tr> <td>V_{DS}</td> <td>30V</td> </tr> <tr> <td>I_D (at $V_{GS}=10V$)</td> <td>15A</td> </tr> <tr> <td>$R_{D1D2(ON)}$ (at $V_{GS}=10V$)</td> <td>< 13mΩ</td> </tr> <tr> <td>$R_{D1D2(ON)}$ (at $V_{GS}=4.5V$)</td> <td>< 18.5mΩ</td> </tr> </table> Typical ESD protection <table border="0" style="width: 100%;"> <tr> <td>100% UIS Tested</td> <td>HBM Class 1C</td> </tr> <tr> <td>100% Rg Tested</td> <td></td> </tr> </table> 	V_{DS}	30V	I_D (at $V_{GS}=10V$)	15A	$R_{D1D2(ON)}$ (at $V_{GS}=10V$)	< 13m Ω	$R_{D1D2(ON)}$ (at $V_{GS}=4.5V$)	< 18.5m Ω	100% UIS Tested	HBM Class 1C	100% Rg Tested	
V_{DS}	30V												
I_D (at $V_{GS}=10V$)	15A												
$R_{D1D2(ON)}$ (at $V_{GS}=10V$)	< 13m Ω												
$R_{D1D2(ON)}$ (at $V_{GS}=4.5V$)	< 18.5m Ω												
100% UIS Tested	HBM Class 1C												
100% Rg Tested													



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONU32320	DFN 3x3 EP	Tape & Reel	5000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	15
		$T_C=100^\circ\text{C}$	15
Pulsed Drain Current ^C	I_{DM}	56	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	15
		$T_A=70^\circ\text{C}$	12
Avalanche Current ^C	I_{AS}	20	A
Avalanche energy	E_{AS}	33	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	16.5
		$T_C=100^\circ\text{C}$	6.5
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	5
		$T_A=70^\circ\text{C}$	3.2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,B}				
Maximum Junction-to-Case	$R_{\theta JC}$	6	7.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.3	V
R _{D1D2(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =11A T _J =125°C		10.8	13	mΩ
		V _{GS} =4.5V, I _D =7A		16.7	20	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =11A		38		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ⁶				15	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1500		pF
C _{OSS}	Output Capacitance			160		pF
C _{rSS}	Reverse Transfer Capacitance			130		pF
R _g	Gate resistance	f=1MHz	1	2	3	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =11A		28	40	nC
Q _{g(4.5V)}	Total Gate Charge			13	22	nC
Q _{gs}	Gate Source Charge			3.5		nC
Q _{gd}	Gate Drain Charge			5.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.35Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			30		ns
t _f	Turn-Off Fall Time			6.5		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =11A, di/dt=500A/μs		7	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =11A, di/dt=500A/μs		10		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

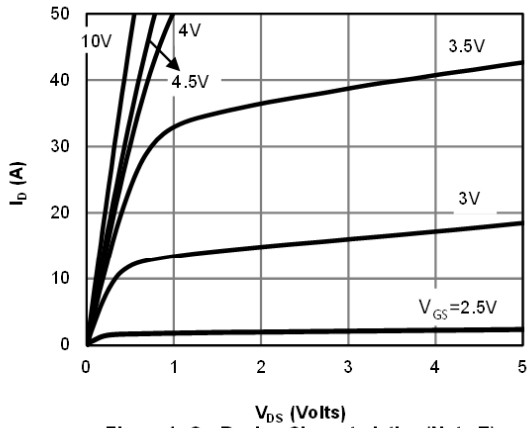


Figure 1: On-Region Characteristics (Note E)

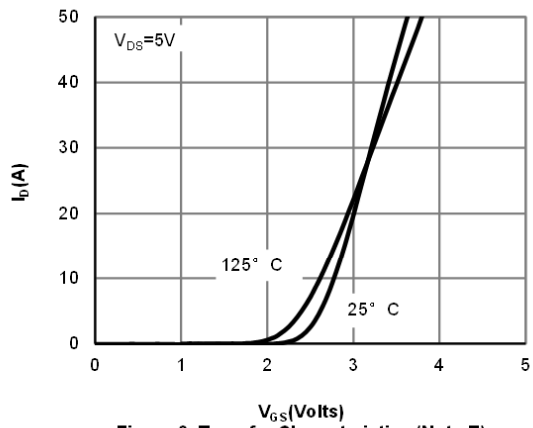


Figure 2: Transfer Characteristics (Note E)

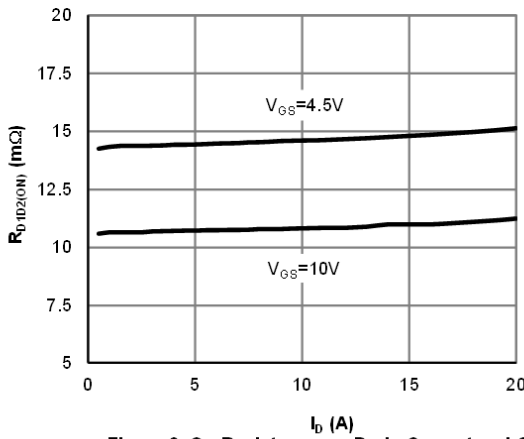


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

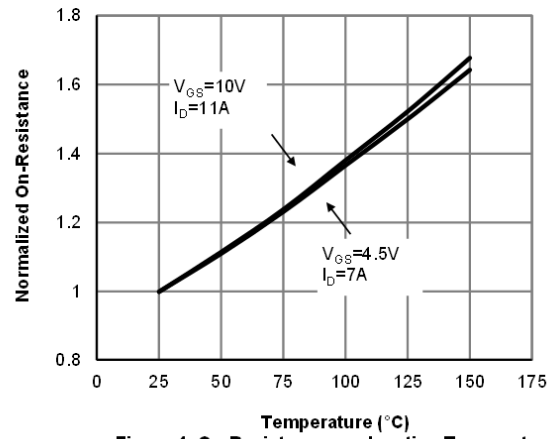


Figure 4: On-Resistance vs. Junction Temperature (Note E)

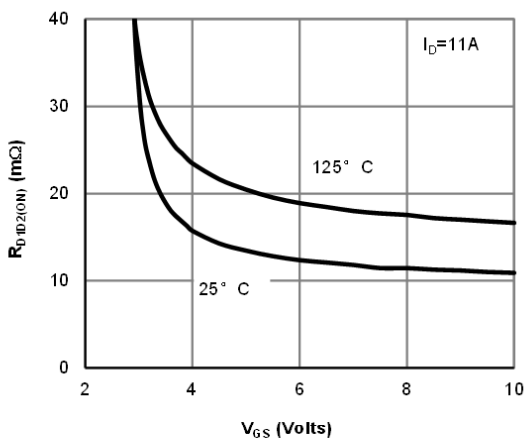


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

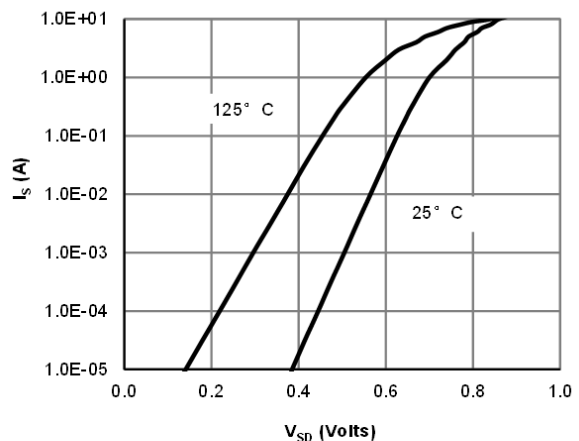


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

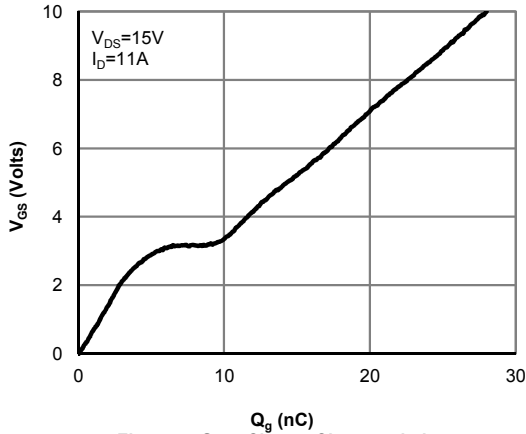


Figure 7: Gate-Charge Characteristics

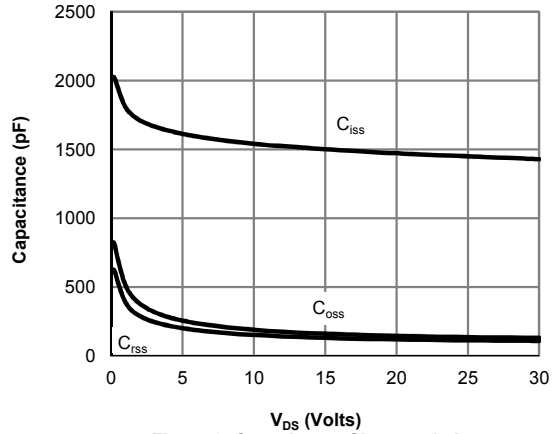


Figure 8: Capacitance Characteristics

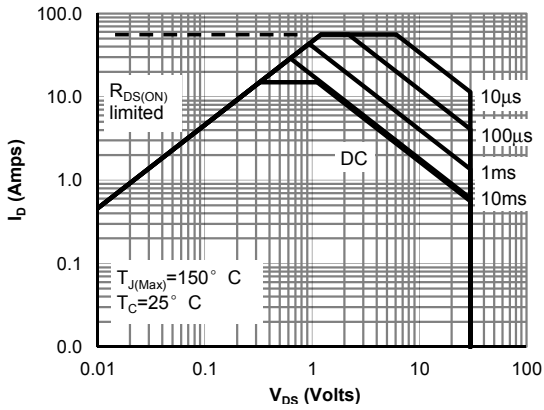


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

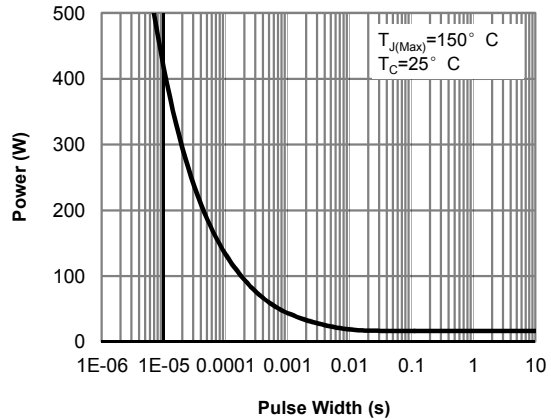


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

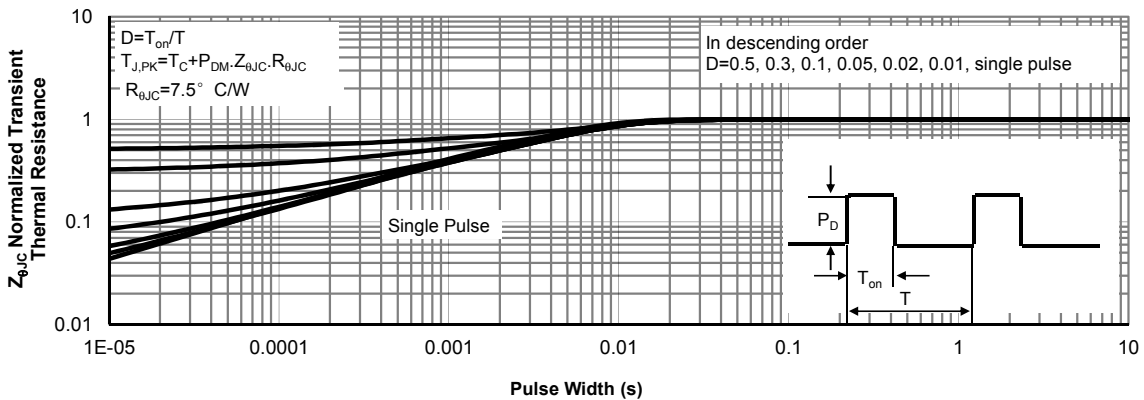


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

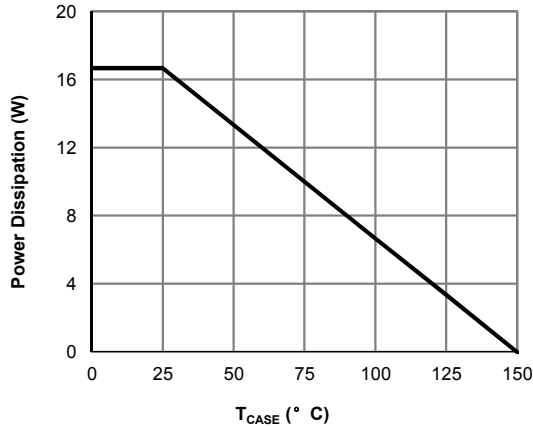


Figure 12: Power De-rating (Note F)

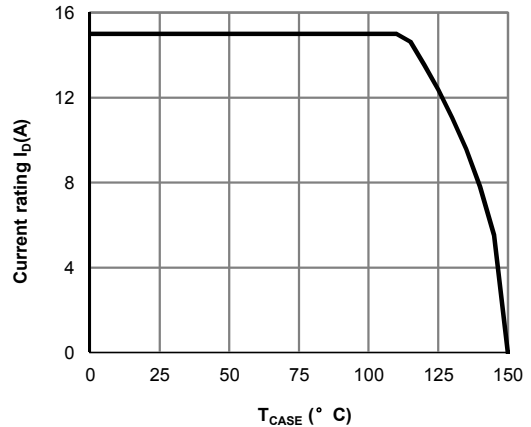


Figure 13: Current De-rating (Note F)

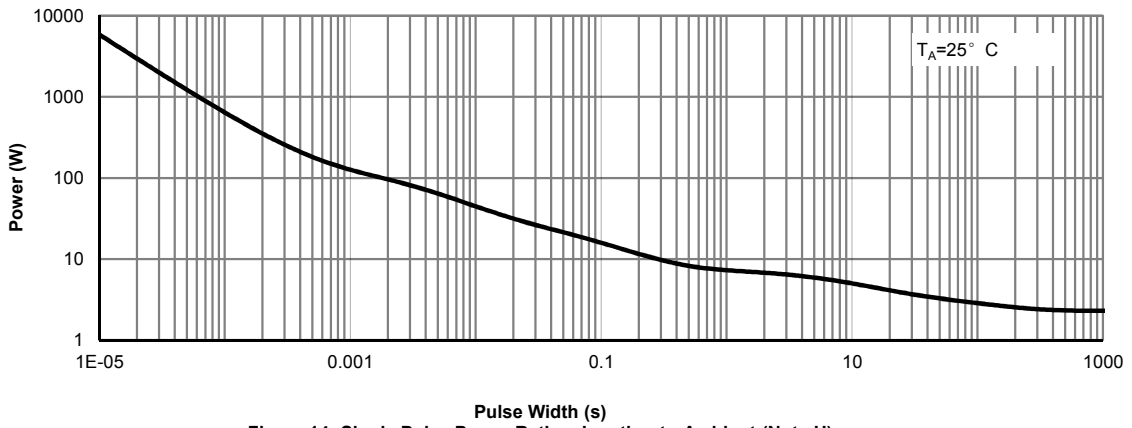


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

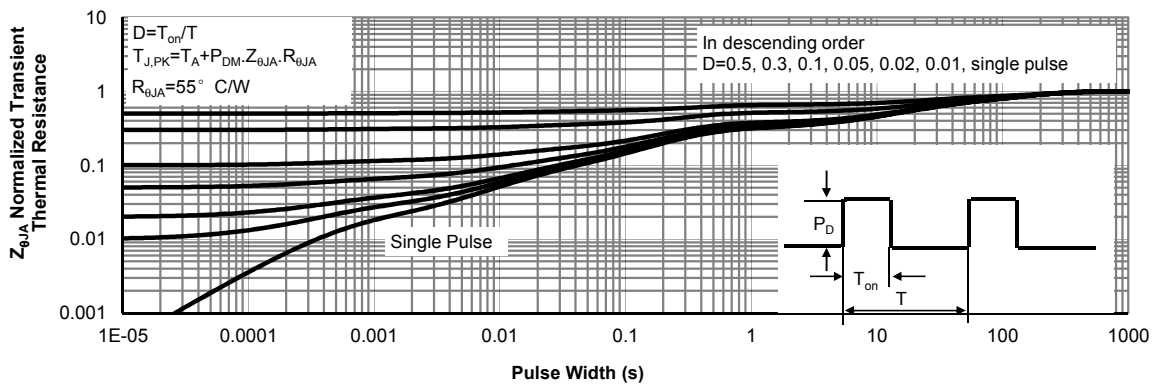
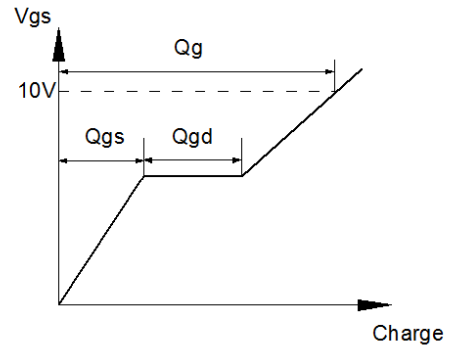
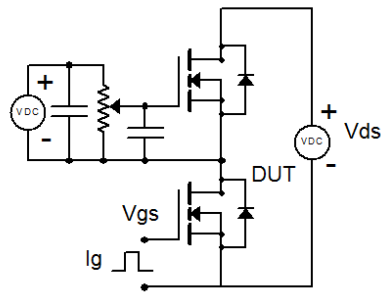
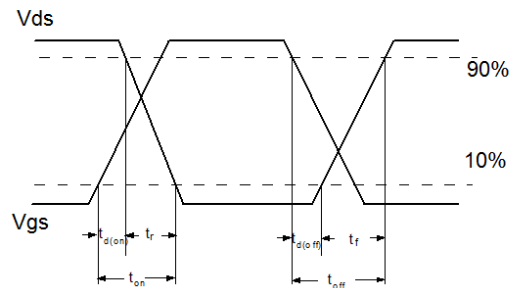
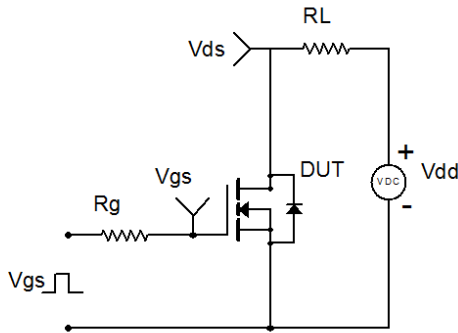


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

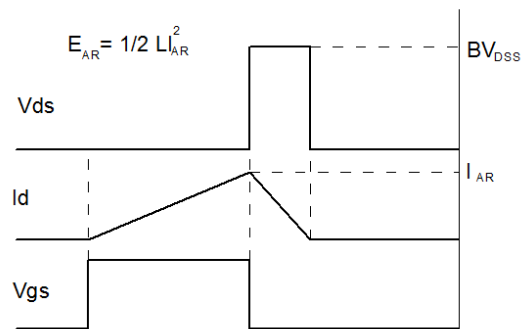
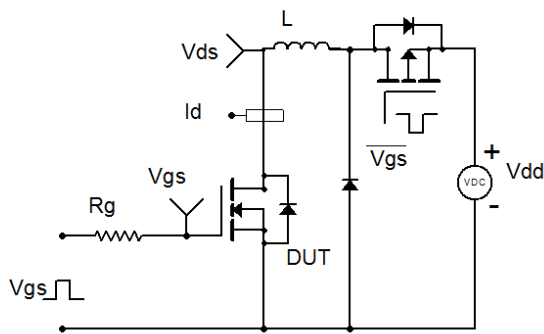
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

