

General Description

- Bottom Source Technology
- Very Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

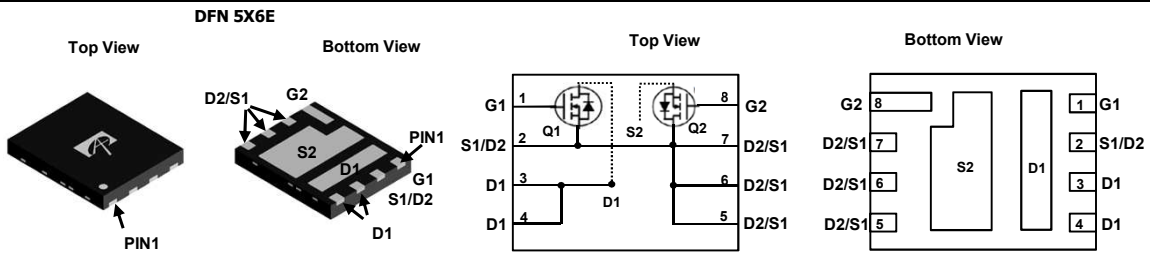
Applications

- DC/DC Converters in Computing, Servers, and POL
- Non-Isolated DC/DC Converters in Telecom and Industrial

Product Summary

	<u>Q1</u>	<u>Q2</u>
V_{DS}	25V	25V
I_D (at $V_{GS}=10V$)	62A	85A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 3.3m Ω	< 0.8m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 5m Ω	< 1.05m Ω

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONX38168	DFN 5x6E	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	V_{DS}	25	25	V
Gate-Source Voltage	V_{GS}	± 12	± 12	V
Continuous Drain Current	I_D	62	85	A
$T_C=100^\circ\text{C}$		40	67	
Pulsed Drain Current ^C	I_{DM}	190	280	
Continuous Drain Current	I_{DSM}	25	50	A
$T_A=70^\circ\text{C}$		20	41	
Avalanche Current ^C	I_{AS}	50	60	A
Avalanche energy	E_{AS}	13	18	mJ
Power Dissipation ^B	P_D	20	69	W
		8	27	
Power Dissipation ^A	P_{DSM}	3.1	3.2	W
		2	2.1	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	32	30	40	38	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient ^{A, D}		60	55	75	68	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case (Note)	$R_{\theta JC}$	4.8	1.45	6.2	1.8	$^\circ\text{C}/\text{W}$

Note: Bottom S2, D1.

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	25			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =25V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.5	1.9	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		2.7	3.3	mΩ
		V _{GS} =4.5V, I _D =20A		3.9	5	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		71		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				25	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =12.5V, f=1MHz		1150		pF
C _{oss}	Output Capacitance			460		pF
C _{rss}	Reverse Transfer Capacitance			40		pF
R _g	Gate resistance	f=1MHz	0.7	1.4	2.1	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =12.5V, I _D =20A		14	24	nC
Q _g (4.5V)	Total Gate Charge			6	12	nC
Q _{gs}	Gate Source Charge			2		nC
Q _{gd}	Gate Drain Charge			2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =12.5V, R _L =0.6Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			16.5		ns
t _{D(off)}	Turn-Off DelayTime			21		ns
t _f	Turn-Off Fall Time			2.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		22.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		37.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

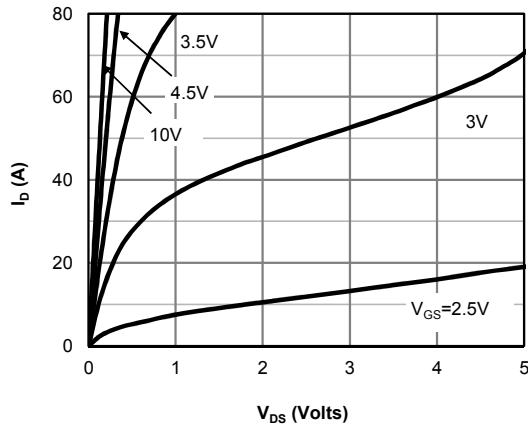


Figure 1: On-Region Characteristics (Note E)

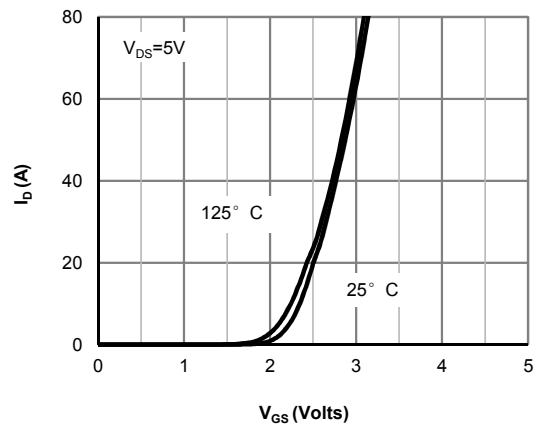


Figure 2: Transfer Characteristics (Note E)

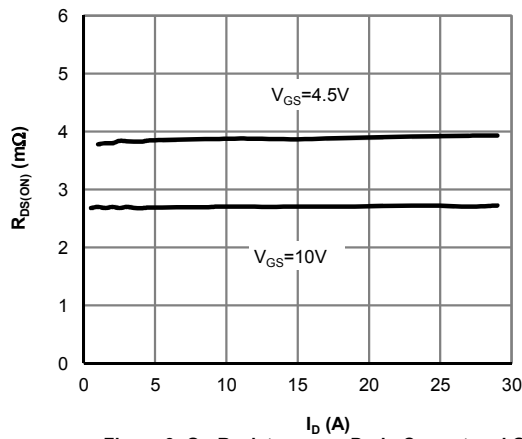


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

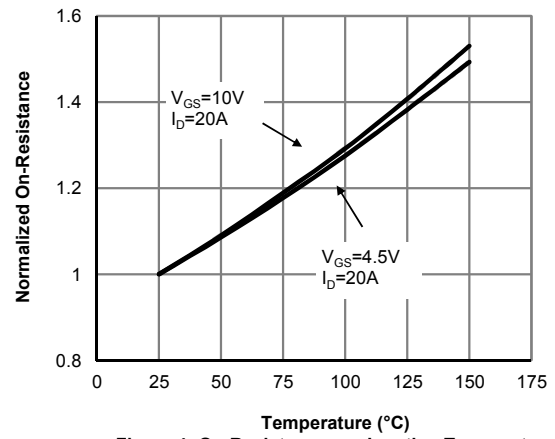


Figure 4: On-Resistance vs. Junction Temperature (Note E)

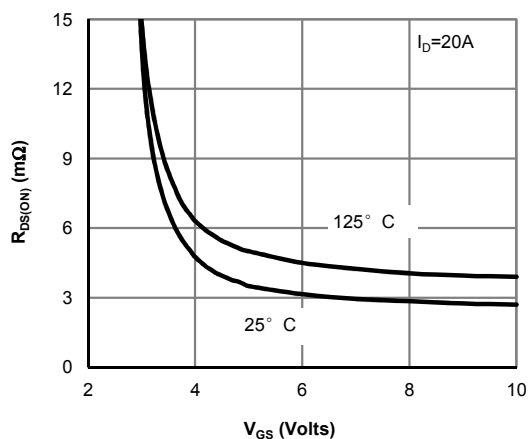


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

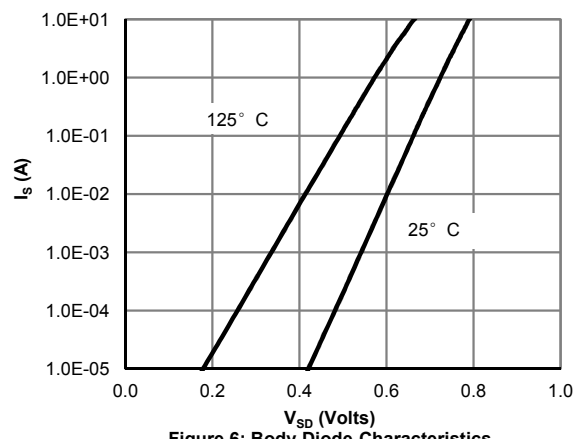


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

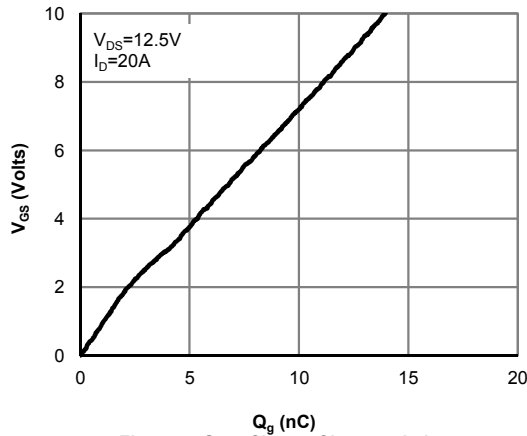


Figure 7: Gate-Charge Characteristics

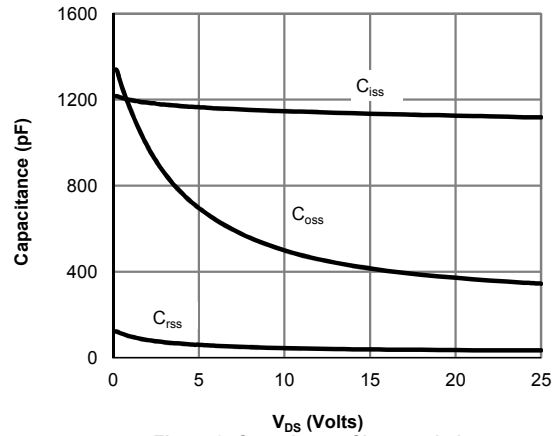


Figure 8: Capacitance Characteristics

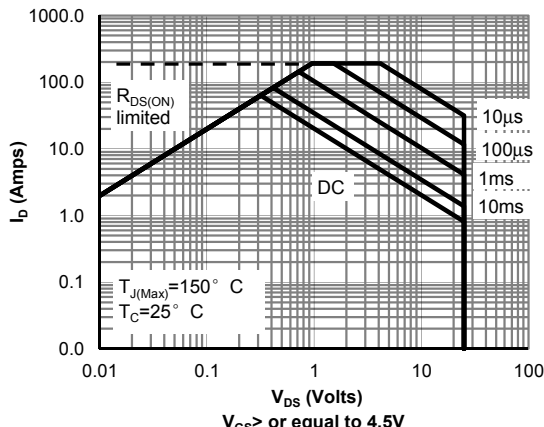


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

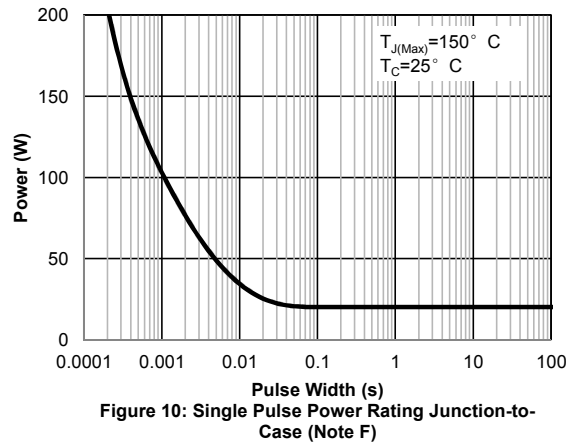


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

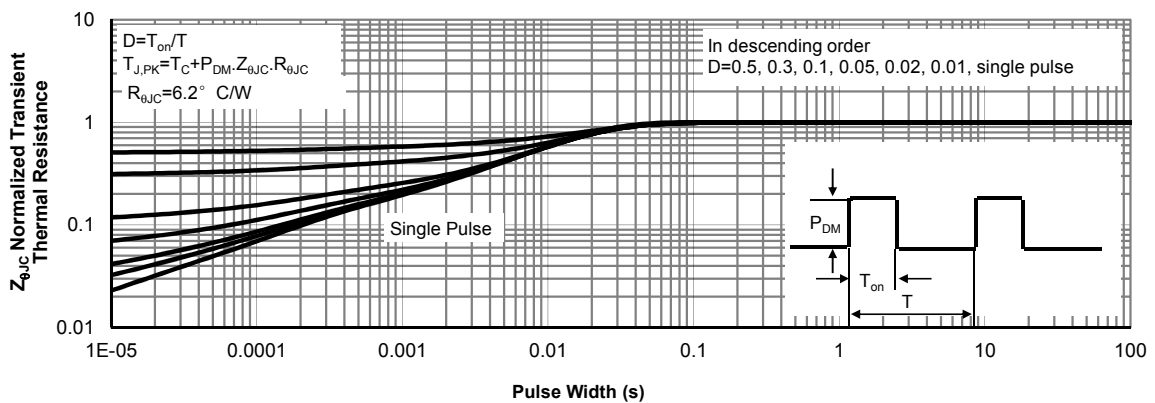


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

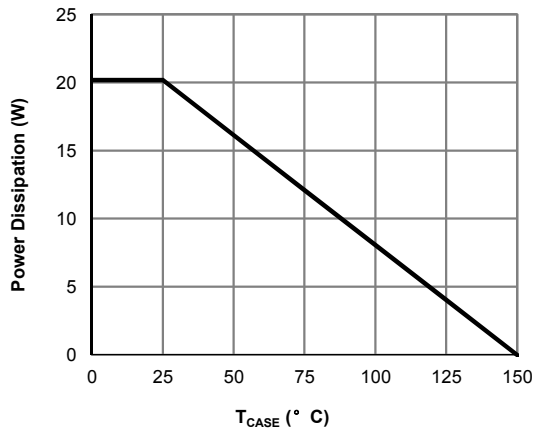


Figure 12: Power De-rating (Note F)

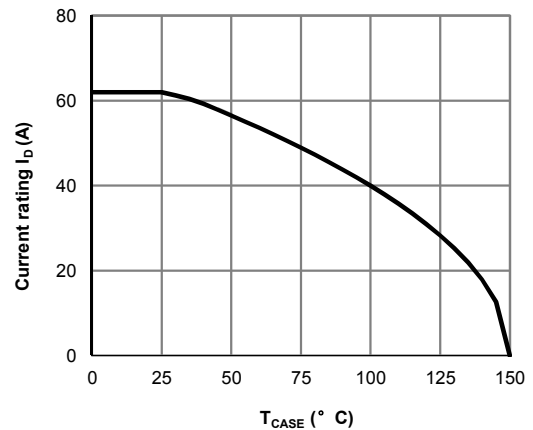


Figure 13: Current De-rating (Note F)

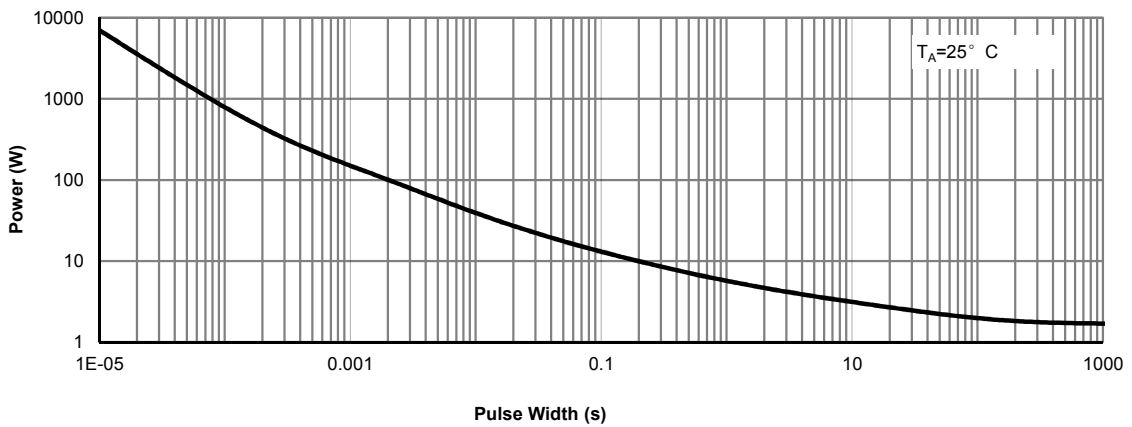


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

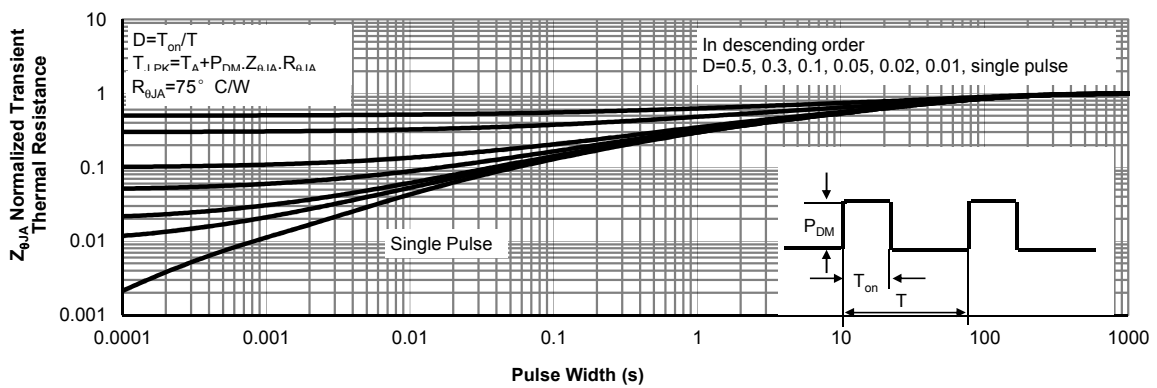


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	25			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =25V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.0	1.4	1.8	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		0.66 0.9	0.8 1.1	mΩ
		V _{GS} =4.5V, I _D =20A		0.82	1.05	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		200		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.66	1	V
I _S	Maximum Body-Diode Continuous Current ^G				85	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =12.5V, f=1MHz		4520		pF
C _{oss}	Output Capacitance			1270		pF
C _{riss}	Reverse Transfer Capacitance			170		pF
R _g	Gate resistance	f=1MHz	0.6	1.3	2	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =12.5V, I _D =20A		60	85	nC
Q _g (4.5V)	Total Gate Charge			25	35	nC
Q _{gs}	Gate Source Charge			9.6		nC
Q _{gd}	Gate Drain Charge			4.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =12.5V, R _L =0.6Ω, R _{GEN} =3Ω		7		ns
t _r	Turn-On Rise Time			19		ns
t _{D(off)}	Turn-Off DelayTime			48.5		ns
t _f	Turn-Off Fall Time			14.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		20		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		48.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

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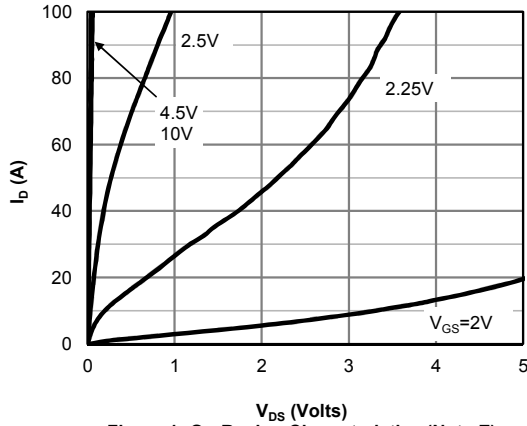


Figure 1: On-Region Characteristics (Note E)

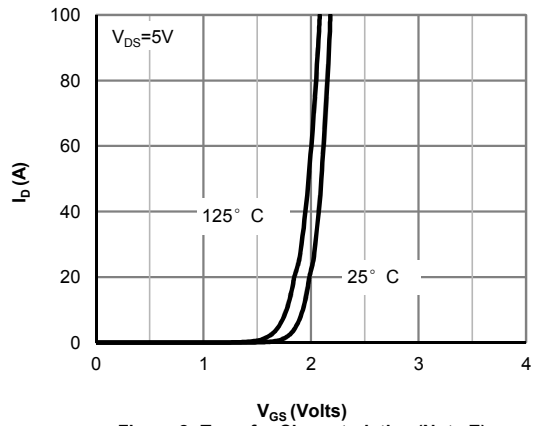


Figure 2: Transfer Characteristics (Note E)

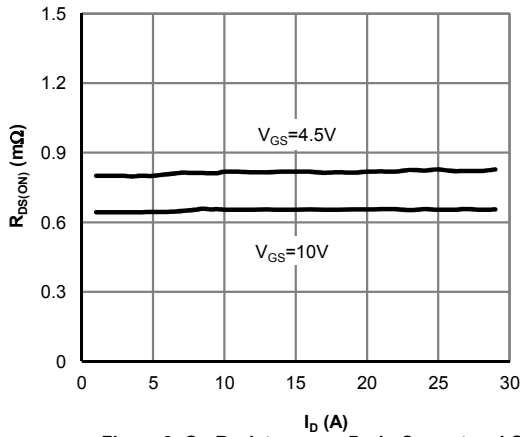


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

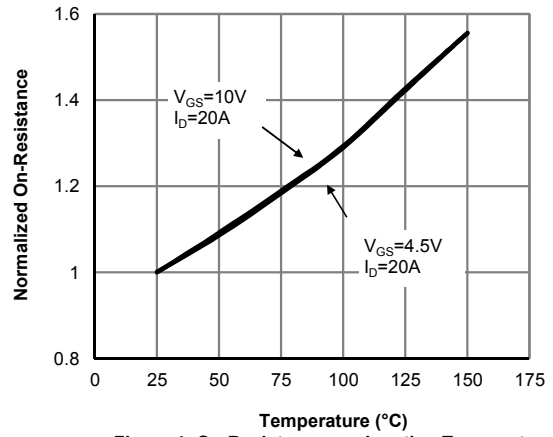


Figure 4: On-Resistance vs. Junction Temperature (Note E)

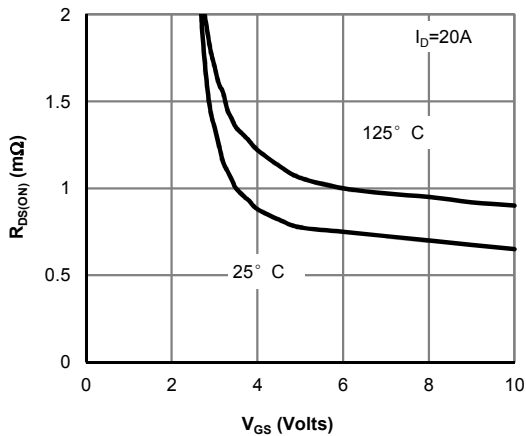


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

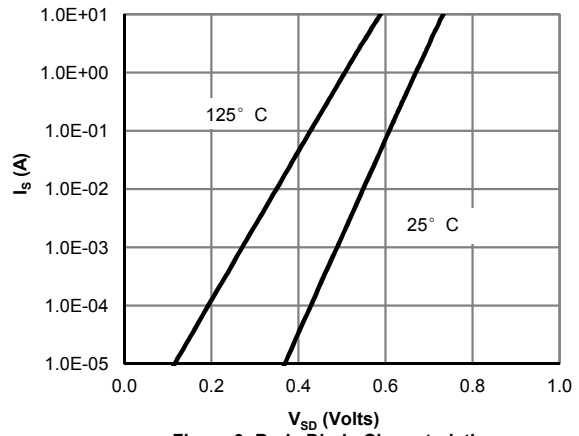


Figure 6: Body-Diode Characteristics (Note E)

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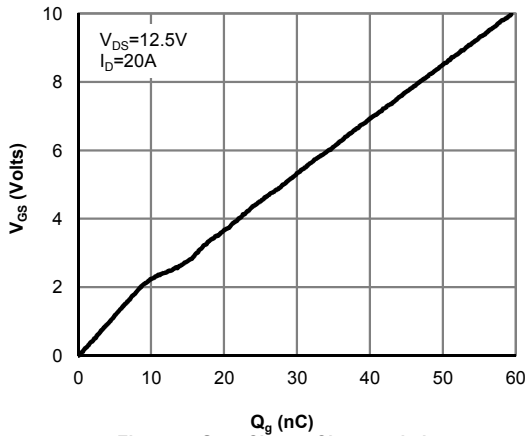


Figure 7: Gate-Charge Characteristics

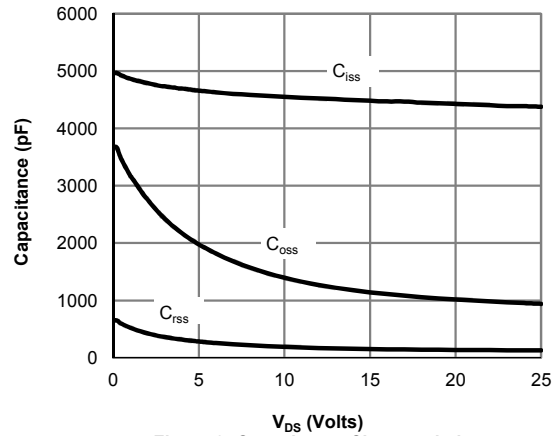


Figure 8: Capacitance Characteristics

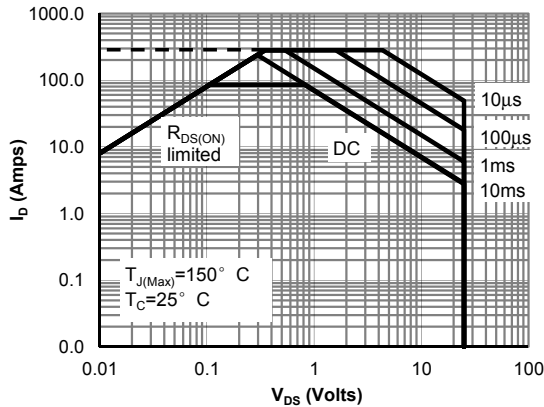


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

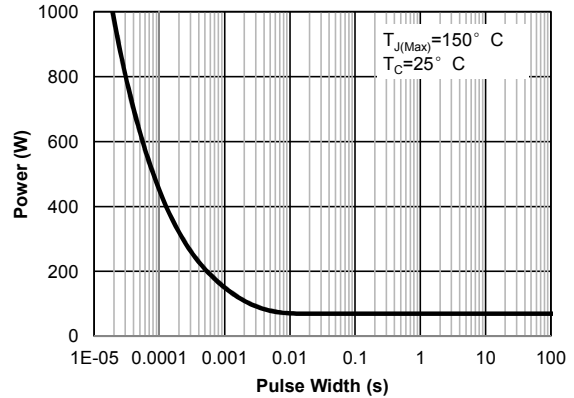


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

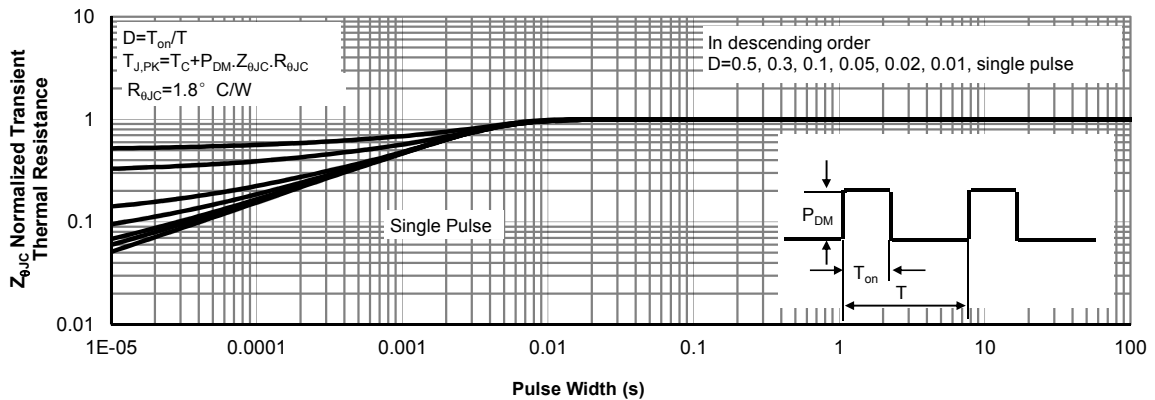


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

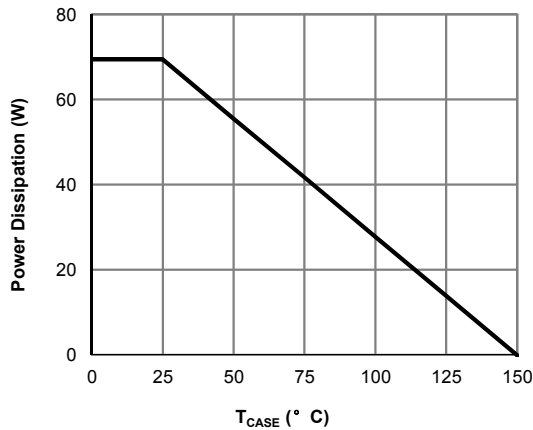


Figure 12: Power De-rating (Note F)

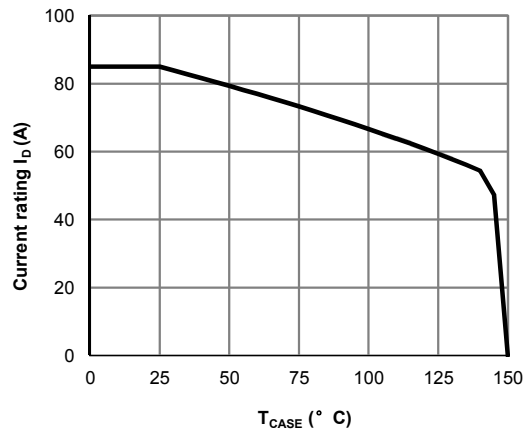


Figure 13: Current De-rating (Note F)

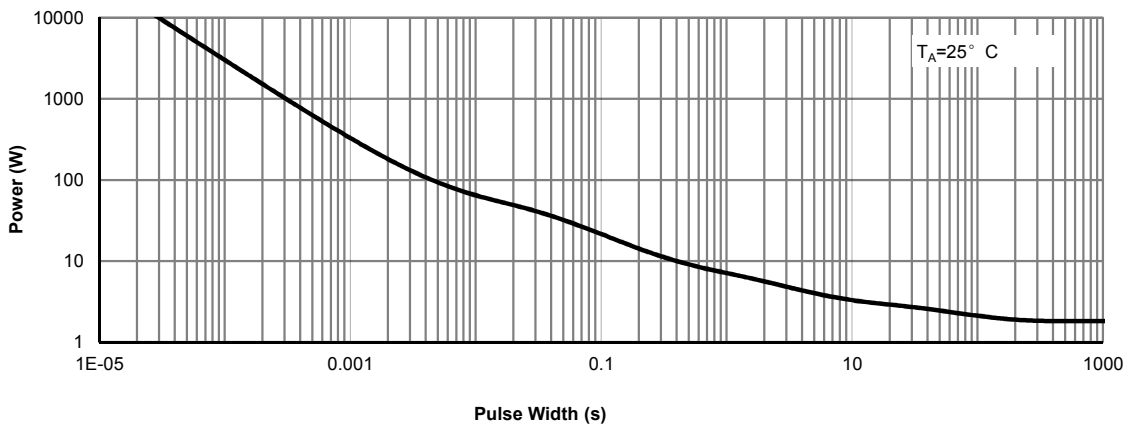


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

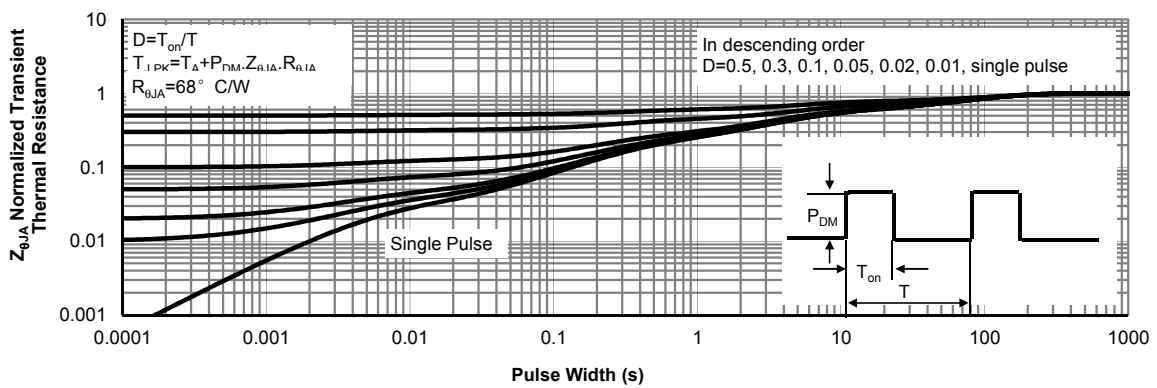


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

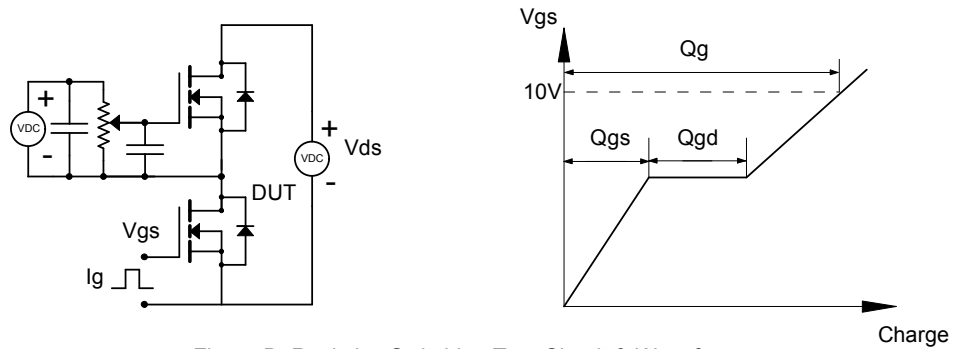


Figure B: Resistive Switching Test Circuit & Waveforms

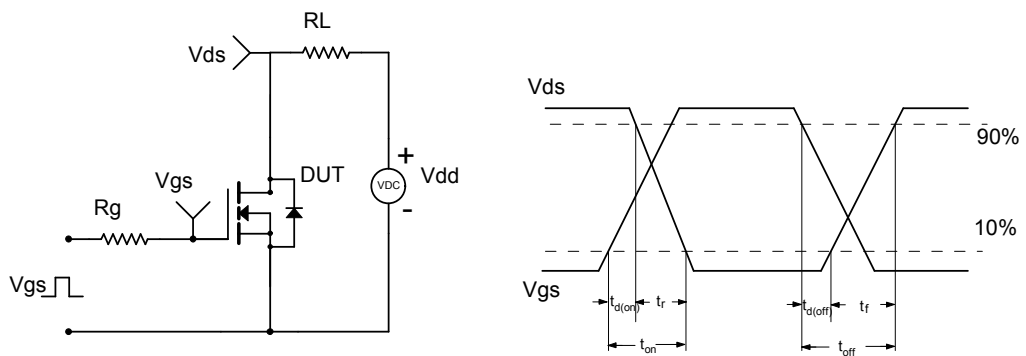


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

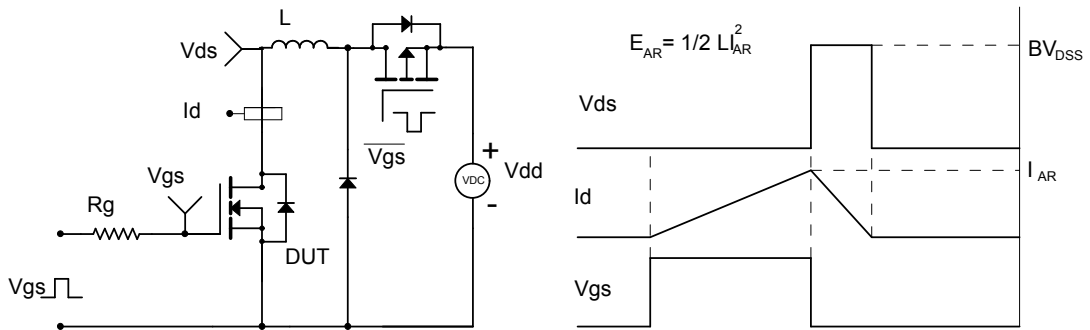


Figure D: Diode Recovery Test Circuit & Waveforms

