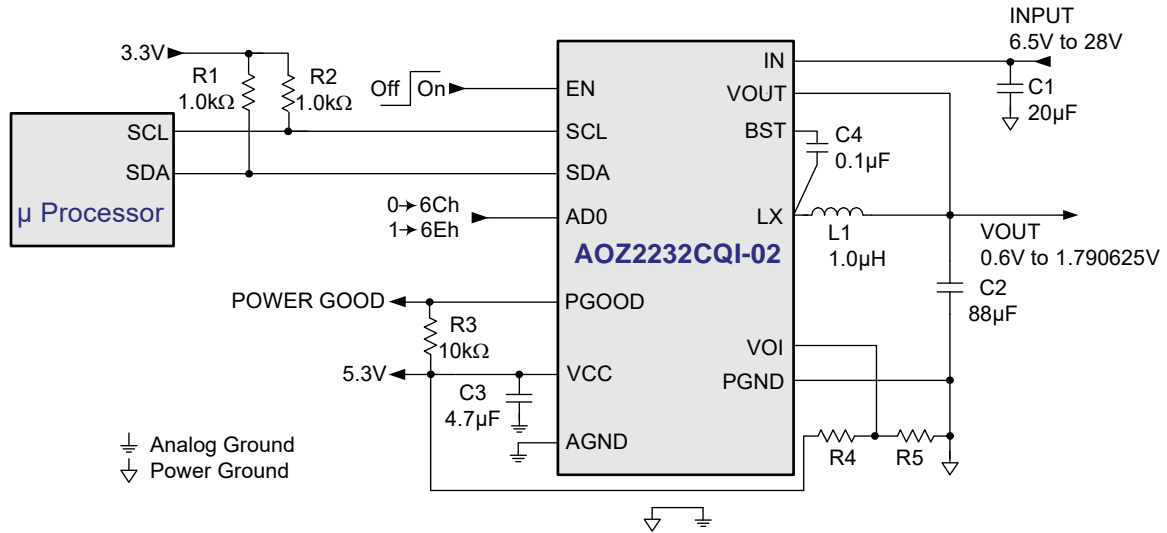


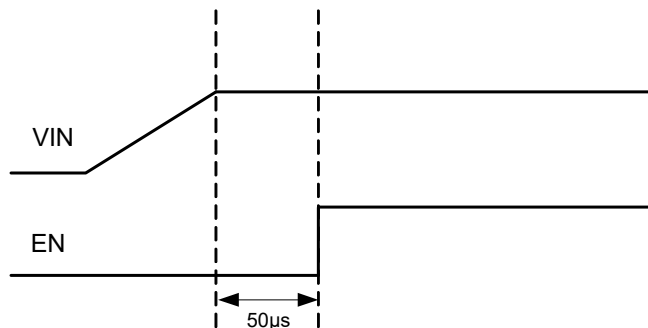
Typical Application



Option Table

| Code \ Item | AD0 | Address (Binary) | Address (Hex) |
|---------------|------------|------------------|---------------|
| AOZ2232CQI-01 | Ground (0) | 01101000 | 68h |
| | Open (1) | 01101010 | 6Ah |
| AOZ2232CQI-02 | Ground (0) | 01101100 | 6Ch |
| | Open (1) | 01101110 | 6Eh |

Recommended Start-up Sequence



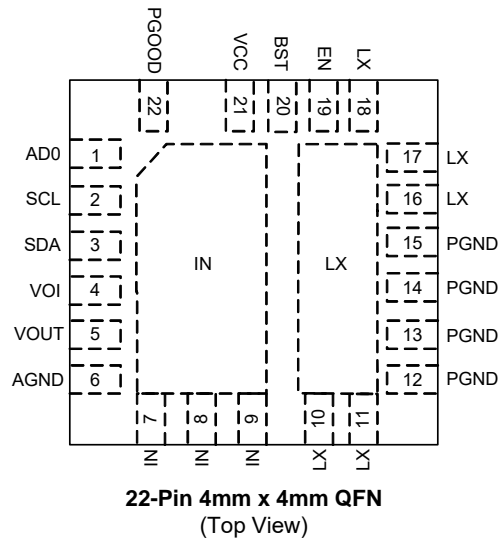
Ordering Information

| Part Number | Ambient Temperature Range | Package | Environmental |
|---------------|---------------------------|----------------------|---------------|
| AOZ2232CQI-02 | -40°C to +85°C | 22-Pin 4mm x 4mm QFN | Green Product |



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|--------------------|----------|---|
| 1 | AD0 | Chip Address. The AD0 pin just connects to AOZ2232CQI-02 VCC pin or GND. |
| 2 | SCL | Clock I/O Terminal. |
| 3 | SDA | Data I/O Terminal. |
| 4 | VOI | Initial Output Voltage Feedback Input. Adjust the output voltage with a resistive voltage-divider between VCC and AGND. |
| 5 | VOUT | Output Voltage Feedback Input. Connection to output voltage. |
| 6 | AGND | Analog Ground. |
| 7, 8, 9 | IN | Supply Input. IN is the regulator input. All IN pins must be connected together. |
| 10, 11, 16, 17, 18 | LX | Switching Node. |
| 12, 13, 14, 15 | PGND | Power Ground. |
| 19 | EN | Enable Input. The AOZ2232CQI-02 is enabled when EN is pulled high. The device shuts down when EN is pulled low. |
| 20 | BST | Bootstrap Capacitor Connection. The AOZ2232CQI-02 includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in Typical Application diagram. |
| 21 | VCC | Supply Input for Analog Functions. Bypass VCC to AGND with a 1 μ F~4.7 μ F ceramic capacitor. Place the capacitor close to VCC pin. |
| 22 | PGOOD | Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down. |

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

| Parameter | Rating |
|--|-----------------|
| IN to AGND | -0.3V to 30V |
| LX to AGND ⁽¹⁾ | -0.3V to 30V |
| BST to AGND | -0.3V to 36V |
| PGOOD, EN, VCC, SCL, SDA, VOUT, VOI, AD0 to AGND | -0.3V to 6V |
| PGND to AGND | -0.3V to +0.3V |
| Junction Temperature (T _J) | +150°C |
| Storage Temperature (T _S) | -65°C to +150°C |
| ESD Rating ⁽²⁾ | 2kV |

Notes:

- LX to PGND Transient (t<20ns) ----- -7V to V_{IN}+7V.
- Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Electrical Characteristics

T_A = 25°C, V_{IN}=12V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|----------------------|--|--|------------|--------------------------|------------|------------------|
| V _{IN} | IN Supply Voltage | | 6.5 | | 28 | V |
| V _{UVLO} | Under-Voltage Lockout Threshold of V _{CC} | V _{CC} rising V _{CC} falling | 3.7 | 4.2 3.9 | 4.4 | V |
| I _q | Quiescent Supply Current of V _{CC} | I _{OUT} = 0, V _{EN} ≥ 2V, PFM mode | | 0.5 | | mA |
| I _{OFF} | Shutdown Supply Current | V _{EN} = 0V | | 1 | 20 | μA |
| V _{OUT} | Output Voltage | T _A = 25°C, V _{IN} =12V V _{OUT} = 0.6 to 1.790625V, L= 1μH | -2% | 0% | 2% | V _{OUT} |
| V _{OUT} | Output Voltage | T _A = 25°C, V _{IN} =12V, V _{OUT} =0.9 to 1.125V, L=1uH | -1.5% | 0% | 1.5% | V _{OUT} |
| T _{r_OUT} | Output Voltage Rising Time | V _{OUT} = 0.9V to 1.3V, C _{OUT} = 88μF, PWM mode | 2.5 | | 15 | μs |
| T _{f_OUT} | Output Voltage Falling Time | V _{OUT} = 1.3V to 0.9V, C _{OUT} = 88μF, PWM mode | 2.5 | | 15 | μs |
| Enable | | | | | | |
| V _{EN} | EN Input Threshold | Off threshold On threshold | 1.4 | | 0.5 | V V |
| V _{EN_HYS} | EN Input Hysteresis | | | 100 | | mV |
| AD0 | | | | | | |
| V _{AD0} | AD0 Input Threshold | Off threshold On threshold | 4.2 | | 0.5 | V V |
| Modulator | | | | | | |
| f _{SW} | Operating Frequency | | | 400 | | kHz |
| T _{ON_MIN} | Minimum On Time | | | 100 | | ns |
| T _{ON_MAX} | Maximum On Time | | | 2.6 | | μs |
| T _{OFF_MIN} | Minimum Off Time | | | 300 | | ns |

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating ratings.

| Parameter | Rating |
|--|--------------------|
| Supply Voltage (V _{IN}) | 6.5V to 28V |
| Output Voltage Range | 0.6 V to 1.790625V |
| Ambient Temperature (T _A) | -40°C to +85°C |
| Package Thermal Resistance (θ _{JA}) (θ _{JC}) | 32°C/W 4°C/W |

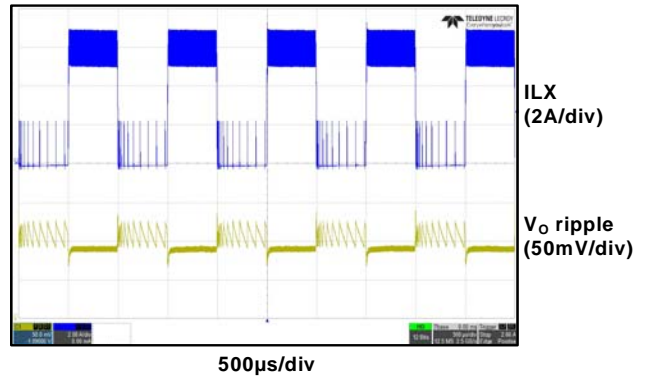
Typical Performance Characteristics

Circuit of Typical Application. $T_A = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $V_{OUT} = 1\text{V}$, $f_s = 400\text{kHz}$ unless otherwise specified.

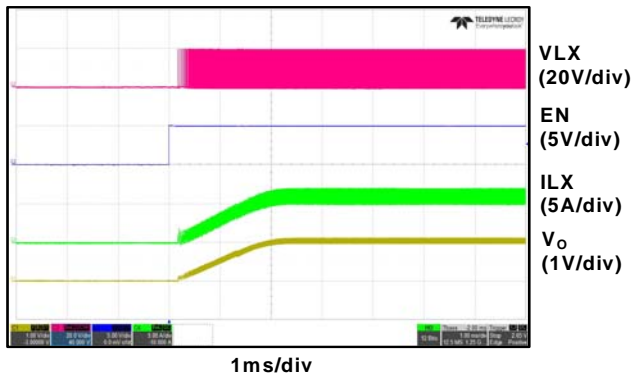
Normal Operation



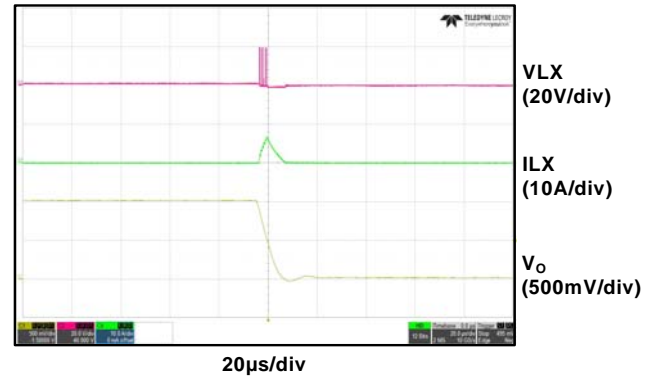
Load Transient 0A to 6A



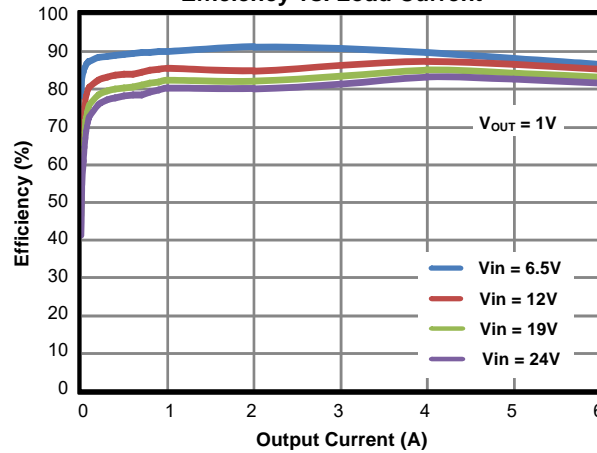
Full Load Start-up



Short Circuit Protection



Efficiency vs. Load Current



I²C Control Specification⁽³⁾⁽⁴⁾⁽⁵⁾

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---------------------|---|------------|----------------------|------|-----|-------|
| V _{IL} | Low level input voltage | | | | 0.6 | V |
| V _{IH} | High level input voltage | | 2.9 | | | V |
| V _{hys} | Hysteresis of Schmitt trigger inputs | | 0.11 | | | V |
| V _{OL} | Low level output voltage (Open drain, 3mA sink current) | | | | 0.4 | V |
| T _{SP} | Pulse width of spikes suppressed by input filter | | 32 | | | ns |
| f _{SCL} | SCL clock frequency | | | | 400 | kHz |
| t _{HD;STA} | Hold time (repeated), START condition | | 0.6 | | | μs |
| t _{LOW} | Low period of SCL clock | | 1.3 | | | μs |
| t _{HIGH} | High period of SCL clock | | 0.6 | | | μs |
| t _{SU;STA} | Set-up time for a repeated START condition | | 0.6 | | | μs |
| t _{HD;DAT} | Data hold time | | 50 | | 900 | ns |
| t _{SU;DAT} | Data set-up time | | 100 | | | ns |
| t _r | Rise time (SDA or SCL) | | 20+0.1C _b | | 300 | ns |
| t _f | Fall time (SDA or SCL) | | 5+0.1C _b | | 300 | ns |
| t _{SU;STO} | Set-up time for STOP condition | | 0.6 | | | μs |
| t _{BUF} | Bus free time between STOP and START conditions | | 1.3 | | | μs |
| C _b | Capacitive load for each bus line | | | | 400 | pF |
| I _d | SDA driver capability | | 25 | | 100 | mA |

Notes:

3. Ensured by design. Not production tested.
4. Refer to Figure 1 for I²C timing definitions.
5. C_b = capacitance of bus line in pF.

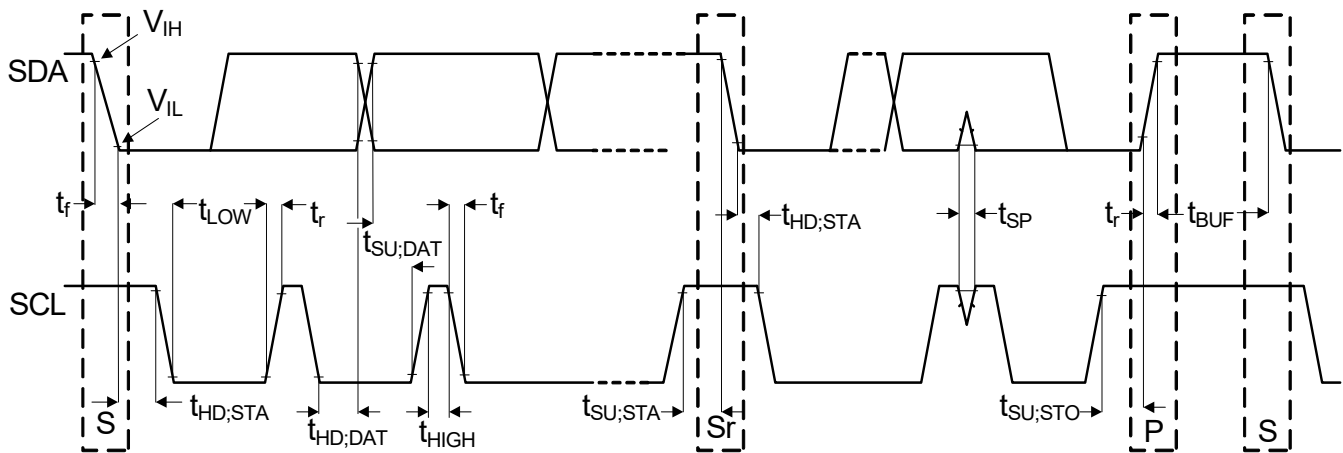


Figure 1. I²C Timing Definitions

I²C Register Maps

| Register Name | Register Address | Bit 7 | Bit6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|------------------|---------------|----------------------|-------|-----------------------|-------|-------|-------|-----------------|
| Output Voltage | 00 | Odd Parity | Output Voltage [6:0] | | | | | | |
| Control A | 01 | Internal Mode | | | Output Voltage Change | PFMb | | | Protection Mode |

Summary of Default Control Bits⁽⁶⁾

| Control Bit(s) | Default | Function |
|-----------------------|-------------------|--|
| VOUT [6:0] | 0110010 | VOUT code, 7 bits VOUT [6:0]. Part default to 1.068750V. |
| Internal Mode | 0 (External Mode) | 0 case: External Mode 1 case: Internal Mode (1). If set to 1, the part switches to internal mode and VOUT register value controls output voltage. (2). The part can be set back to external control mode at any time by wiring this bit to 0. |
| Output Voltage Change | 0 | 0 case: Internal protection on 1 case: Internal protection off (1). If set to 0, when VOUT code change, the internal protection isn't turned off. (2). If set to 1, when VOUT code change, the internal protection is turned off to avoid triggering internal protection. |
| PFMb | 1 | Select PFM or PWM at light load. 0 case: PFM 1 case: PWM Part defaults to PWM. |
| Protection Mode | 1 | Select Latch-off or Auto-recovery for protection. 0 case: Auto-recovery mode 1 case: Latch-off mode Part defaults to Latch-off mode. |

Note:

6. When the system satisfies any of the following conditions, the I²C register will be reset to default settings:

- (1) No input voltage
- (2) LDO VCC is less than VCC UVLO falling threshold.
- (3) EN signal is disabled

Odd Parity Bit

The odd parity bit is set by the Master controller to be the exclusive-NOR of the output voltage [6:0] bits. It will be used by the AOZ2232CQI-02 to check that a valid data byte has been received. If odd parity is not equal to the exclusive-NOR of the output voltage [6:0] bits, the

AOZ2232CQI-02 assumes that an error has been occurred during the data transmission, and it will not send an ACK bit, nor will it reset the VOUT to the received code. (or, if the Control register will not reset the register contents as requested). The Master should try again to re-send the data. When reading back the VOUT register, the parity bit is sent back.

