

General Description

The AOZ32033AQI is an integrated half-bridge solution with intelligent slew-rate control for wireless charger application. The device includes the high-side, low-side N-channel MOSFETs and its driver circuit. Typically, it's dedicated for the design of wireless charger transmitter circuit which is composed of full-bridge topology with resonant tank circuit to get best efficiency of power converter.

The AOZ32033AQI provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance. Moreover, the features of AOZ32033AQI have multiple protection functions such as V_{CC} UVLO, over temperature protection to make the design more robust.

The AOZ32033AQI is available in a 3mm×3mm QFN-18L package and is rated over a -40°C to +85°C ambient temperature range.

Features

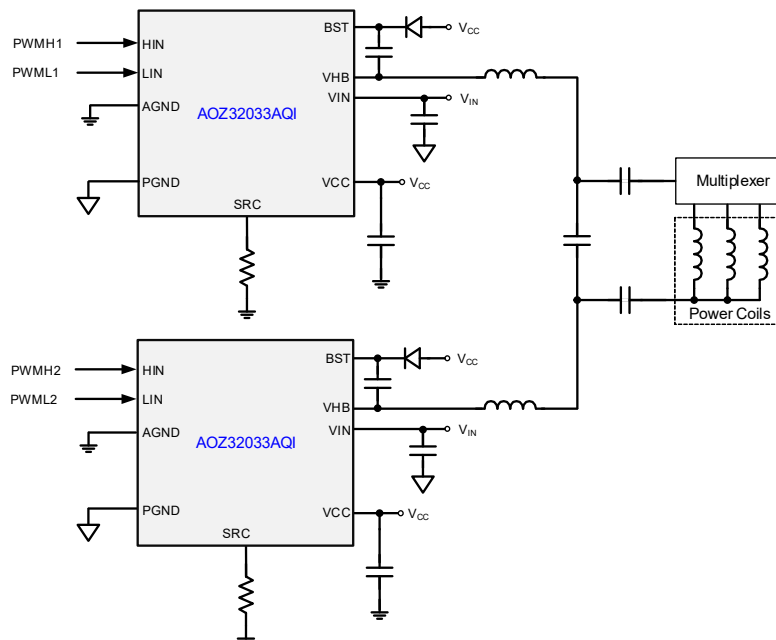
- Maximum input voltage 30V
 - Support 12V & 24V voltage rail system
- 15W~30W coil driver
 - For wireless charger transmitter circuit
- Slew-rate control to improve EMI performance
- Integrated bootstrap diode
- Support protectiond
 - OTP, UVLO
- Thermally enhanced 18-pin 3×3 QFN

Applications

- Wireless charger TX



Typical Application (Wireless Charger TX)



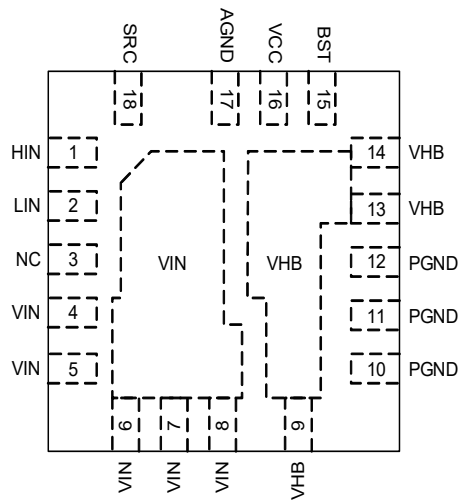
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32033AQI	-40°C to +85°C	18-Pin 3x3 QFN	Green



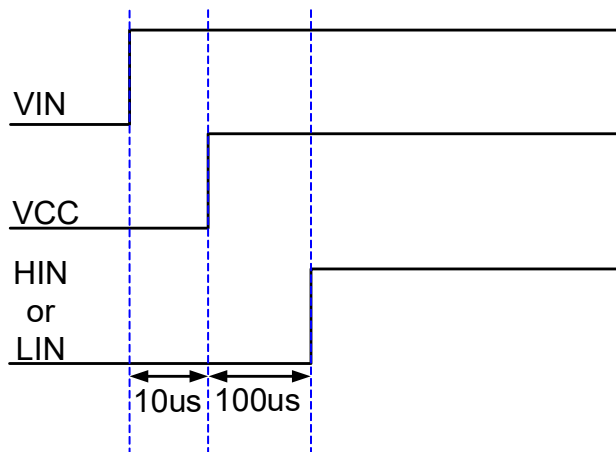
All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit <http://www.aosmd.com/media/AOSGreenPolicy.pdf> for additional information.

Pin Configuration



18-Pin 3mm x 3mm QFN

Start-up Sequence



Pin Description

Pin Number	Pin Name	Pin Function
1	HIN	PWM Input for High-Side MOSFET.
2	LIN	PWM Input for Low-Side MOSFET.
3	NC	No connect
4, 5, 6, 7, 8	VIN	Supply Input. All VIN pins must be connected together.
9, 13, 14	VHB	Switching Node for Half-Bridge. All VHB must be connected together.
10, 11, 12	PGND	Power Ground.
15	BST	Bootstrap Capacitor Connection. Connect an external capacitor between BST and VHB for supplying high-side MOSFET.
16	VCC	Supply Input for Analog Functions. Bypass VCC to AGND with a 0.1uF~10uF ceramic capacitor and as close to VCC pin as possible
17	AGND	Analog Ground.
18	SRC	Slew-Rate Control to Adjust Driver Speed of Internal MOSFET.

Absolute Maximum Ratings⁽¹⁾

Parameter	Rating
V _{IN} to AGND	-0.3V to 30V
V _{HB} to AGND	-0.3V to 30V
B _{ST} to AGND	-0.3V to 40V
B _{ST} to V _{HB}	-0.3 to 6V
S _{RC} , V _{CC} to AGND	-0.3V to 6V
P _{GND} to AGND	-0.3V to +1V
Junction Temperature (T _J)	+150°C
Storage Temperature (T _S)	-65°C to +150°C
ESD Rating	±2kV

Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating ratings.

Recommend Operating Ratings⁽²⁾

Parameter	Rating
Supply Voltage (V _{IN})	3.8V to 30V
Supply Voltage (V _{CC})	4.75V to 5.5V
Ambient Temperature (T _A)	-40°C to +85°C
Package Thermal Resistance (θ _{JA}) (θ _{JC})	40°C/W 0.6°C/W

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise specified.

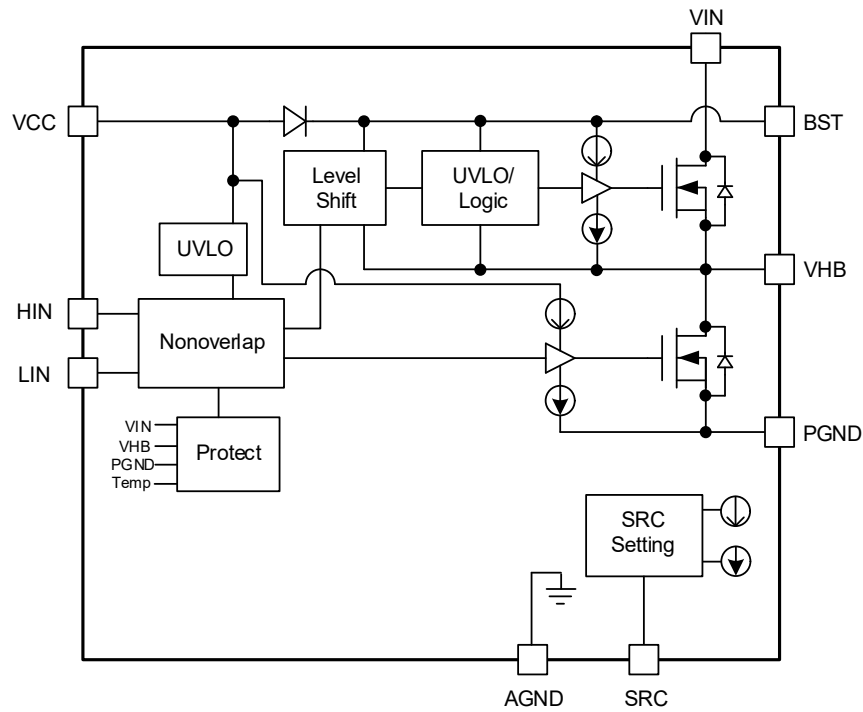
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{UVLO_R}	V _{CC} UVLO Rising	V _{IN} =12V, V _{CC} increase, Monitor SRC from low to high		4.3		V
V _{UVLO_F}	V _{CC} UVLO Falling	V _{IN} =12V, V _{CC} decrease, Monitor SRC from high to low		4.2		V
V _{B_UVLO_R}	V _{BST} -V _{HB} UVLO Rising	V _{IN} =20V, (V _{BST} -V _{HB}) increase, Monitor V _{HB} from low to high		4.3		V
V _{B_UVLO_F}	V _{BST} -V _{HB} UVLO Falling	V _{IN} =20V, (V _{BST} -V _{HB}) decrease, Monitor V _{HB} from high to low		4.2		V
I _{VIN_QC}	I _{VIN} Quiescent Current	V _{IN} =12V, V _{CC} =5V, HIN=LIN=0V, SRC=100kΩ		30		μA
I _{VCC_QC}	I _{VCC} Quiescent Current	V _{IN} =12V, V _{CC} =5V, HIN=LIN=0V, SRC=100kΩ		200		μA
I _{BST-VHB_QC}	I _{BST-VHB} Quiescent Current	HIN/LIN=0V, V _{HB} =1V, (V _{BST} -V _{HB})=5V, Monitor (V _{BST} -V _{HB}) Current			0.2	mA
V _{H_{LIN}_L}	HIN/LIN Logic Low Voltage	V _{IN} =12V	0		1.2	V
V _{H_{LIN}_H}	HIN/LIN Logic High Voltage	V _{IN} =12V	2.2		5.5	V
R _{H_{LIN}_IN}	HIN/LIN Input Pull Low Impedance			280		kΩ
t _{H_{LIN}_RP}	HIN Rising Propagation Delay	V _{IN} =10V, V _{CC} =5V, SRC=20kΩ, V _{HB} to GND=100Ω, HIN=Low to High, Monitor V _{HB} Low to High		55		ns
t _{H_{LIN}_FP}	HIN Falling Propagation Delay	V _{IN} =10V, V _{CC} =5V, SRC=20kΩ, V _{HB} to GND=100Ω, HIN=High to Low, Monitor V _{HB} High to Low		75		ns
t _{L_{LIN}_RP}	LIN Rising Propagation Delay	V _{IN} =10V, V _{CC} =5V, SRC=20kΩ, V _{HB} to VIN=100Ω, LIN=Low to High, Monitor V _{HB} High to Low		45		ns
t _{L_{LIN}_FP}	LIN Falling Propagation Delay	V _{IN} =10V, V _{CC} =5V, SRC=20kΩ, V _{HB} to VIN=100Ω, LIN=High to Low, Monitor V _{HB} Low to High		70		ns

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T _{DM_R}	Delay Matching Rising	Difference between t _{HIN_RP} and t _{LIN_RP}		10		ns
T _{DM_F}	Delay Matching Falling	Difference between t _{HIN_FP} and t _{LIN_FP}		5		ns
V _{SRC}	SRC	V _{IN} =12V, V _{CC} =5V, SRC=20kΩ	0.97	1	1.03	V
I _{SRC_MIN}	SRC Min. Source Current	V _{IN} =12V, V _{CC} =5V, SRC=4V		0.5		μA
I _{SRC_MAX}	SRC Max. Source Current	V _{IN} =12V, V _{CC} =5V, SRC=0.8V		140		μA
SR _{HIN_R}	HIN Rising Slew Rate (SRC=20kΩ)	V _{IN} =10V, V _{CC} =5V, V _{HB} to GND=100Ω, HIN=Low to High, Monitor V _{HB} Rising Slew Rate		0.85		V/ns
SR _{HIN_F}	HIN Falling Slew Rate (SRC=20kΩ)	V _{IN} =10V, V _{CC} =5V, V _{HB} to GND=100Ω, HIN=High to Low, Monitor V _{HB} Falling Slew Rate		0.06		V/ns
SR _{LIN_R}	LIN Rising Slew Rate (SRC=20kΩ)	V _{IN} =10V, V _{CC} =5V, V _{HB} to V _{IN} =100Ω, LIN=High to Low, Monitor V _{HB} Rising Slew Rate		0.07		V/ns
SR _{LIN_F}	LIN Falling Slew Rate (SRC=20kΩ)	V _{IN} =10V, V _{CC} =5V, V _{HB} to V _{IN} =100Ω, LIN=Low to High Monitor V _{HB} Falling Slew Rate		1.3		V/ns
R _{H_ON}	V _{IN} -V _{HB} RON	V _{IN} =12V, V _{CC} =5V, HIN=5V, (V _{BST} -V _{HB})=5V, I _{VHB} =1A		11		mΩ
R _{L_ON}	V _{HB} -PGND RON	V _{IN} =12V, V _{CC} =5V, LIN=5V, PGND=0, I _{VHB} =1A		11		mΩ
V _{SD}	Boost Diode Forward Voltage	Forward Current = 2mA		0.4		V
T _{OTP}	OTP	V _{IN} =12V, V _{CC} =5V		150		°C

Functional Block Diagram



Typical Performance Characteristics

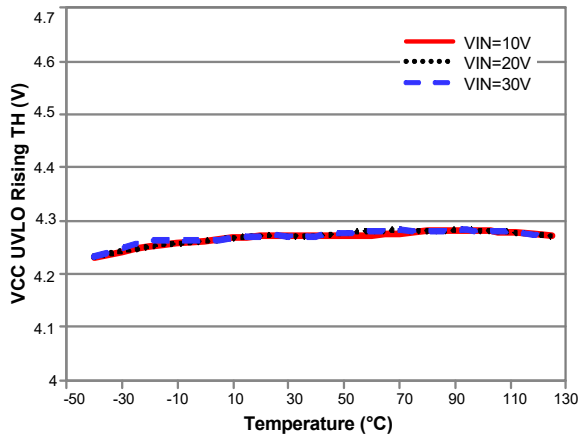


Figure 1. VCC UVLO Rising Threshold

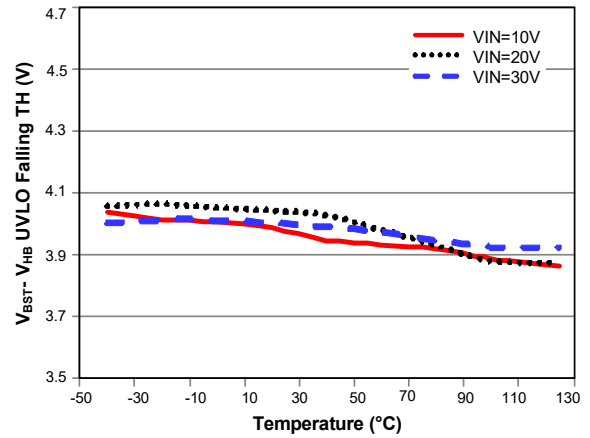


Figure 2. $V_{BST} - V_{HB}$ UVLO Falling Threshold

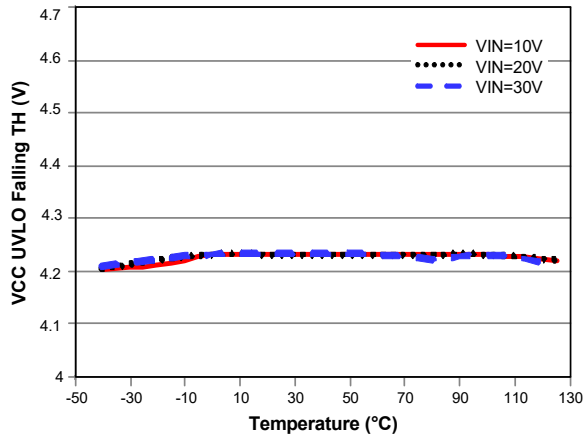


Figure 3. VCC UVLO Falling Threshold

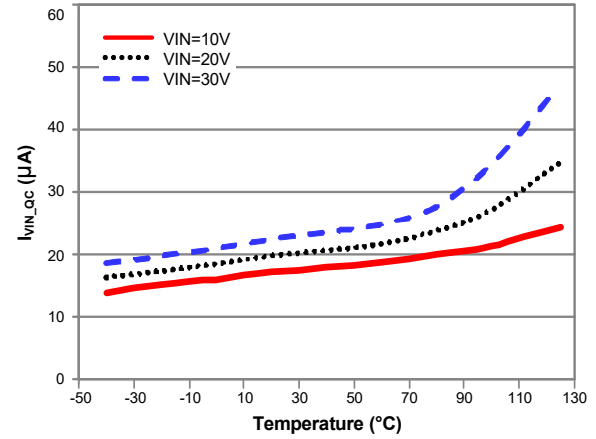


Figure 4. Input Standby Current

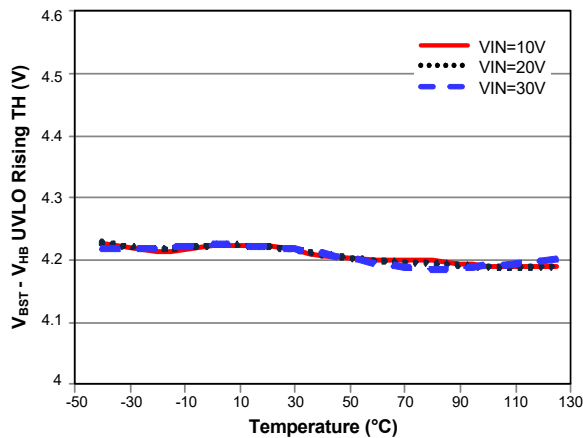


Figure 5. $V_{BST} - V_{HB}$ UVLO Rising Threshold

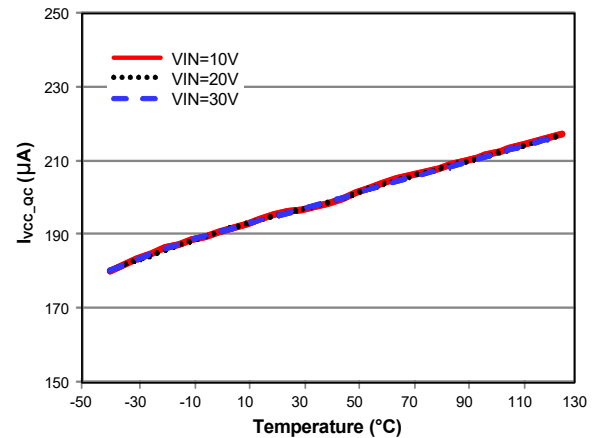


Figure 6. V_{CC} Standby Current

Typical Performance Characteristics (Continued)

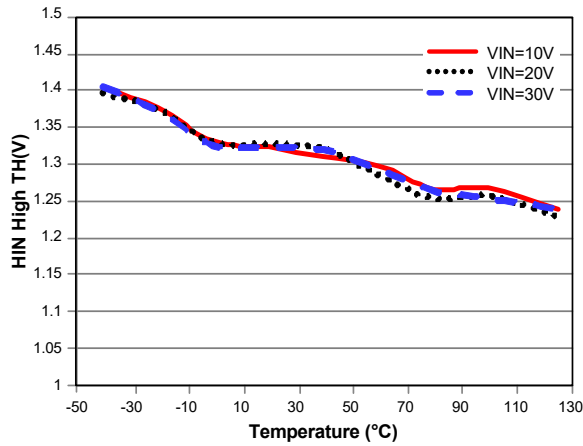


Figure 7. HIN High Threshold

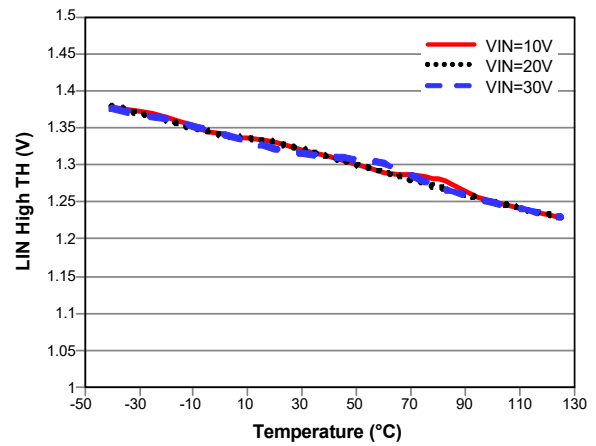


Figure 8. LIN High Threshold

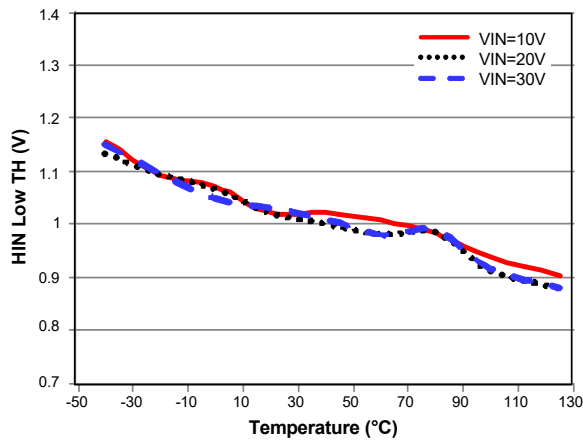


Figure 9. HIN Low Threshold

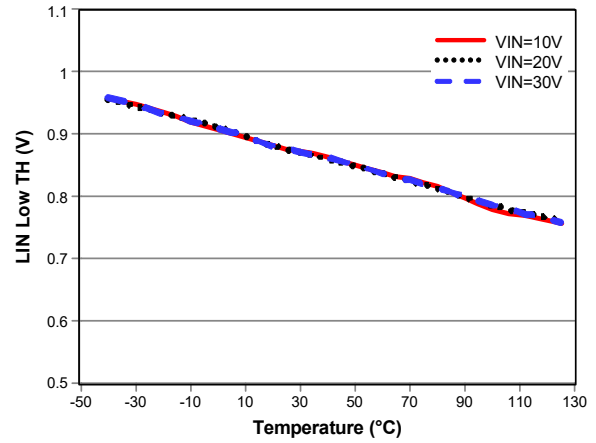


Figure 10. LIN Low Threshold

Detailed Description

The AOZ32033AQI is an integrated half-bridge solution with intelligent slew-rate control for wireless charger application. The device includes the high-side, low-side N-channel MOSFETs and its driver circuit. Typically, it's dedicated for the design of wireless charger transmitter circuit which is composed of full-bridge topology with resonant tank circuit to get best efficiency of power converter.

The AOZ32033AQI provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance.

In addition, the AOZ32033AQI provides several fault protections, such as UVLO, OTP and non-overlapping mechanism.

The AOZ32033AQI is available in 18-pin 3mm×3mm QFN package.

Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. So, AOZ32033AQI provides external adjustable resistors for tuning gate drive source and sink current.

SRC is used to tune gate drive source and sink current, respectively. A resistor connects between SRC pin and GND to setting gate drive source / sink current by internal current mirror, as illustrated Fig. 11. Source and sink current use maximum capability to drive when SRC pin is floating or the voltage on SRC pin is exceed 4V.

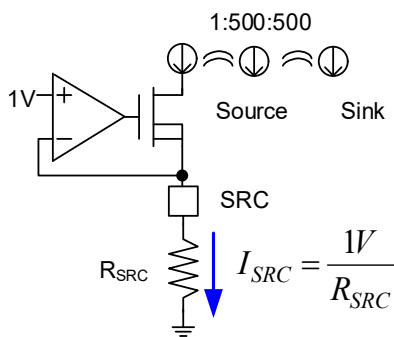


Figure 11. Source/Sink Current Implement Waveform

In addition, source and sink current controls are implemented only during MOSFET Miller effect and $V_{GS} > 1V$, as illustrated Fig. 12.

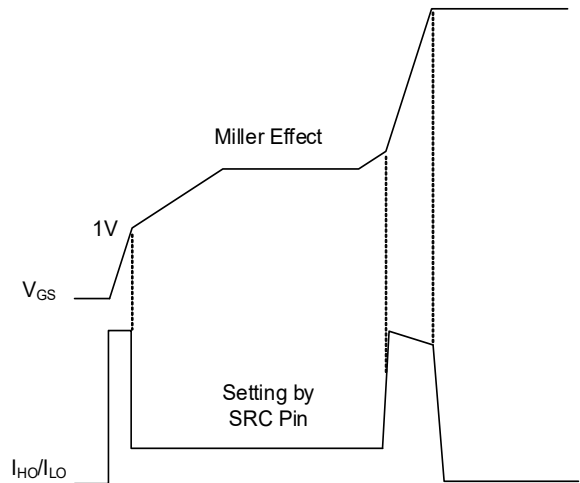


Figure 12. Source /Sink Current Implement Waveform

Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.
2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.
3. The VHB pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VHB pins to help thermal dissipation.
4. Decoupling capacitor C_{VCC} should be connected to V_{CC} and AGND as close as possible.
5. Bootstrap capacitor C_{BST} should be connected to VBST and VHB as close as possible.

6. A ground plane is preferred; PGND and AGND must be connected to the ground plane through vias.
7. Keep sensitive signal traces such as feedback trace and digital signals far away from the VHB pins.

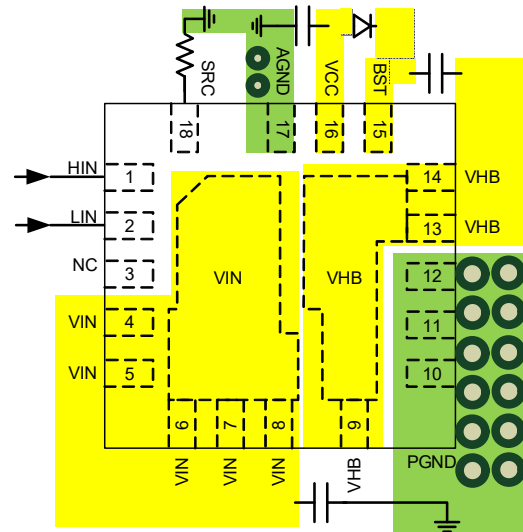
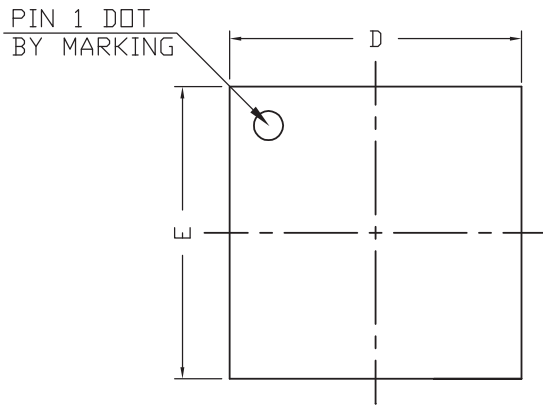
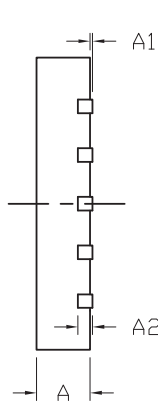


Figure 13. Layout Placement

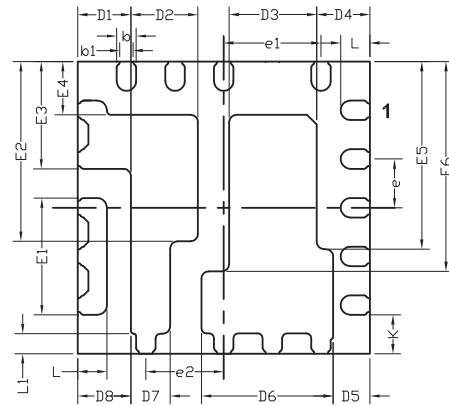
Package Dimensions, QFN3x3-18L



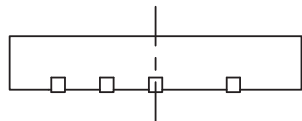
Top VIEW



SIDE VIEW

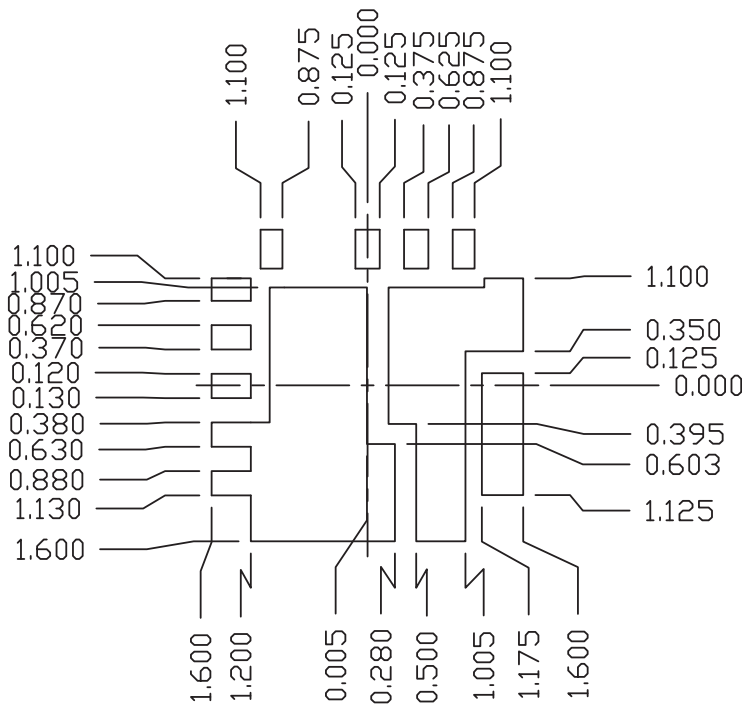


Bottom VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



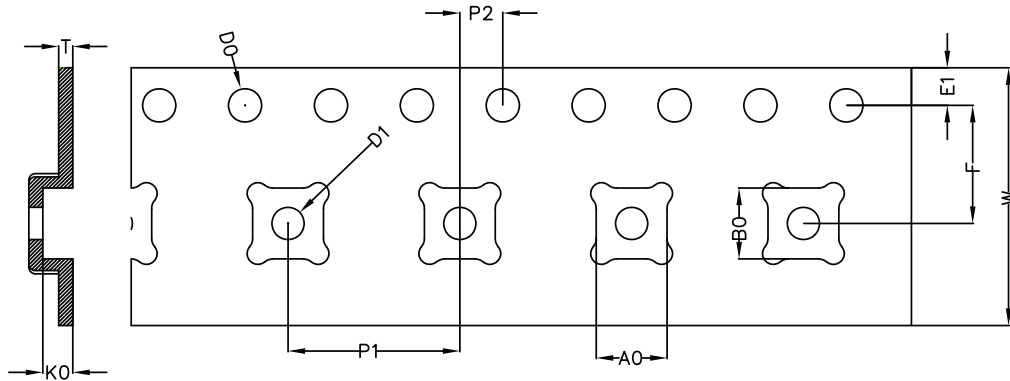
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.55	0.65	0.018	0.022	0.026
A1	0.00	-	0.05	0.000	-	0.002
A2	0.10	0.15	0.20	0.004	0.006	0.008
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.15	1.20	1.25	0.045	0.047	0.049
E2	1.80	1.85	1.90	0.071	0.073	0.075
E3	1.00	1.10	1.20	0.039	0.043	0.047
E4	0.45	0.55	0.65	0.018	0.021	0.025
E5	1.88	1.93	1.98	0.074	0.076	0.078
E6	2.10	2.15	2.20	0.083	0.085	0.087
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	0.45	0.55	0.65	0.018	0.021	0.025
D2	0.64	0.69	0.74	0.025	0.027	0.029
D3	0.85	0.90	0.95	0.033	0.035	0.037
D4	0.45	0.55	0.65	0.018	0.021	0.025
D5	0.33	0.38	0.43	0.013	0.015	0.017
D6	1.30	1.35	1.40	0.051	0.053	0.055
D7	0.35	0.40	0.45	0.014	0.016	0.018
D8	0.50	0.55	0.60	0.019	0.021	0.023
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.15	0.20	0.25	0.006	0.008	0.010
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.09	0.14	0.19	0.004	0.006	0.007
K	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50			0.020		
e1	1.00			0.039		
e2	0.80			0.031		

NOTE
CONTROLLING DIMENSION IS MILLIMETER.

Tape and Reel Drawing, QFN3x3-18L

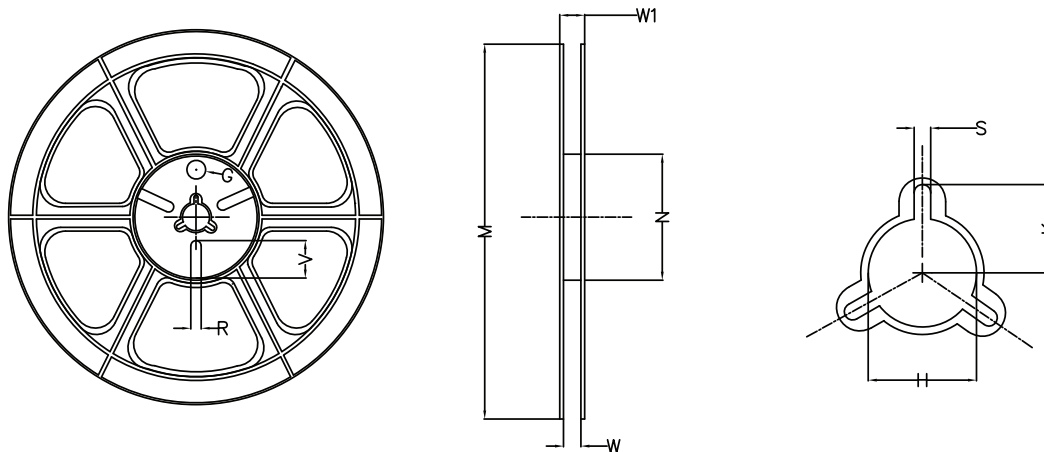
QFN3x3 18L EP2 S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E1	F	P0	P1	P2	T
QFN3x3_18L	3.30 ±0.10	3.30 ±0.10	0.80 ±0.10	1.55 ±0.05	1.50 Min.	12.00 +0.30 -0.00	1.75 ±0.10	5.50 ±0.10	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	0.30 ±0.05

QFN3x3 18L EP2 S Reel



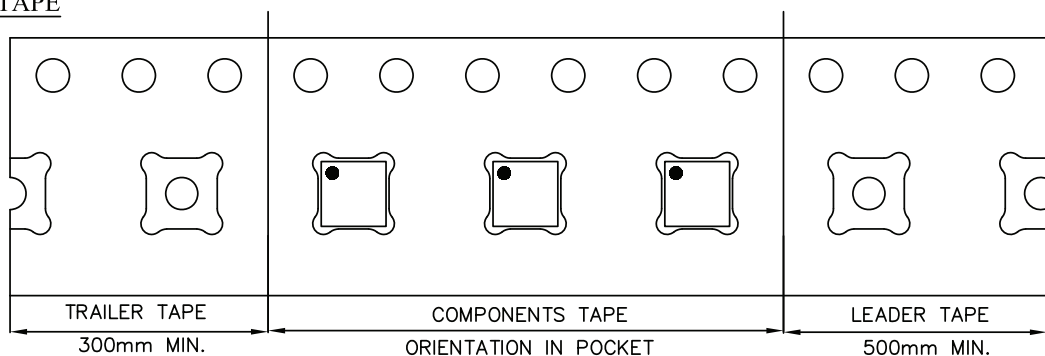
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	S	K	G	R	V
12 mm	ø330	ø330.00 ±2.00	ø101.6 ±2.00	12.40 +2.00 -0.00	12.40 +3.00 -0.20	ø13.20 ±0.30	1.70-2.60	---	---	---	---

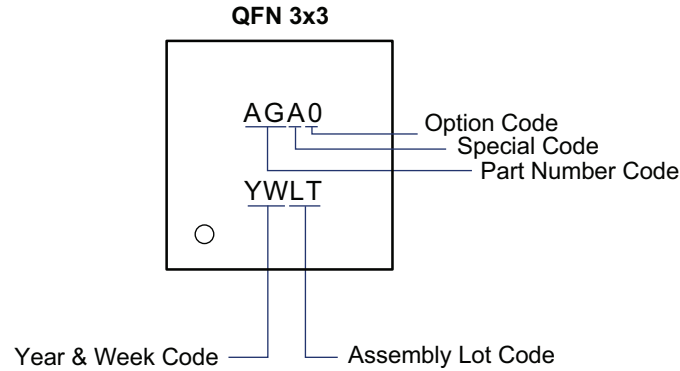
QFN3x3 18L EP2 S TAPE

Leader / Trailer
& Orientation

Unit Per Reel:
5000pcs



Part Marking



Note:

Assembly Location - YWLT/YWLT_I/YWLT_I

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.