ALPHA & OMEGA
S E M I C O N D U C T O R

AOZ32033AQI

Coil Driver for Wireless Charger Transmitter with Slew-Rate Control

General Description

The AOZ32033AQI is an integrated half-bridge solution with intelligent slew-rate control for wireless charger application. The device includes the high-side, low-side N-channel MOSFETs and its driver circuit. Typically, it's dedicated for the design of wireless charger transmitter circuit which is composed of full-bridge topology with resonant tank circuit to get best efficiency of power converter.

The AOZ32033AQI provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance. Moreover, the features of AOZ32033AQI have multiple protection functions such as V_{CC} UVLO, over temperature protection to make the design more robust.

The AOZ32033AQI is available in a 3mm×3mm QFN-18L package and is rated over a -40°C to +85°C ambient temperature range.

Features

- Maximum operating input voltage 28V
  - Support 12V & 24V voltage rail system
- 15W~30W coil driver
  - For wireless charger transmitter circuit
- Slew-rate control to improve EMI performance
- Integrated bootstrap diode
- Support protection
  - OTP, UVLO
- Thermally enhanced 18-pin 3×3 QFN

Applications

- Wireless charger TX

Green Product

Typical Application (Wireless Charger TX)
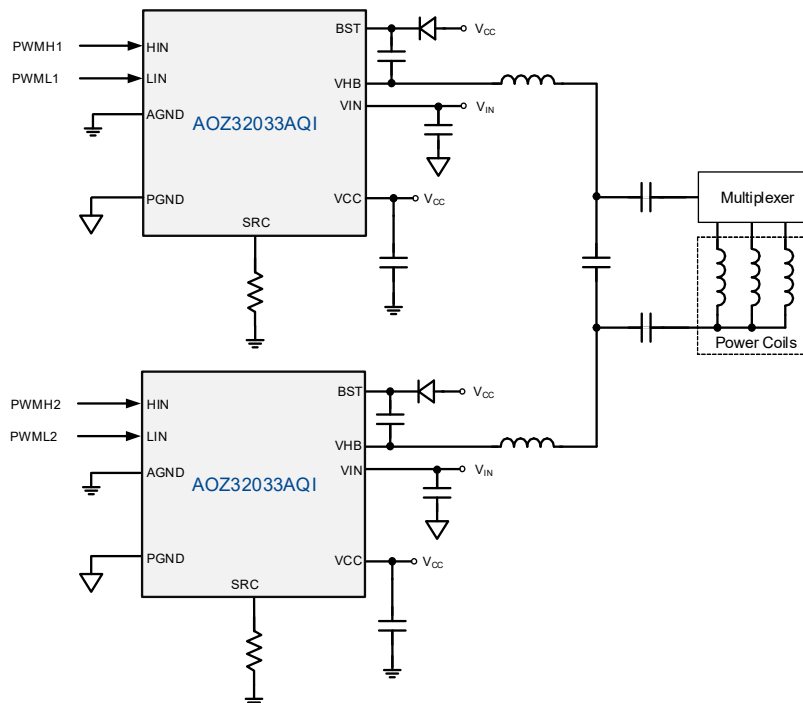
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32033AQI	-40°C to +85°C	18-Pin 3x3 QFN	Green

All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit http://www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Green
Product

Pin Configuration
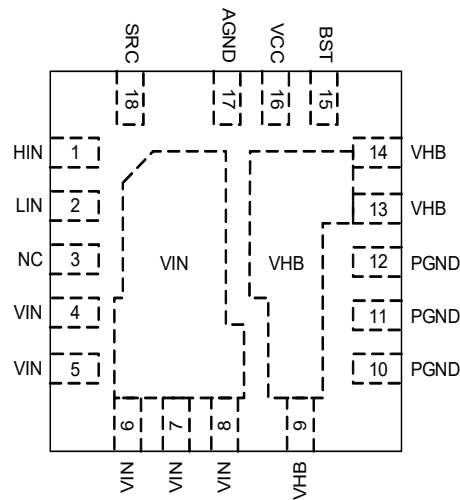
18-Pin 3mm x 3mm QFN

Start-up Sequence
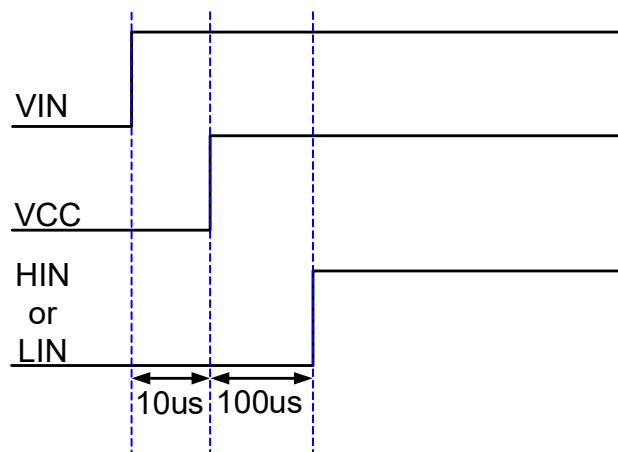
Pin Description

Pin Number	Pin Name	Pin Function
1	HIN	PWM Input for High-Side MOSFET.
2	LIN	PWM Input for Low-Side MOSFET.
3	NC	No connect
4, 5, 6, 7, 8	VIN	Supply Input. All VIN pins must be connected together.
9, 13, 14	VHB	Switching Node for Half-Bridge. All VHB must be connected together.
10, 11, 12	PGND	Power Ground.
15	BST	Bootstrap Capacitor Connection. Connect an external capacitor between BST and VHB for supplying high-side MOSFET.
16	VCC	Supply Input for Analog Functions. Bypass VCC to AGND with a 0.1uF~10uF ceramic capacitor and as close to VCC pin as possible
17	AGND	Analog Ground.
18	SRC	Slew-Rate Control to Adjust Driver Speed of Internal MOSFET.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
VIN to AGND	-0.3V to 30V
VHB to AGND	-0.3V to 30V
BST to AGND	-0.3V to 40V
BST to VHB	-0.3 to 6V
SRC, VCC to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +1V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating	±2kV

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	3.8V to 28V
Supply Voltage (V_{CC})	4.75V to 5.5V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	40°C/W 0.6°C/W

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{UVLO_R}	Vcc UVLO Rising	V_{IN} =12V, Vcc increase, Monitor SRC from low to high		4.3		V
V_{UVLO_F}	Vcc UVLO Falling	V_{IN} =12V, Vcc decrease, Monitor SRC from high to low		4.2		V
$V_{B\_UVLO\_R}$	V_{BST}-V_{HB} UVLO Rising	V_{IN} =20V, (V_{BST} -V_{HB}) increase, Monitor V_{HB} from low to high		4.3		V
$V_{B\_UVLO\_F}$	V_{BST}-V_{HB} UVLO Falling	V_{IN} =20V, (V_{BST} -V_{HB}) decrease, Monitor V_{HB} from high to low		4.2		V
I_{VIN_QC}	I_{VIN} Quiescent Current	V_{IN} =12V, V_{CC}=5V, HIN=LIN=0V, SRC=100kΩ		30		µA
I_{VCC_QC}	I_{VCC} Quiescent Current	V_{IN} =12V, V_{CC}=5V, HIN=LIN=0V, SRC=100kΩ		200		µA
$I_{BST-VHB\_QC}$	$I_{BST-VHB}$ Quiescent Current	HIN/LIN=0V, V_{HB}=1V, (V_{BST} -V_{HB})=5V, Monitor (V_{BST} -V_{HB}) Current			0.2	mA
V_{HLIN_L}	HIN/LIN Logic Low Voltage	V_{IN}=12V	0		1.2	V
V_{HLIN_H}	HIN/LIN Logic High Voltage	V_{IN}=12V	2.2		5.5	V
R_{HLIN_IN}	HIN/LIN Input Pull Low Impedance			280		kΩ
t_{HIN_RP}	HIN Rising Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ, VHB to GND=100Ω, HIN=Low to High, Monitor V_{HB} Low to High		55		ns
t_{HIN_FP}	HIN Falling Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ, VHB to GND=100Ω, HIN=High to Low, Monitor V_{HB} High to Low		75		ns
t_{LIN_RP}	LIN Rising Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ,VHB to VIN=100Ω, LIN=Low to High, Monitor V_{HB} High to Low		45		ns
t_{LIN_FP}	LIN Falling Propagation Delay	V_{IN}=10V, V_{CC}=5V, SRC=20kΩ,VHB to VIN=100Ω, LIN=High to Low, Monitor V_{HB} Low to High		70		ns

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{DM_R}	Delay Matching Rising	Difference between t_{HIN_RP} and t_{LIN_RP}		10		ns
T_{DM_F}	Delay Matching Falling	Difference between t_{HIN_FP} and t_{LIN_FP}		5		ns
V_{SRC}	SRC	V_{IN}=12V, V_{CC}=5V, SRC=20kΩ	0.97	1	1.03	V
I_{SRC_MIN}	SRC Min. Source Current	V_{IN}=12V, V_{CC}=5V, SRC=4V		0.5		µA
I_{SRC_MAX}	SRC Max. Source Current	V_{IN}=12V, V_{CC}=5V, SRC=0.8V		140		µA
SR_{HIN_R}	HIN Rising Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to GND=100Ω, HIN=Low to High, Monitor V_{HB} Rising Slew Rate		0.85		V/ns
SR_{HIN_F}	HIN Falling Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to GND=100Ω, HIN=High to Low, Monitor V_{HB} Falling Slew Rate		0.06		V/ns
SR_{LIN_R}	LIN Rising Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to VIN=100Ω, LIN=High to Low, Monitor V_{HB} Rising Slew Rate		0.07		V/ns
SR_{LIN_F}	LIN Falling Slew Rate (SRC=20kΩ)	VIN=10V, V_{CC}=5V, V_{HB} to VIN=100Ω, LIN=Low to High Monitor V_{HB} Falling Slew Rate		1.3		V/ns
R_{H_ON}	V_{IN}-V_{HB} RON	V_{IN}=12V, V_{CC}=5V, HIN=5V, (V_{BST} -V_{HB})=5V, I_{VHB}=1A		11		mΩ
R_{L_ON}	V_{HB}-PGND RON	V_{IN}=12V, V_{CC}=5V, LIN=5V, PGND=0, I_{VHB}=1A		11		mΩ
V_{SD}	Boost Diode Forward Voltage	Forward Current = 2mA		0.4		V
T_{OTP}	OTP	V_{IN}=12V, V_{CC}=5V		150		°C

Functional Block Diagram
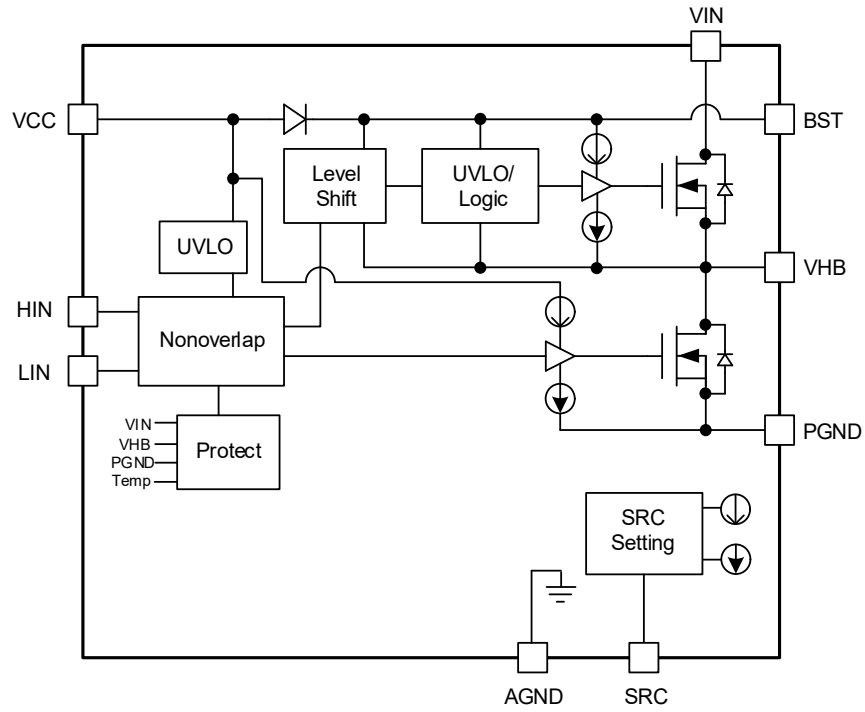
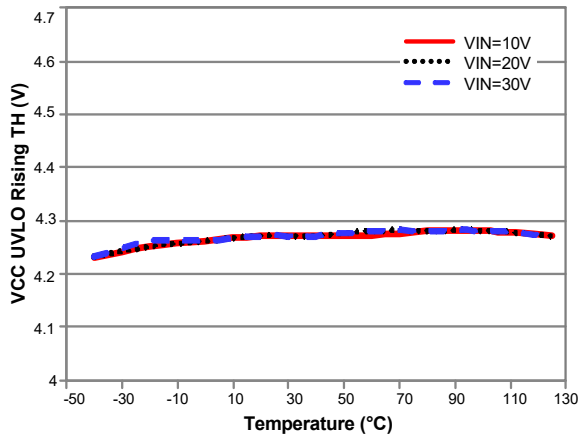## Typical Performance Characteristics

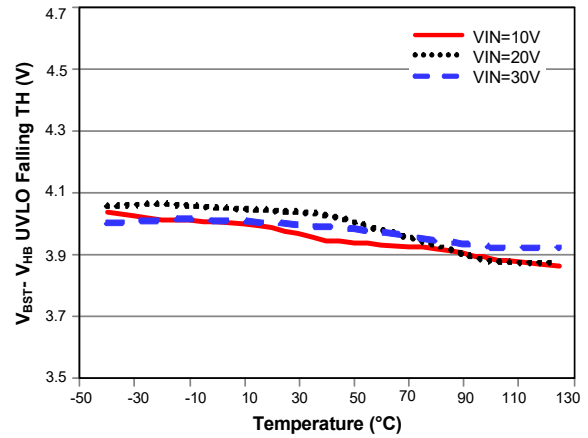**Figure 1. VCC UVLO Rising Threshold**
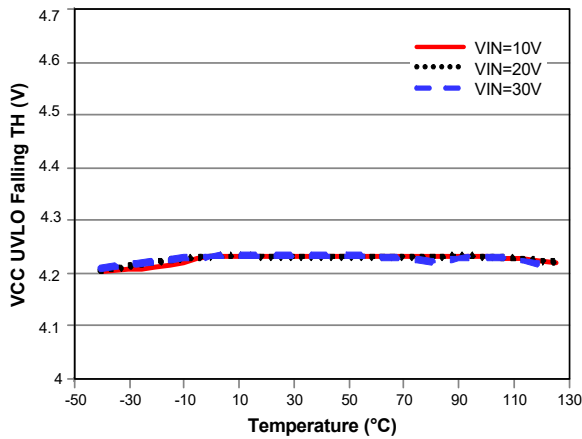
Figure 2. $V_{BST} - V_{HB}$ UVLO Falling Threshold
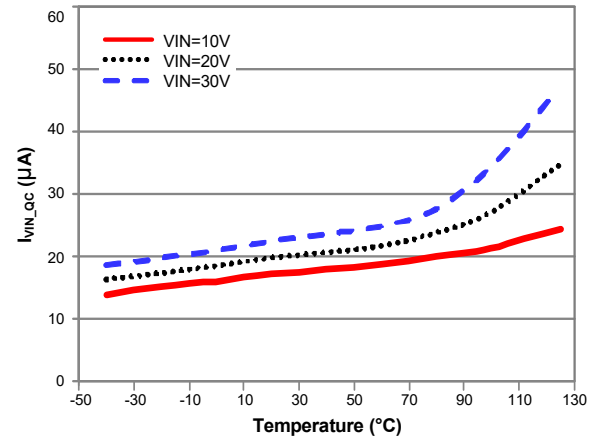
Figure 3. VCC UVLO Falling Threshold
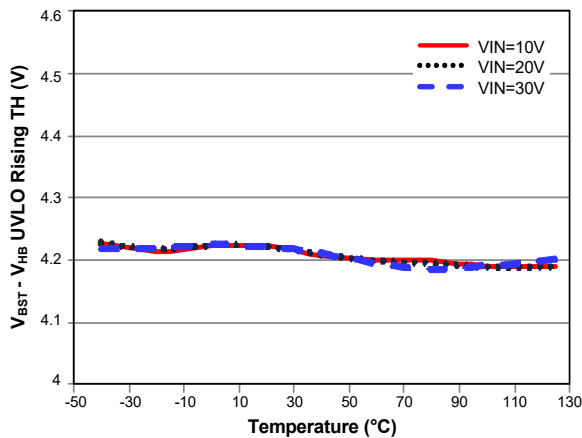
Figure 4. Input Standby Current

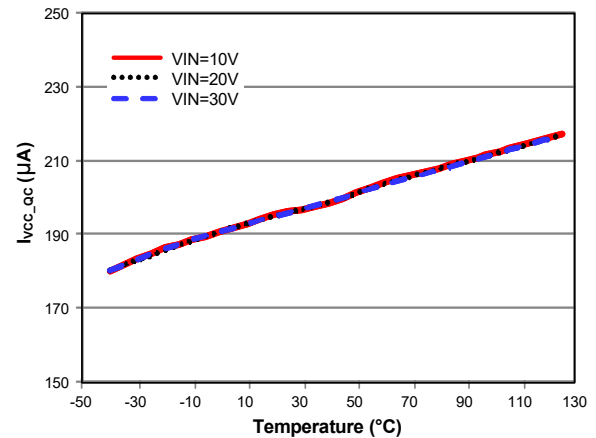**Figure 5. $V_{BST} - V_{HB}$ UVLO Rising Threshold**

Figure 6. V_{CC} Standby Current
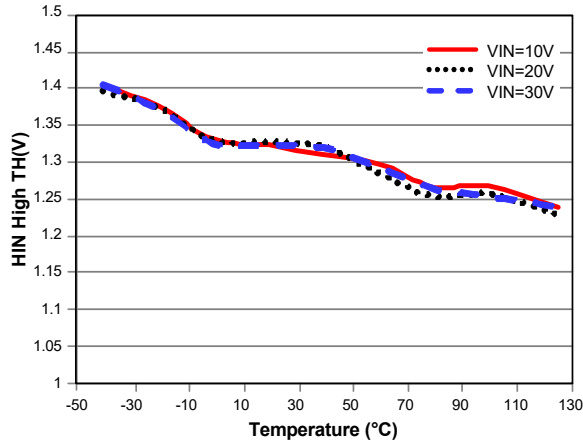
Typical Performance Characteristics *(Continued)*

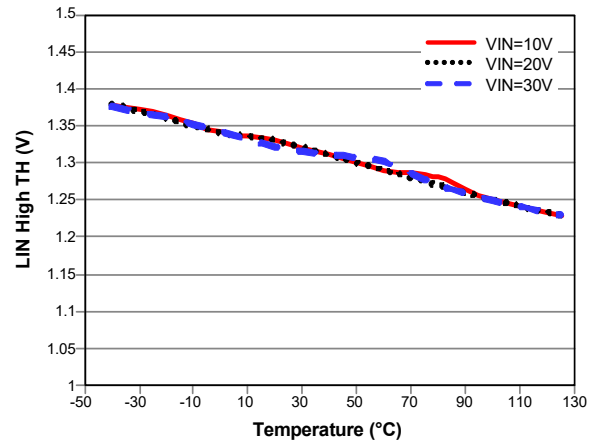**Figure 7. HIN High Threshold**

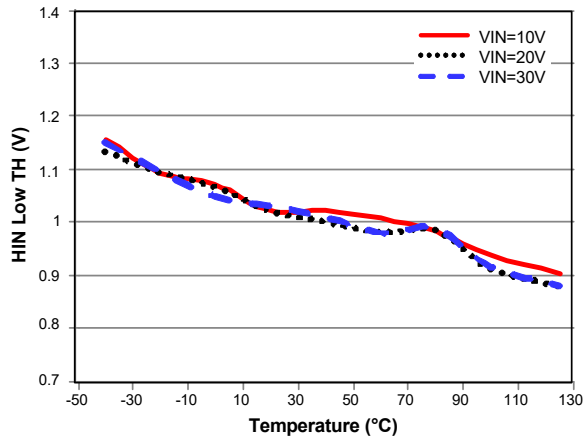**Figure 8. LIN High Threshold**
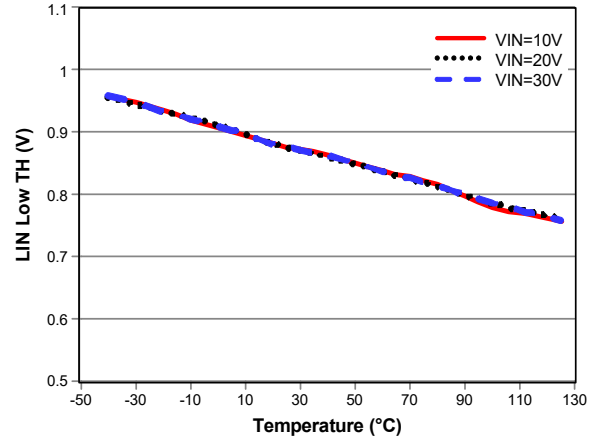
Figure 9. HIN Low Threshold

Figure 10. LIN Low Threshold

Detailed Description

The AOZ32033AQI is an integrated half-bridge solution with intelligent slew-rate control for wireless charger application. The device includes the high-side, low-side N-channel MOSFETs and its driver circuit. Typically, it's dedicated for the design of wireless charger transmitter circuit which is composed of full-bridge topology with resonant tank circuit to get best efficiency of power converter.

The AOZ32033AQI provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance.

In addition, the AOZ32033AQI provides several fault protections, such as UVLO, OTP and non-overlapping mechanism.

The AOZ32033AQI is available in 18-pin 3mm×3mm QFN package.

Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. So, AOZ32033AQI provides external adjustable resistors for tuning gate drive source and sink current.

SRC is used to tune gate drive source and sink current, respectively. A resistor connects between SRC pin and GND to setting gate drive source / sink current by internal current mirror, as illustrated Fig. 11. Source and sink current use maximum capability to drive when SRC pin is floating or the voltage on SRC pin is exceed 4V.
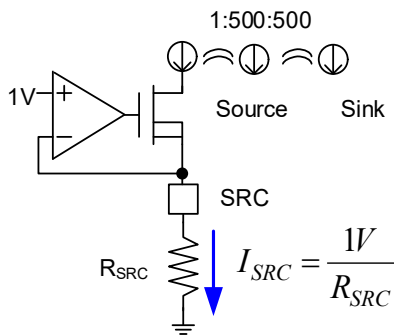
In addition, source and sink current controls are implemented only during MOSFET Miller effect and VGS >1V, as illustrated Fig. 12.

Figure 12. Source /Sink Current Implement Waveform
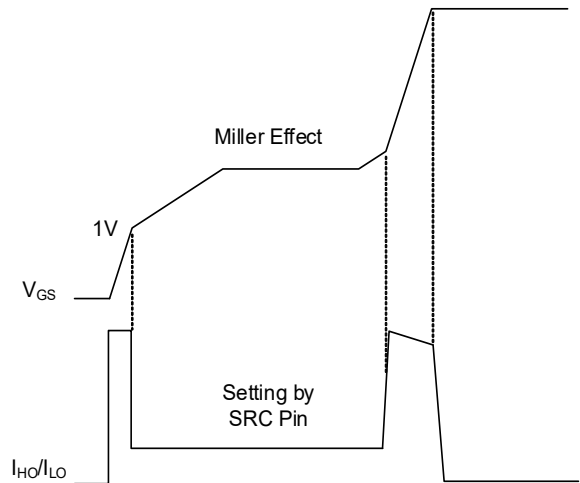

$$I_{SRC} = \frac{1V}{R_{SRC}}$$

Figure 11. Source/Sink Current Implement Waveform

Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.

2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.

3. The VHB pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VHB pins to help thermal dissipation.

4. Decoupling capacitor C_{VCC} should be connected to V_{CC} and AGND as close as possible.

5. Bootstrap capacitor C_{BST} should be connected to VBST and VHB as close as possible.

6. A ground plane is preferred; PGND and AGND must be connected to the ground plane through vias.

7. Keep sensitive signal traces such as feedback trace and digital signals far away from the VHB pins.
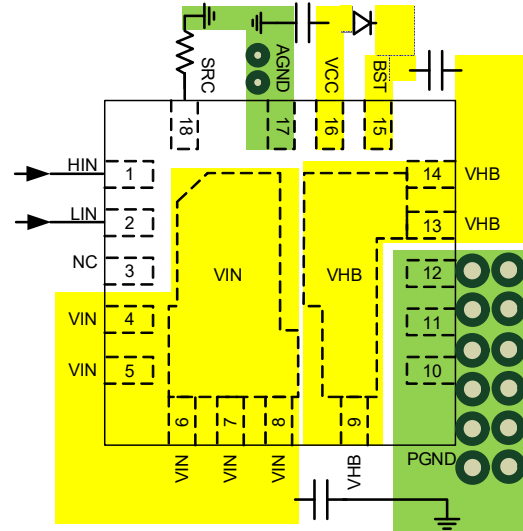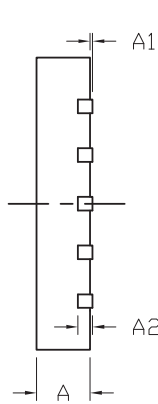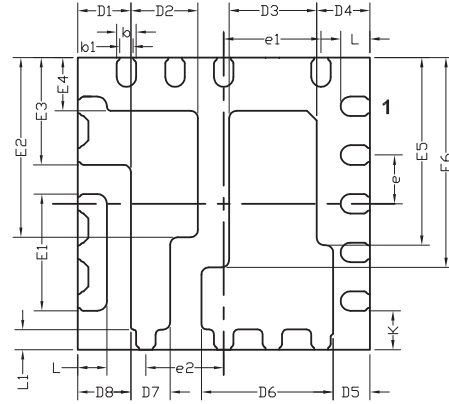

Figure 13. Layout Placement
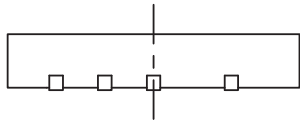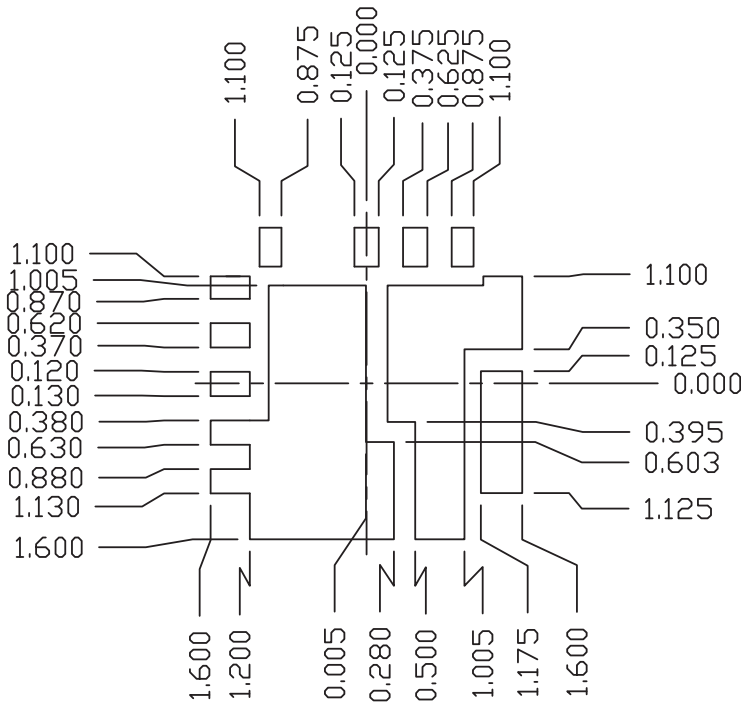
Package Dimensions, QFN3x3-18L

PIN 1 DOT BY MARKING
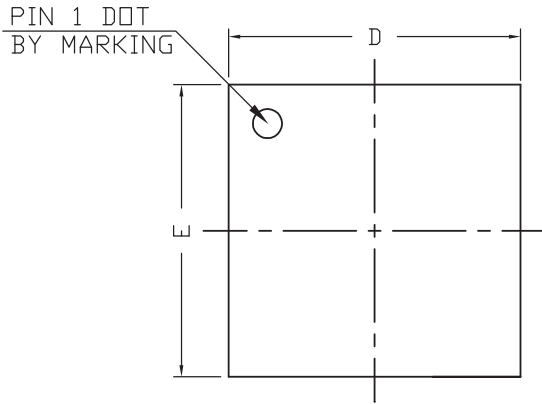
Top VIEW

SIDE VIEW

Bottom VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN

UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.55	0.65	0.018	0.022	0.026
A1	0.00	-	0.05	0.000	-	0.002
A2	0.10	0.15	0.20	0.004	0.006	0.008
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.15	1.20	1.25	0.045	0.047	0.049
E2	1.80	1.85	1.90	0.071	0.073	0.075
E3	1.00	1.10	1.20	0.039	0.043	0.047
E4	0.45	0.55	0.65	0.018	0.021	0.025
E5	1.88	1.93	1.98	0.074	0.076	0.078
E6	2.10	2.15	2.20	0.083	0.085	0.087
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	0.45	0.55	0.65	0.018	0.021	0.025
D2	0.64	0.69	0.74	0.025	0.027	0.029
D3	0.85	0.90	0.95	0.033	0.035	0.037
D4	0.45	0.55	0.65	0.018	0.021	0.025
D5	0.33	0.38	0.43	0.013	0.015	0.017
D6	1.30	1.35	1.40	0.051	0.053	0.055
D7	0.35	0.40	0.45	0.014	0.016	0.018
D8	0.50	0.55	0.60	0.019	0.021	0.023
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.15	0.20	0.25	0.006	0.008	0.010
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.09	0.14	0.19	0.004	0.006	0.007
K	0.35	0.40	0.45	0.014	0.016	0.018
e		0.50			0.020	
e1		1.00			0.039	
e2		0.80			0.031	

NOTE
CONTROLLING DIMENSION IS MILLIMETER.

Tape and Reel Dimensions, QFN3x3-18L

QFN3x3_18L_EP2_S Carrier Tape
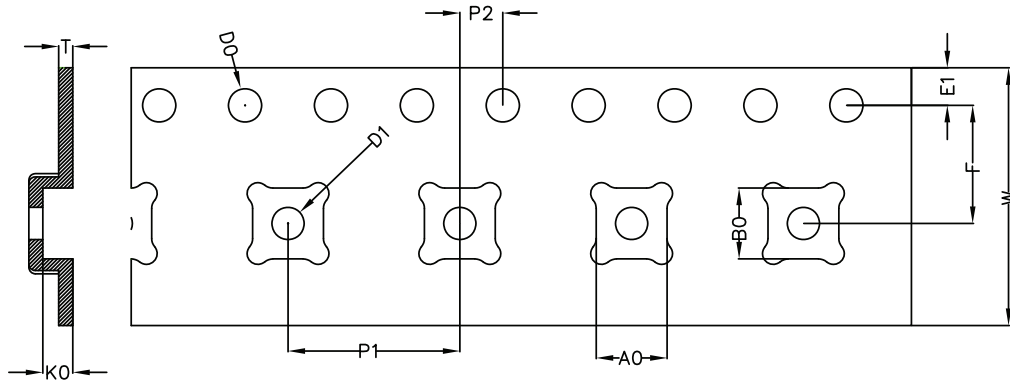
UNIT: MM

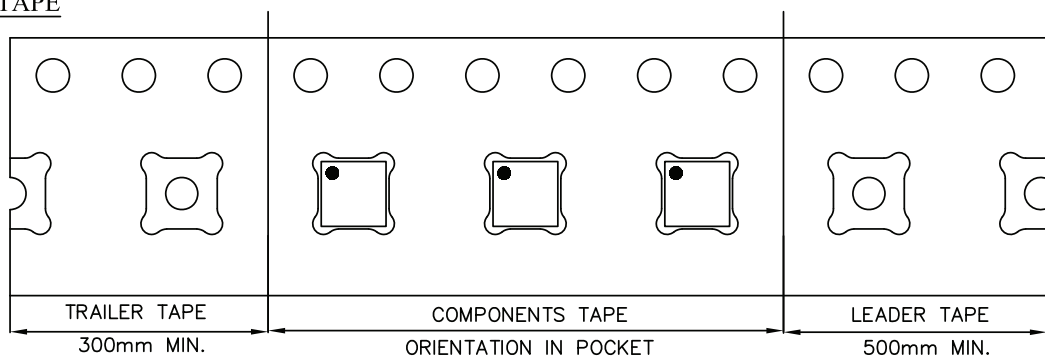| PACKAGE	A0	B0	K0	D0	D1	W	E1	F	P0	P1	P2	T
QFN3X3_18L	3.30 ±0.10	3.30 ±0.10	0.80 ±0.10	1.55 ±0.05	1.50 Min.	12.00 +0.30 −0.00	1.75 ±0.10	5.50 ±0.10	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	0.30 ±0.05

QFN3x3_18L_EP2_S Reel
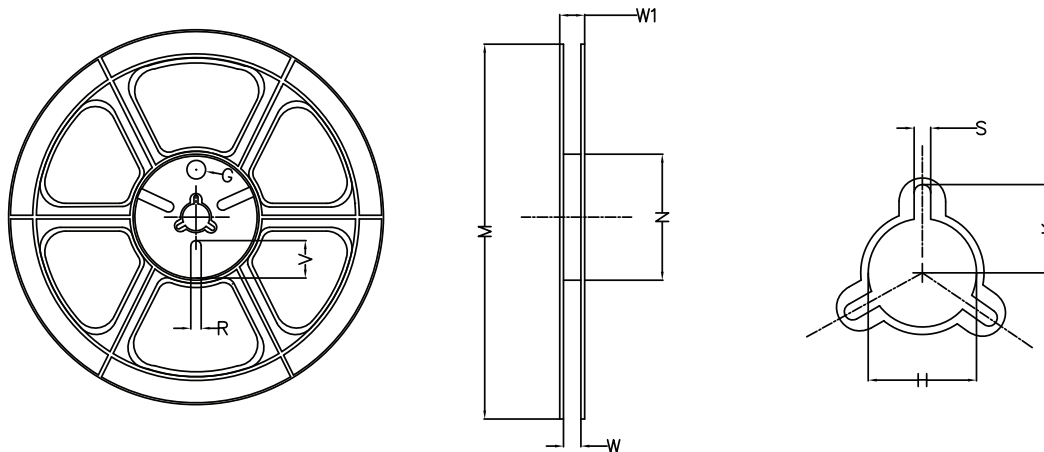
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	S	K	G	R	V
12 mm	⌀330	⌀330.00 ±2.00	⌀101.6 ±2.00	12.40 +2.00 −0.00	12.40 +3.00 −0.20	⌀13.20 ±0.30	1.70−2.60	---	---	---	---

QFN3x3_18L_EP2_S_TAPE

Leader / Trailer
& Orientation

Unit Per Reel:
5000pcs

TRAILER TAPE
300mm MIN.

COMPONENTS TAPE
ORIENTATION IN POCKET

LEADER TAPE
500mm MIN.

Part Marking

AOZ32033AQI
(QFN 3x3)

AGA0 ——— Option Code
——— Special Code
——— Part Number Code

YWLT

○

Year & Week Code ——— ——— Assembly Lot Code
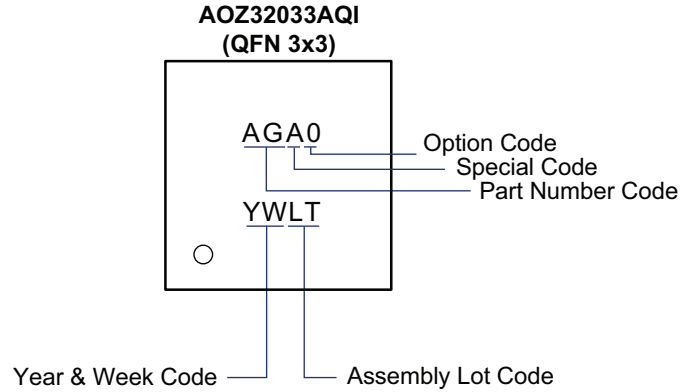
Note:
Assembly Location - YWLT/YWL<u>T</u>/YWL<u>T̄</u>

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.