

## General Description

The AOZ5547QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra low ON resistance to minimize conduction loss. The compact 3.5mm x 5mm QFN package is optimally chosen and designed to minimize parasitic inductance for minimal EMI signature.

The AOZ5547QI is intended for use with TTL and Tri-state compatibility by using both the PWM and/or FCCM inputs for accurate control of the power MOSFETs.

A number of features are provided making the AOZ5547QI a highly versatile power module: The bootstrap diode is integrated in the driver. The low side MOSFET can be driven into diode emulation mode to provide asynchronous operation when required. The pin-out is optimized for low inductance routing of the converter, keeping the parasitics and their effects to a minimum.

## Features

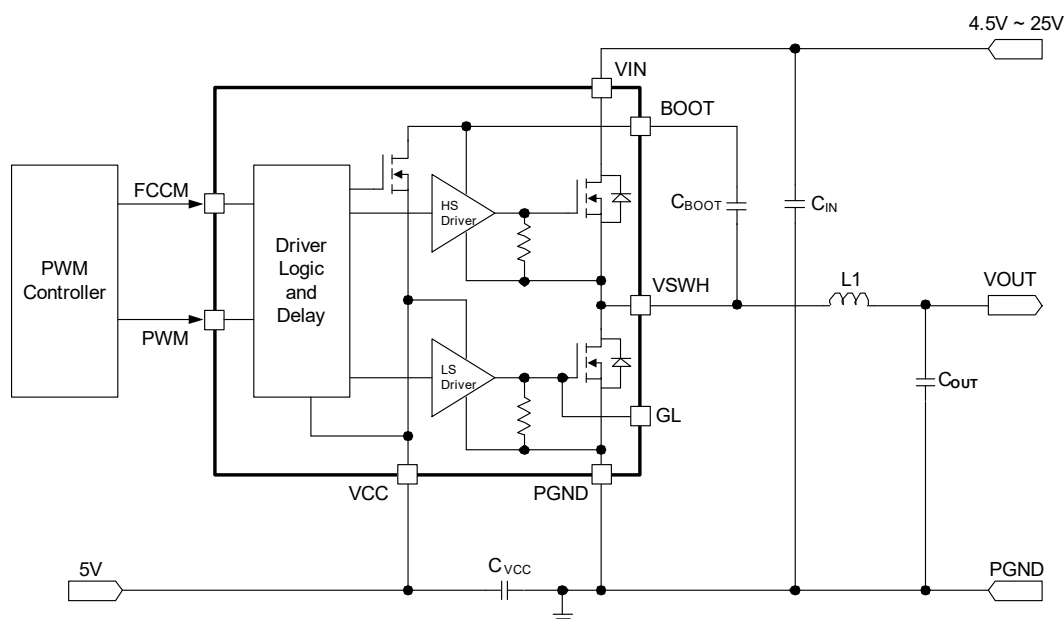
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- Up to 35A peak output current
- Integrated boost strap switch
- Up to 2MHz switching operation
- Tri-state PWM input compatible
- Under-Voltage lockout protection
- Single pin control for Shutdown / Diode Emulation / CCM operation
- Small 3.5mm x 5mm QFN-24L package

## Applications

- Servers
- Notebook computers
- VRMs for motherboards
- Point of load DC/DC converters
- Memory and graphic cards
- Video gaming console



## Typical Application Circuit



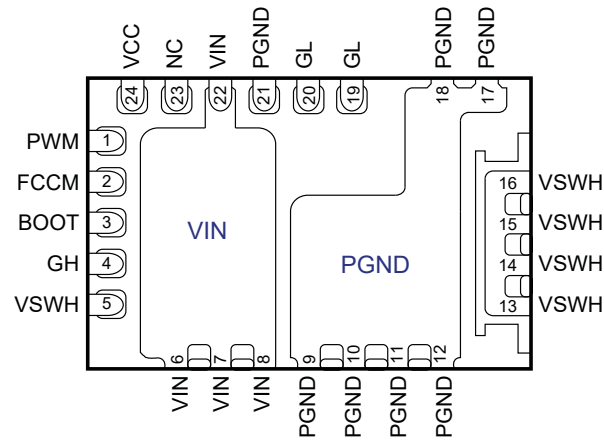
## Ordering Information

| Part Number | Ambient Temperature Range | Package      | Environmental |
|-------------|---------------------------|--------------|---------------|
| AOZ5547QI   | -40°C to +125°C           | QFN3.5x5_24L | RoHS          |



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## Pin Configuration

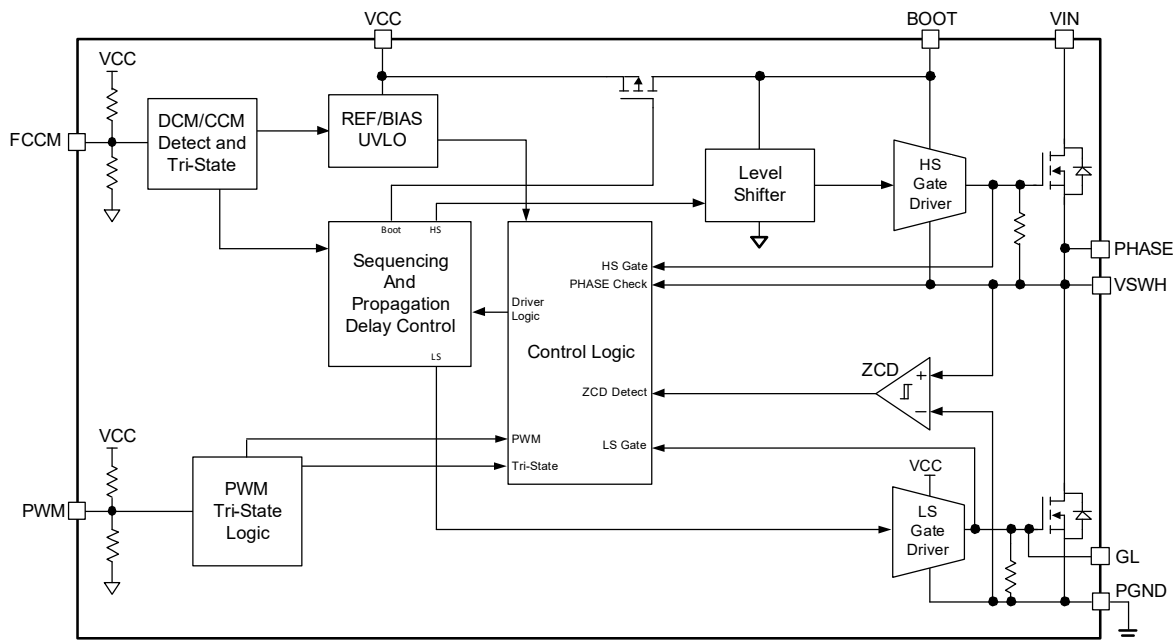


3.5mm x 5mm QFN-24  
(Top View)

## Pin Description

| Pin Number                | Pin Name | Pin Function  |
|---------------------------|----------|---|
| 1                         | PWM      | PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic levels.   |
| 2                         | FCCM     | Continuous conduction mode of operation is allowed when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. Shutdown when FCCM = Floating.         |
| 3                         | BOOT     | High Side MOSFET Gate Driver supply rail (5V with reference to VSWH). Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 5).   |
| 4                         | GH       | High Side MOSFET Gate connection. This is for test purposes.  |
| 5                         | PHASE    | This pin is dedicated for bootstrap capacitor AC connection to BOOT (Pin 3).  |
| 6, 7, 8, 22               | VIN      | Power stage High Voltage Input (Drain Connection of High-Side MOSFET).  |
| 9, 10, 11, 12, 17, 18, 21 | PGND     | Power and Signal Ground.  |
| 13, 14, 15, 16            | VSWH     | Switching node connected to source of High-Side MOSFET and drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal. |
| 19, 20                    | GL       | Low Side MOSFET Gate connection. This is for test purposes.   |
| 23                        | NC       | No Connect.   |
| 24                        | VCC      | Internal Logic Circuitry and Gate Driver supply rail (5V with reference to PGND). Add a 4.7uF MLCC directly between VCC and PGND (Pin 21).  |

## Functional Block Diagram



## Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

| Parameter   | Rating                           |
|---|----------------------------------|
| Low Voltage Supply ( $V_{CC}$ )                           | -0.3V to 7V                      |
| High Voltage Supply ( $V_{IN}$ )                          | -0.3V to 30V                     |
| Control Inputs (PWM, FCCM)                                | -0.3V to ( $V_{CC}+0.3V$ )       |
| Bootstrap Voltage DC (BOOT-PGND)                          | -0.3V to 33V                     |
| Bootstrap Voltage DC (BOOT-PHASE/VSWH)                    | -0.3V to 7V                      |
| BOOT Voltage Transient <sup>(1)</sup> (BOOT-PHASE/VSWH)   | -0.3V to 9V                      |
| Switch Node Voltage DC (PHASE/VSWH)                       | -0.3V to 30V                     |
| Switch Node Voltage Transient <sup>(1)</sup> (PHASE/VSWH) | -0.3V to 38V                     |
| High Side Gate Voltage DC (GH)                            | (VSWH-0.3V) to BOOT              |
| High Side Gate Voltage Transient <sup>(1)</sup> (GH)      | (VSWH-5V) to BOOT                |
| Low Side Gate Voltage DC (GL)                             | (PGND-0.3V) to ( $V_{CC}+0.3V$ ) |
| Low Side Gate Voltage Transient <sup>(1)</sup> (GL)       | (PGND-2.5V) to ( $V_{CC}+0.3V$ ) |
| Storage Temperature ( $T_S$ )                             | -65°C to +150°C                  |
| Max Junction Temperature ( $T_J$ )                        | 125°C                            |
| ESD Rating <sup>(2)</sup>                                 | 2kV                              |

### Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5k $\Omega$  in series with 100pF.

## Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

| Parameter                        | Rating         |
|----------------------------------|----------------|
| High Voltage Supply ( $V_{IN}$ ) | 4.5V to 25V    |
| Low Voltage Supply ( $V_{CC}$ )  | 4.5V to 5.5V   |
| Control Inputs (PWM, FCCM)       | 0V to VCC      |
| Operating Frequency              | 200kHz to 2MHz |

## Electrical Characteristics<sup>(4)</sup>

TA = 25°C to 125°C. Typical values reflect 25°C ambient temperature. VIN = 12V, VCC = 5V, unless otherwise specified.

| Symbol                       | Parameter                             | Conditions   | Min. | Typ. | Max. | Units |
|------------------------------|---------------------------------------|--|------|------|------|-------|
| V <sub>IN</sub>              | Power Stage Power Supply              |  | 4.5  |      | 25   | V     |
| V <sub>CC</sub>              | Driver Power Supply                   | V <sub>CC</sub> = 5V   | 4.5  |      | 5.5  | V     |
| R <sub>θJC</sub>             | Thermal Resistance                    | PCB Temp = 100°C   |      | 3    |      | °C/W  |
| R <sub>θJA</sub>             |                                       | AOS Demo Board   |      | 10   |      | °C/W  |
| <b>INPUT SUPPLY AND UVLO</b> |                                       |  |      |      |      |       |
| V <sub>CC</sub>              | Under-Voltage Lockout                 | V <sub>CC</sub> Rising   |      | 3.5  | 3.9  | V     |
| V <sub>CC_HYST</sub>         |                                       | V <sub>CC</sub> Falling  |      | 400  |      | mV    |
| I <sub>VCC_SD</sub>          | Shutdown Bias Supply Current          | FCCM = Floating<br>PWM = Floating  |      | 3    |      | μA    |
| I <sub>VCC</sub>             | Control Circuit Bias Current          | FCCM = 5V<br>PWM = Floating  |      | 170  |      | μA    |
|                              |                                       | FCCM = 0V,<br>PWM = Floating   |      | 180  |      | μA    |
| <b>PWM INPUT</b>             |                                       |  |      |      |      |       |
| V <sub>PWMH</sub>            | Logic High Input Voltage              |  | 4.1  |      |      | V     |
| V <sub>PWML</sub>            | Logic Low Input Voltage               |  |      |      | 0.7  | V     |
| I <sub>PWM</sub>             | PWM Pin Input Current                 | PWM = 5V   |      | +200 |      | μA    |
|                              |                                       | PWM = 0V   |      | -200 |      | μA    |
| V <sub>TRI</sub>             | PWM Input Tri-State Window            | PWM = Floating   | 1.5  |      | 3.5  | V     |
| <b>FCCM INPUT</b>            |                                       |  |      |      |      |       |
| V <sub>FCCMH</sub>           | Logic High Input Voltage              | Shutdown → CCM   | 3.9  |      |      | V     |
| V <sub>FCCML</sub>           | Logic Low Input Voltage               | Shutdown → DCM   |      |      | 1.2  | V     |
| I <sub>FCCM</sub>            | FCCM Pin Input Current                | FCCM = 5V  |      | +50  |      | μA    |
|                              |                                       | FCCM = 0V  |      | -50  |      | μA    |
| V <sub>TRI_HYST</sub>        | FCCM Input Threshold Hysteresis       | Shutdown → CCM → Shutdown<br>DCM → Shutdown → DCM  |      | 200  |      | mV    |
| V <sub>TRI</sub>             | FCCM Input Tri-State Threshold Window | FCCM = Floating  | 2.1  |      | 3.1  | V     |
| t <sub>PS4_EXIT</sub>        | PS4 Exit Latency                      |  |      | 5    | 15   | μs    |
| <b>GATE DRIVER TIMING</b>    |                                       |  |      |      |      |       |
| t <sub>PDLU</sub>            | PWM to High-Side Gate                 | PWM: H→L, VSWH: H→L  |      | 30   |      | ns    |
| t <sub>PDLL</sub>            | PWM to Low-Side Gate                  | PWM: L→H, GL: H→L  |      | 25   |      | ns    |
| t <sub>PDHU</sub>            | Low-side to High-Side Gate Deadtime   | GL: H→L, GH: L→H   |      | 15   |      | ns    |
| t <sub>PDHL</sub>            | High-Side to Low-side Gate Deadtime   | GH: H→L, GL: L→H   |      | 13   |      | ns    |
| t <sub>TSSHD</sub>           | Tri-State Shutdown Delay              | PWM: L → V <sub>TRI</sub> , GL: H→L and<br>PWM: H → V <sub>TRI</sub> . VSWH: H→L         |      | 150  |      | ns    |
| t <sub>PTS</sub>             | Tri-State Propagation Delay           | PWM: V <sub>TRI</sub> → 4.1V, VSWH: L→H<br>and PWM: V <sub>TRI</sub> → <0.7V,<br>GL: L→H |      | 45   |      | ns    |
| t <sub>LGMIN</sub>           | Low-Side Minimum On-Time              | FCCM = 0V  |      | 350  |      | ns    |

**Note:**

- All voltages are specified with respect to the corresponding PGND pin.
- Characterization value. Not tested in production.

### Timing Diagram

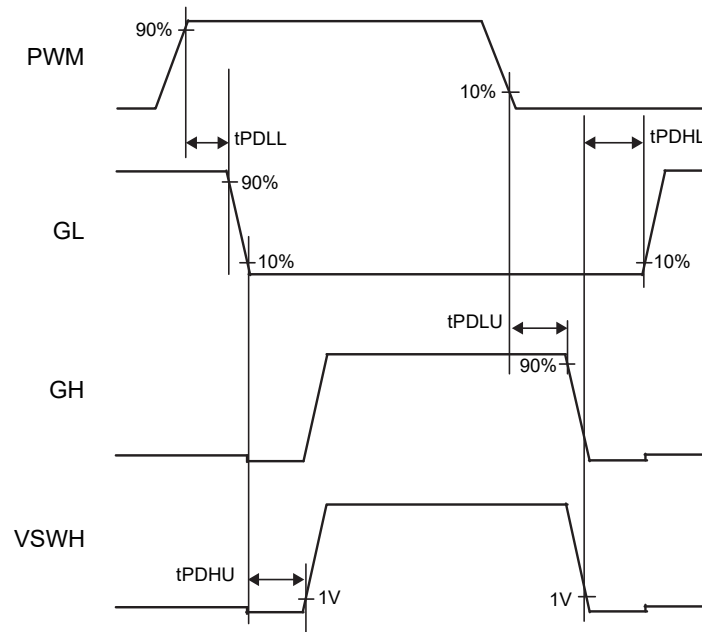


Figure 1. PWM Logic Input Timing Diagram

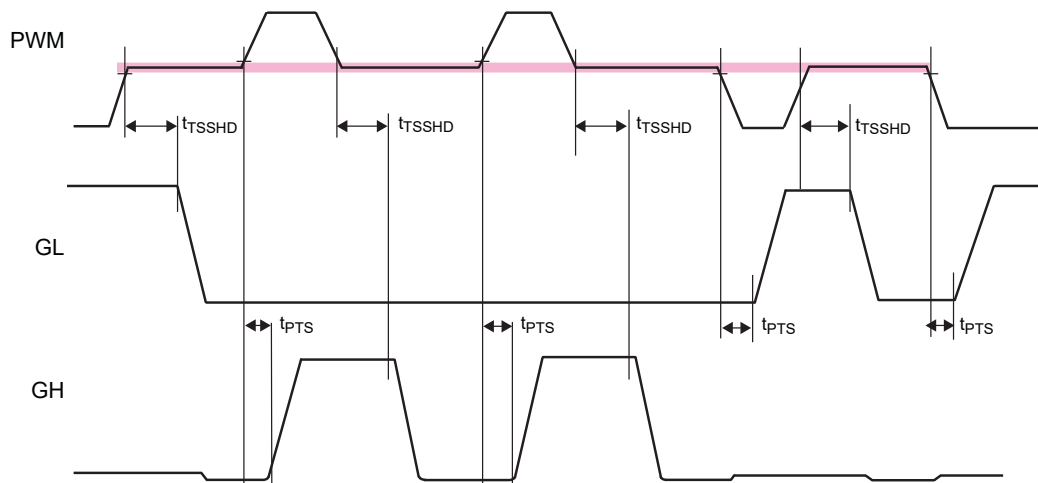


Figure 2. Tri-State Input Logic Timing Diagram

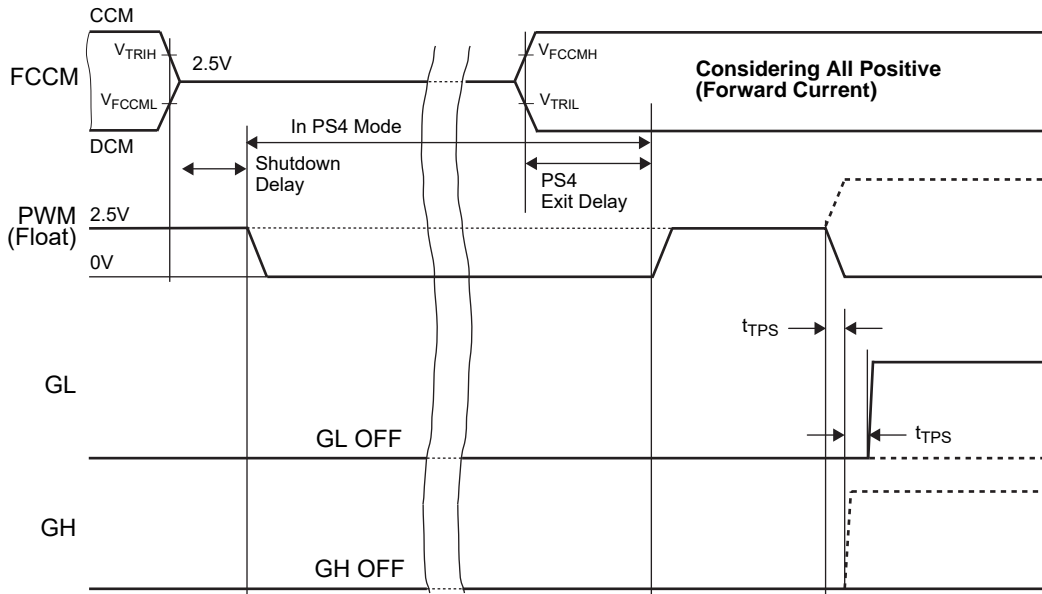


Figure 3. FCCM Logic during High Impedance at PWM Input

### Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{CC} = 5\text{V}$ , unless otherwise specified.

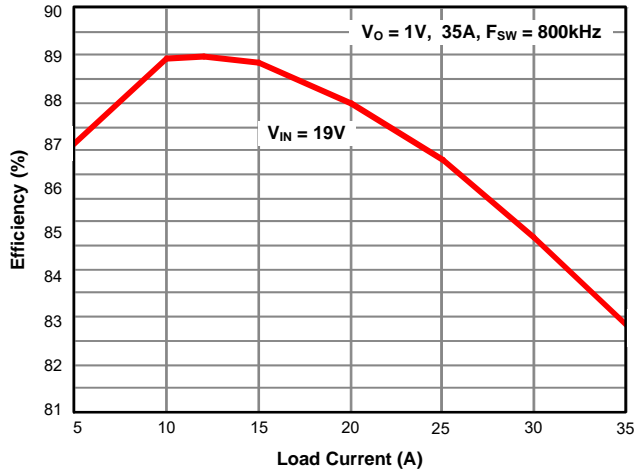


Figure 4. Efficiency vs. Load Current

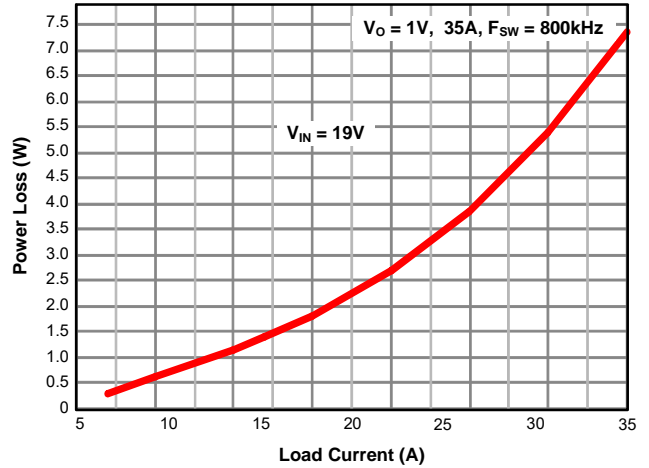


Figure 5. Power Loss vs. Load Current

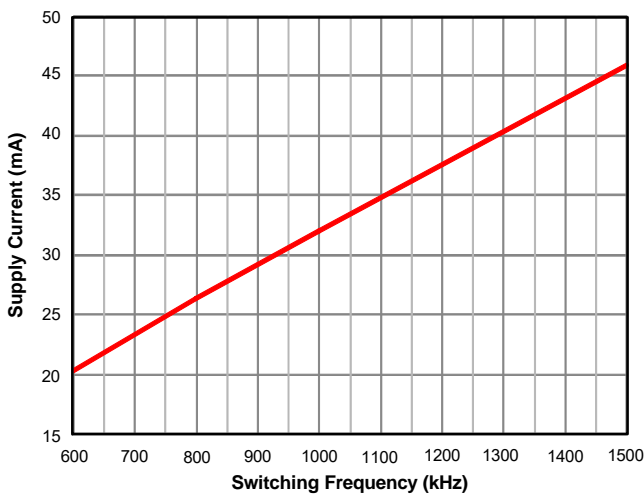


Figure 6. Supply Current vs. Switching Frequency

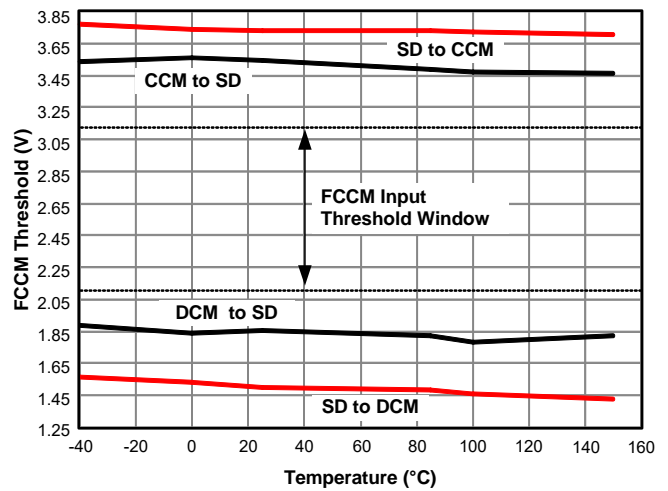


Figure 7. FCCM Input Threshold vs. Temperature

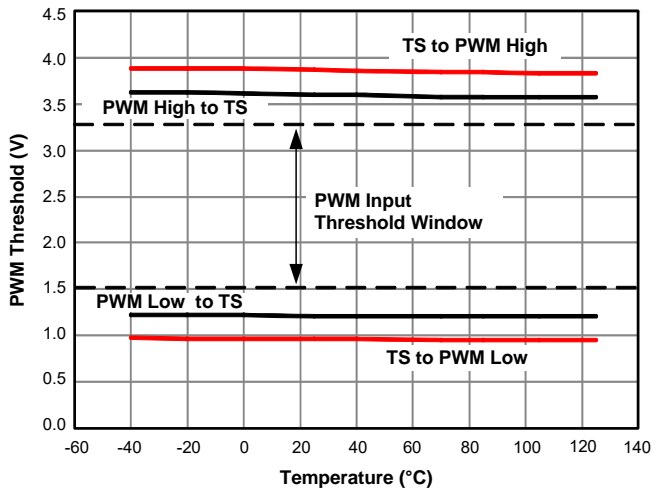


Figure 8. PWM Threshold vs. Temperature

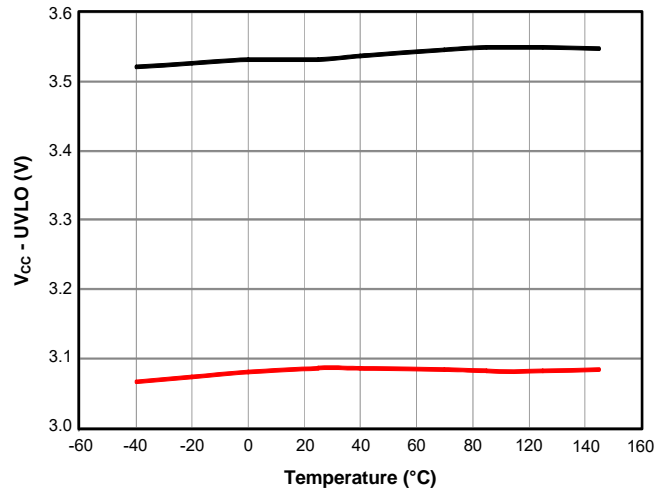


Figure 9.  $V_{CC}$  UVLO vs. Temperature



### Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{CC} = 5\text{V}$ , unless otherwise specified.

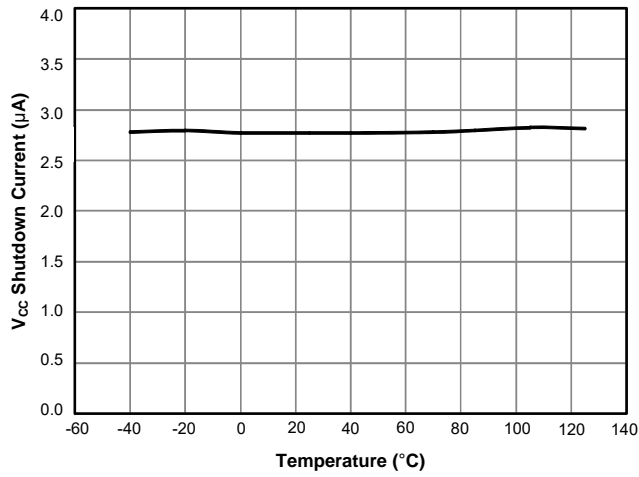


Figure 10. V<sub>CC</sub> Shutdown Current vs. Temperature

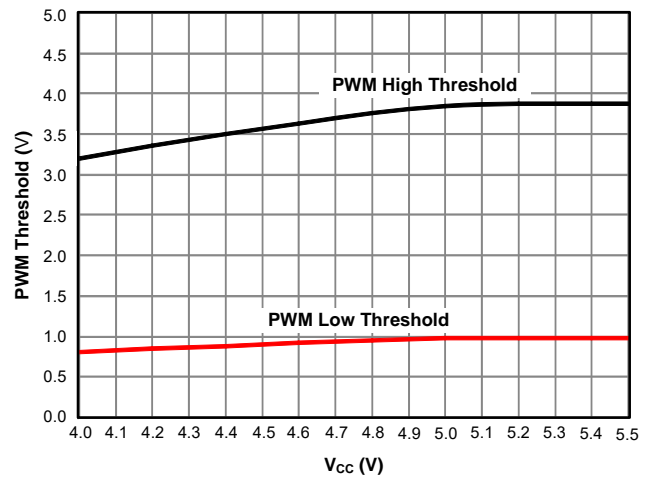


Figure 11. PWM Threshold vs. V<sub>CC</sub>

## Application Information

AOZ5547QI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuits. A number of desirable features make AOZ5547QI a highly versatile power module. The MOSFETs are individually optimized for efficient operation on either high side or low side switches in a low duty cycle synchronous buck converter. A high current driver is also integrated in the package which minimizes the gate drive loop and results in extremely fast switching. The modules are fully compatible with Intel DrMOS specification IMVP8 in form fit and function.

### Powering the Module and the Gate Drives

An external supply  $V_{CC}$  of 5V is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The integrated gate driver is capable of supplying large peak current into the Low Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 4.7 $\mu$ F or higher is recommended from  $V_{CC}$  to PGND. For effective filtering it is strongly recommended to directly connect this capacitor to PGND (pin 21).

The BOOT supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between BOOT (Pin 3) and the switching node PHASE (Pin 5). It is recommended that this capacitor  $C_{boot}$  be connected as close as possible to the device across pins 3 and 5. Boost switch is integrated into the package. A resistor in series with  $C_{boot}$  can be optionally used by designers to slow down the turn on speed of the High-Side MOSFET. Typically, values between 1 $\Omega$  to 5 $\Omega$  is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

### Under-Voltage Lockout

In a UVLO event, both GH and GL outputs are actively held low until adequate gate supply becomes available. The under-voltage lockout is set to 3.5V with a 400mV hysteresis. The AOZ5547QI must be powered up before the PWM input is applied.

Since the PWM control signals are provided typically from an external controller or a digital processor, extra care must be taken during start up. It should be ensured that PWM signal goes through a proper soft start sequence to minimize in-rush current through the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable

consequences as explained below. In general it should be noted that AOZ5547QI is a combination of two MOSFETs with an IMVP8 compliant driver, all of which are optimized for switching at the highest efficiency. Other than UVLO, it does not have any monitoring or protection functions built in. The PWM controller should be designed in to perform these functions under all possible operating and transient conditions.

### Input Voltage $V_{IN}$

AOZ5547QI is rated to operate over a wide input range of 4.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply very close to package leads with X7R or X5R quality surface mount ceramic capacitors.

The High-Side MOSFET in AOZ5547QI is optimized for fast switching with low duty ratios. It has ultra low gate charges which have been achieved as a trade off with higher RDS(ON) value. When the module is operated at low  $V_{IN}$  the duty ratio will be higher and conduction losses in the High-Side MOSFET will also be correspondingly higher. This will be compensated to some extent by reduced switching losses. The total power loss in the module may appear to be low even though in reality the High-Side MOSFET losses may be disproportionately high. Since the two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation, the High-Side MOSFET may be much hotter than the Low-Side MOSFET. It is recommended that worst case junction temperature be measured and ensured to be within safe limits when the module is operated with high duty ratios.

### PWM Input

AOZ5547QI is offered to interface with PWM logic compatible with 5V (TTL). Refer to Figure 1 for the timing and propagation delays between the PWM input and the gate drives.

The PWM is also a tri-state compatible input. When the input is high impedance or unconnected both the gate drives will be off and the gates are held active low. The PWM Threshold Table in Table 1 lists the thresholds for high and low level transitions as well as tri-state operation. As shown in Figure 2, there is a hold off delay between the corresponding gate drive is pulled low. This delay is typically 150ns and intended to prevent spurious triggering of the tri-state mode which may be caused either by noise induced glitches in the PWM waveform or slow rise and fall times.

**Table 1. PWM Input and Tri-State Thresholds**

| Thresholds → | V <sub>PWMH</sub> | V <sub>PWML</sub> | V <sub>TRIH</sub> | V <sub>TRIL</sub> |
|--------------|-------------------|-------------------|-------------------|-------------------|
| AOZ5547QI    | 4.1 V             | 0.7 V             | 1.5 V             | 3.5 V             |

**Note:** See Figure ure 2 for propagation delays and tri-state window.

**Diode Mode Emulation of Low Side MOSFET (FCCM)**

AOZ5547QI can be operated in the diode emulation or skip mode using the FCCM pin. This is useful if the converter has to operate in asynchronous mode during start up, light load or under pre bias conditions. If FCCM is taken high, the controller will use the PWM signal as reference and generate both the high and low side complementary gate drive outputs with the minimal delays necessary to avoid cross conduction. When the pin is taken low the HS MOSFET drive is not affected but diode emulation mode is activated for the LS MOSFET. See Table 2 for a comprehensive view of all logic inputs and corresponding drive conditions. A high impedance state at the FCCM pin shuts down the AOZ5547QI.

**Function of FCCM When Signal is Rising**

**FCCM = 0V**

1. The power stage is enabled and in DCM (Discontinuous Conduction Mode).
2. GH and GL will follow PWM signal
3. Zero Current Detection (ZCD) is enabled. When VSWH = 4mV and MIN\_ON expires, ZCD will trigger state machine to turn off GL. If VSWH reaches 4mV before than MIN\_ON, MIN\_ON time takes priority and will continue until this time period has completed.

**FCCM = 0V to 2.1V**

1. GH and GL will turn off after shutdown delay (2.5µs).

**FCCM = Tri-State Window**

1. Input to FCCM is high impedance.
2. An internal buffer clamps FCCM to 2.5V.
3. GH and GL remain Off and ignore PWM signal.

**FCCM = Tri-State to 3.9V (Fast Ramping)**

1. The power stage is in CCM (Continuous Conduction Mode)
2. GH and GL will follow PWM command
3. ZCD: is disabled

**FCCM = 5V**

1. The power stage is in CCM (Continuous Mode of Operation)
2. Zero Current Detection (ZCD) is disabled

3. GH and GL follow PWM signal:

PWM = Logic H → GH = H, GL = L

PWM = Logic L → GH = L, GL = H

4. No detection for direction of inductor current
5. No detection for Voltage Level at VSWH node

**Function of FCCM When Signal is Falling**

**FCCM = 5V → 3.1V**

1. Re-enter shutdown mode
2. Shutdown delay: 2.5µs
3. Occurs when Controller FCCM output enter high impedance state

**FCCM = Tri-State Window**

**(Ramp down window is 3.1 to 1.2V)**

1. FCCM will be internally clamped to 2.5V
2. Remains in Shutdown Mode

**FCCM = Tri-State → 1.2V**

**(250 to 300mV lower than the DCM → TS threshold)**

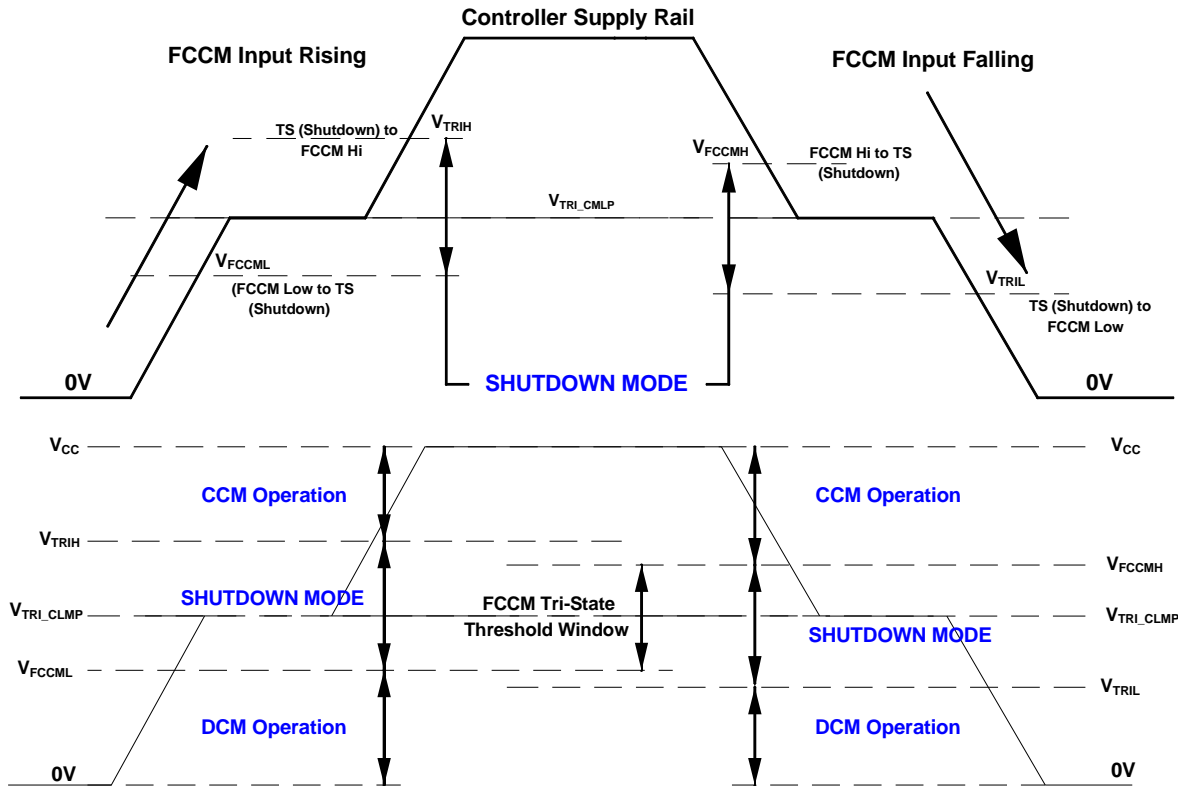
1. Re-enable power stage
2. Controller pulls down on FCCM pin exiting shutdown mode into DCM
3. Enable Delay: 5µs
4. Re-enable ZCD

**Table 2. Control Logic Truth Table**

| FCCM      | PWM       | GH | GL      |
|-----------|-----------|----|---------|
| L         | L         | L  | L (ZCD) |
| L         | H         | H  | L       |
| H         | L         | L  | H       |
| H         | H         | H  | L       |
| L         | Tri-State | L  | L       |
| H         | Tri-State | L  | L       |
| Tri-State | X         | L  | L       |

**Note:** Diode emulation mode is activated when FCCM pin is held low.

### FCCM Timing Diagram and Truth Table



| FCCM      | ZCD | PWM   | VSWH             | GH | GL         | Main Inductor Current Direction                                 |
|-----------|-----|-------|------------------|----|------------|---|
| 0V        | ON  | L     | <-4mV            | L  | L          | Forward Current   |
| 0V        |     | L     | Equal -4mV       | L  | MinOn Time | VSWH= -(R <sub>dson</sub> x I <sub>L</sub> <sub>FORWARD</sub> ) |
| 0V        |     | Tri-S | V <sub>OUT</sub> | L  | L          | Don't Care  |
| 0V        |     | H     | V <sub>IN</sub>  | H  | L          | Forward Only  |
| 5V        | OFF | L     | X                | L  | H          | Bi-Directional  |
| 5V        |     | Tri-S | V <sub>OUT</sub> | L  | L          | Forward (Body)  |
| 5V        |     | H     | V <sub>IN</sub>  | H  | L          | Bi-Directional  |
| Tri-State |     | X     | V <sub>OUT</sub> | L  | L          | Don't Care  |

Figure 12. FCCM Timing Diagram and Truth Table

## Gate Drives

AOZ5547QI has an internal high current high speed driver that generates the floating gate drive for the High-Side MOSFET and a complementary drive for the Low-Side MOSFET.

Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. An internal shoot through protection scheme ensures that neither MOSFET turns on while the other one is still conducting, thereby preventing shoot through condition of the input current. When the PWM signal makes a transition from High to Low or Low to High, the corresponding gate drive GH or GL begins to turn off. The adaptive timing circuit monitors the falling edge of the gate voltage and when the level goes below 1V, the complementary gate driver is turned on. The dead time between the two switches is minimized, at the same time preventing cross conduction across the input bus. The adaptive circuit also monitors the switching node VSWH and ensures that transition from one MOSFET to another always takes place without cross conduction, even under transient and abnormal conditions of operation.

The gate pins GH and GL are brought out on pins 4 and 19 respectively. However these connections are not made directly to MOSFET gate pads and their voltage measurement may not reflect the actual gate voltage applied inside the package. The gate connections are primarily for functional tests during manufacturing and no connections should be made to them in the application.

## PCB Layout Guidelines

AOZ5547QI is a high current module rated for operation up to 2MHz. This requires extremely fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds are achieved, correspondingly high levels of  $dv/dt$  and  $di/dt$  will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the area of the primary switching current loop, formed by the High-Side MOSFET, Low-Side MOSFET and the input bypass capacitor  $C_{in}$ . The PCB design is somewhat simplified because of the optimized pin out in AOZ5547QI. The bulk of  $V_{IN}$  and PGND pins are located adjacent to each other and the input bypass capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by Low-Side MOSFET, output inductor and output capacitor  $C_{out}$

is the next critical parameter, this requires second layer or "Inner 1" should always be an uninterrupted GND plane with sufficient GND vias placed as close as possible to by-pass capacitors GND pads.

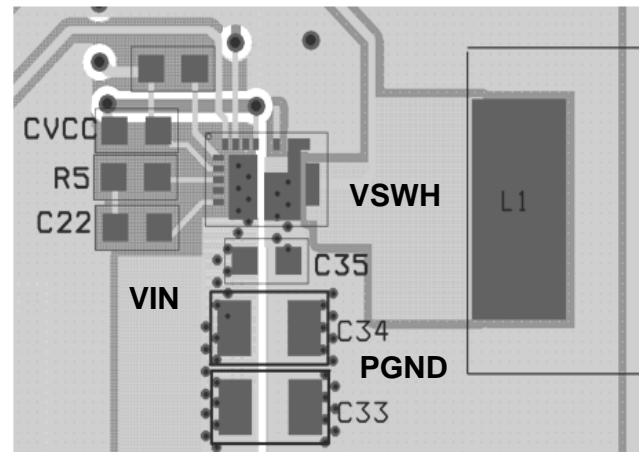


Figure 13. Top Layer of Demo Board,  $V_{IN}$ , VSWH and PGND Copper Planes

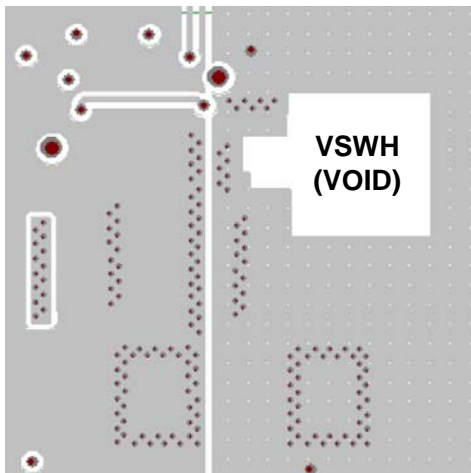
As shown on Figure 13, the top most layer of the PCB should comprise of uninterrupted copper flooding for the primary AC current loop which runs along the  $V_{IN}$  copper plane originating from the bypass capacitors C33, C34 and C35 which are mounted to a large PGND copper plane, also on the top most layer of the PCB. These copper planes also serve as heat dissipating elements as heat simply flows down to the  $V_{IN}$  exposed pad and onto the top layer  $V_{IN}$  copper plane which fans out to a wider area moving away from the 3.5x5 QFN package. Adding vias will only help transfer heat to cooler regions of the PCB board through the other 3 layers (if 4 layer PCB is used) beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

Due to the optimized bonding technique used on the AOZ5547QI internal package, the  $V_{IN}$  input capacitors are optimally placed for AC current activities on both the primary and secondary current loops. The return path of the current during the secondary period flows through a non interrupted PGND copper plane that is symmetrically proportional to the  $V_{IN}$  copper plane.

Due to the PGND exposed pad, heat is optimally dissipated simply by flowing down through the vertically structured lower MOSFET, through the exposed PGND pad and down to the PCB top layer PGND copper plane that also fans outward, moving away from the package.

As the primary and secondary AC current loops move through  $V_{IN}$  to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dts produced through the in package parastics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L1 is mounted to, is sized just so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH copper plane on the top layer is voided and the shape of this void is replicated descending down through the rest of the layers as shown on Figure 14 which is the bottom layer of the PCB as an example.



**Figure 14. Bottom Layer PCB Layout with VSWH Copper Plane Voided on Descending Layers**

The AOZ5547QI can be operated at a switching frequency of up to 2MHz. This implies that the inherent capacitive parameters of the High Side and Low Side MOSFETs need to be charged and discharge on each and every cycle. Due to the back and forth conduction of these AC currents flowing in and out of the Input Capacitors, the exposed pads ( $V_{IN}$  and PGND) would tend to heat up, hence requiring thermal venting.

Positioning vias through the landing pattern of the  $V_{IN}$  and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer.

The exposed pads dimensional footprint of the 3.5x5 QFN package is shown on Figure13. For optimal thermal relief, it is recommended to fill the PGND and  $V_{IN}$  exposed landing pattern with 10mil diameter vias.

10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

#### **Adding Vias Through Exposed Pads Landing Pattern**

The AOZ5547QI can be operated at a switching frequency of up to 2MHz. This implies that the inherent capacitive parameters of the High Side and Low Side MOSFETs need to be charged and discharged on each and every cycle. Due to the back and forth conduction of these AC currents flowing in and out of the Input Capacitors, the exposed pads ( $V_{IN}$  and PGND) would tend to heat up, hence requiring thermal venting. Positioning vias through the landing pattern of the  $V_{IN}$  and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer.

The exposed pads dimensional footprint of the 3.5x5 QFN package is shown on Figure 15. For optimal thermal relief, it is recommended to fill the PGND and  $V_{IN}$  exposed landing pattern with 10mil diameter vias. 10mil via diameter is a commonly used, as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.



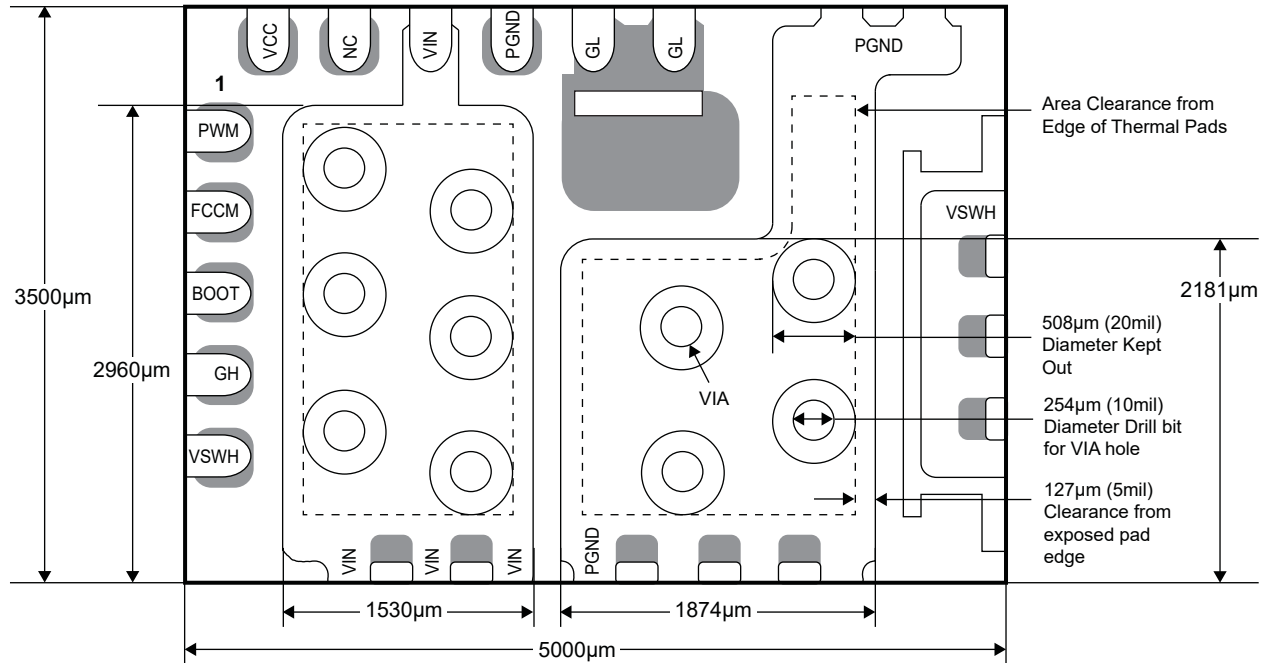


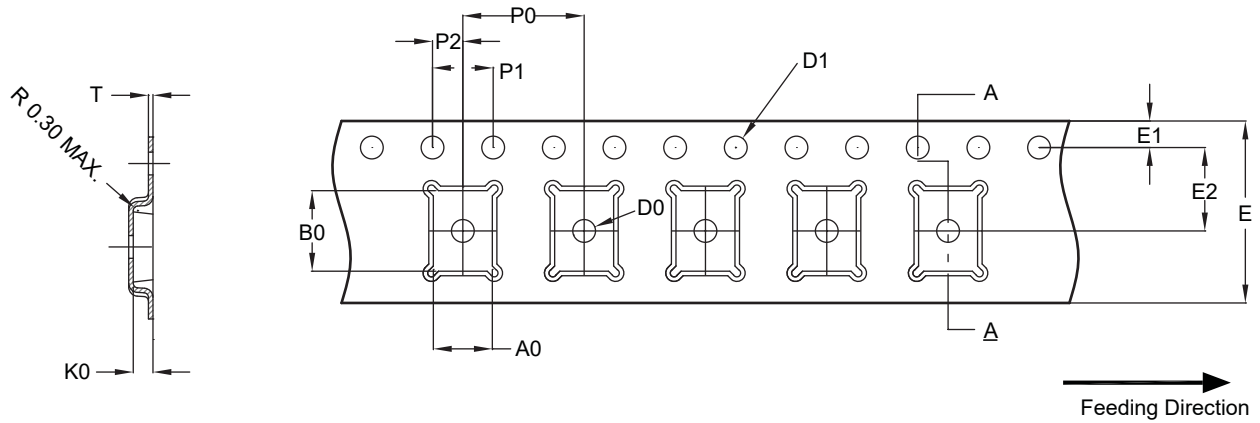
Figure 15. Exposed Pad Land Pattern and Recommended Via Placements





### Tape and Reel Dimensions, QFN\_3.5x5\_24L\_EPS\_2

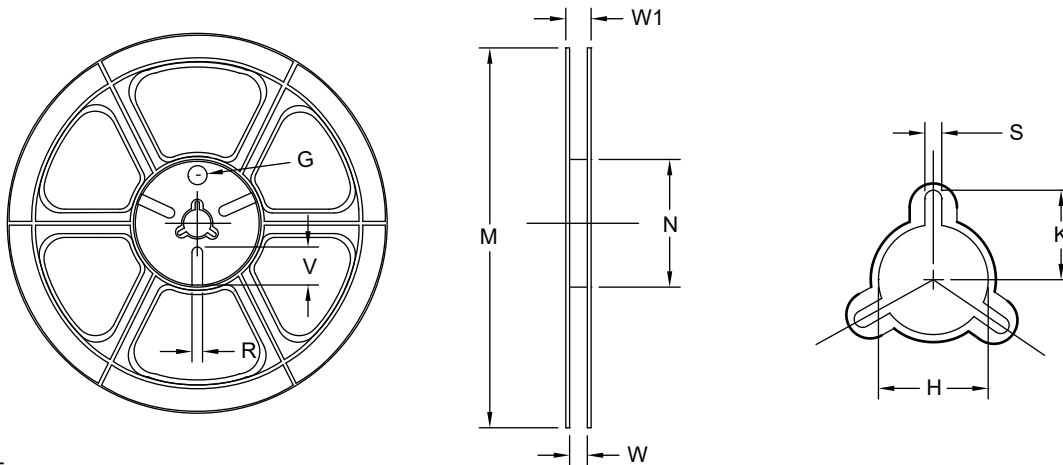
#### Carrier Tape



UNIT: mm

| Package            | A0            | B0            | K0            | D0           | D1                   | E             | E1            | E2            | P0            | P1            | P2            | T             |
|--------------------|---------------|---------------|---------------|--------------|----------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| QFN3.5x5<br>(12mm) | 3.89<br>±0.10 | 5.31<br>±0.10 | 1.30<br>±0.10 | 1.50<br>MIN. | 1.50<br>+0.1<br>-0.0 | 12.0<br>±0.30 | 1.75<br>±0.10 | 5.50<br>±0.05 | 8.00<br>±0.10 | 4.00<br>±0.10 | 2.00<br>±0.05 | 0.30<br>±0.05 |

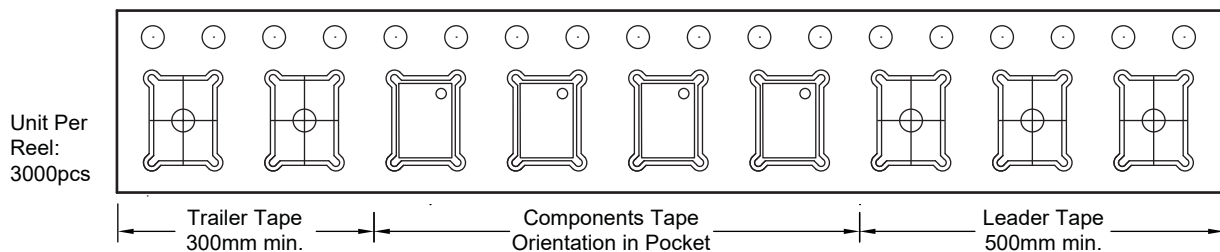
#### Reel



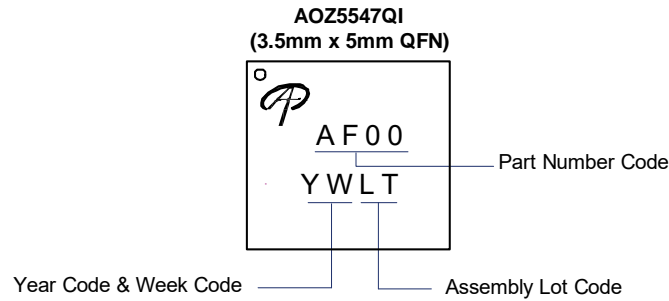
UNIT: mm

| Tape Size | Reel Size | M             | N               | W                    | W1                   | H               | S         | K   | G   | R   | V   |
|-----------|-----------|---------------|-----------------|----------------------|----------------------|-----------------|-----------|-----|-----|-----|-----|
| 12mm      | Ø330      | Ø330<br>±2.00 | Ø101.6<br>±2.00 | 12.40<br>+2.00/-0.00 | 12.40<br>+3.00/-0.20 | Ø13.20<br>±0.30 | 1.70-2.60 | --- | --- | --- | --- |

#### Leader/Trailer and Orientation



## Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.