AOZ9510QI

30V/20A Smart Motor Module Evaluation Board User Guide

General Description

The AOZ9510QI is an integrated half-bridge gate driver with smart functions. The device includes one half-bridge gate driver capable of driving high-side and low-side N-channel MOSFETs, using two AOZ9510QI for single phase motor driver and three AOZ9510QI for three-phase motor drivers.

The device features multiple protection functions such as VCC UVLO and over-temperature protection. Moreover, AOZ9510QI provides an adjustable gate drive sink and source current control. By doing this control, users can optimize performances of EMI and efficiency.

The AOZ9510QI is available in a 4mm×4mm QFN-23L package and is rated over a -40°C to +85°C ambient temperature range.

Features

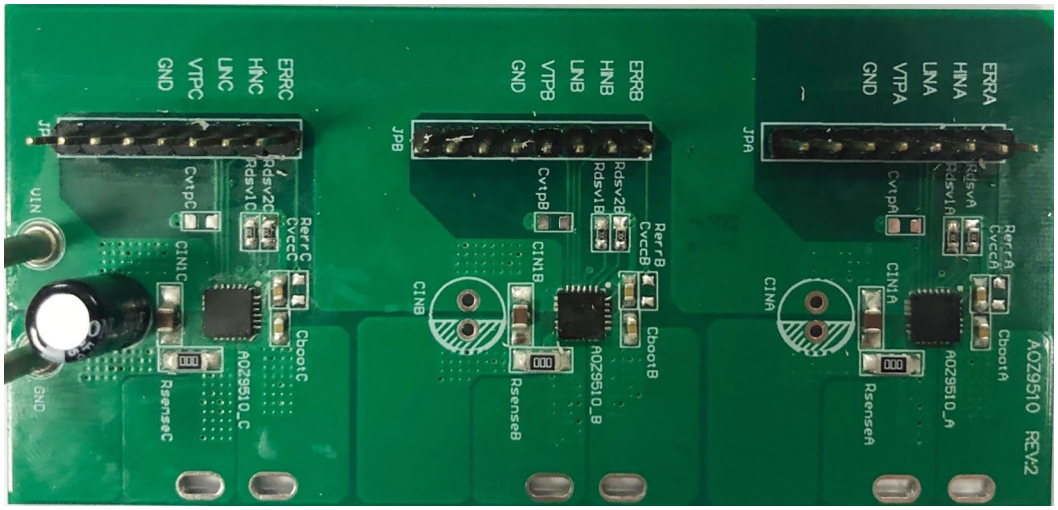
- Input voltage range from 10.8V to 30V
- Maximum output current 20A
- Adjustable gate drive sink/source current
- Support 100% PWM operation
- Integrated bootstrap diode
- Low $R_{DS(ON)}$ internal NFETs
  - 6mΩ for Both HS/LS
- Thermal protection
- Thermally enhanced 23-pin 4×4 QFN

Applications

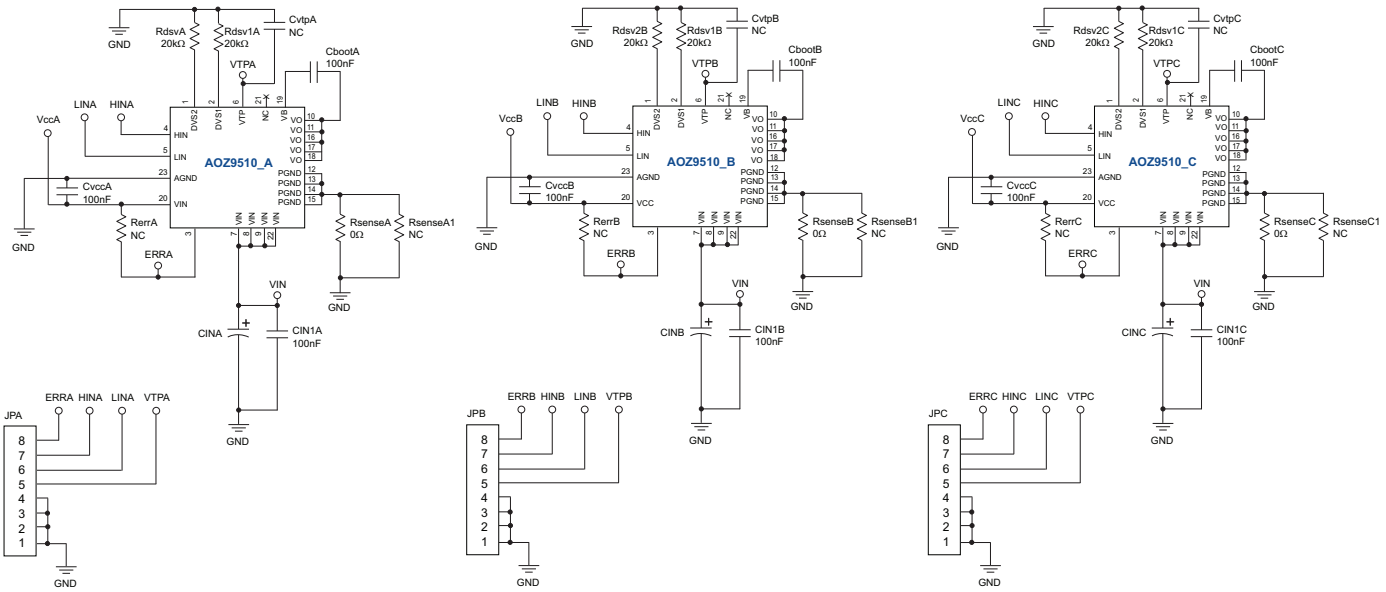
- BLDC motor drive
- Fans and pumps
- Power tools

Green Product

Evaluation Board



Evaluation Board Schematics



BOM of AOZ9510QI

Reference Designator	Part Number	Description
C_{vccA}, C_{vccB}, C_{vccC}	GRM188R71H104KA01D	Cap, 100nF, 0603, 50V, X7R, 10%
C_{bootA}, C_{bootB}, C_{bootC}	GRM188R71H104KA01D	Cap, 100nF, 0603, 50V, X7R, 10%
C_{IN1A}, $C_{IN1B,}$, C_{IN1C}	0805B104K500CT	Cap, 100nF, 0805, 50V, X7R, 10%
C_{INC}		Electrolytic capacitor 33μF/50V
RdvsA, RdvsB, RdvsC		20kΩ, 0603
ReerA, RerrB, ReerC C_{INA}, C_{INB}, C_{vtpB}, C_{vtpC}		NC
RsenseA, RsenseB, RsenseC		0Ω

Quick Start Guide

1. Connect the DC power supply to V_{IN} and GND connects. Set the DC power supply voltage between the operating range of 10.8V and 30V.
2. Connect the terminals of load to V_O and GND connectors.
3. Use oscilloscope or voltage meter to check internal LDO V_{CC} voltage on capacitors C_{vccA}, C_{vccB}, C_{vccC}.
4. Use HIN/LIN pins to control each high-side and low-side switching.
5. When monitoring the V_O switching waveform, directly probe across the V_O-PGND trace to minimize inductive ringing.

PCB Layout

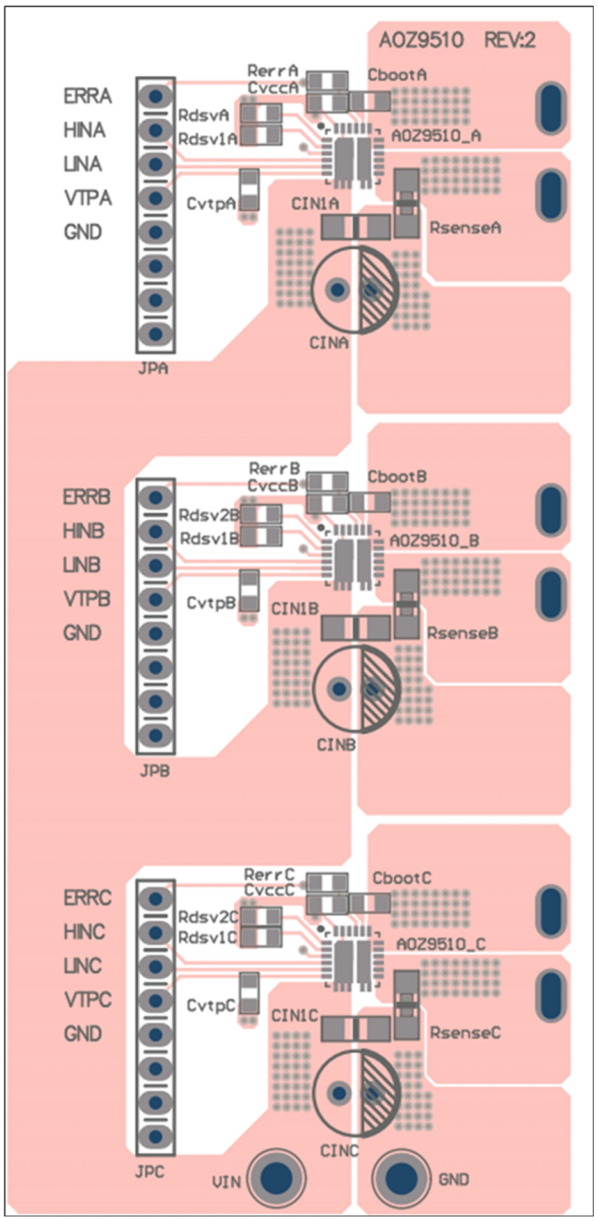


Figure 1. Top Layer

PCB Layout

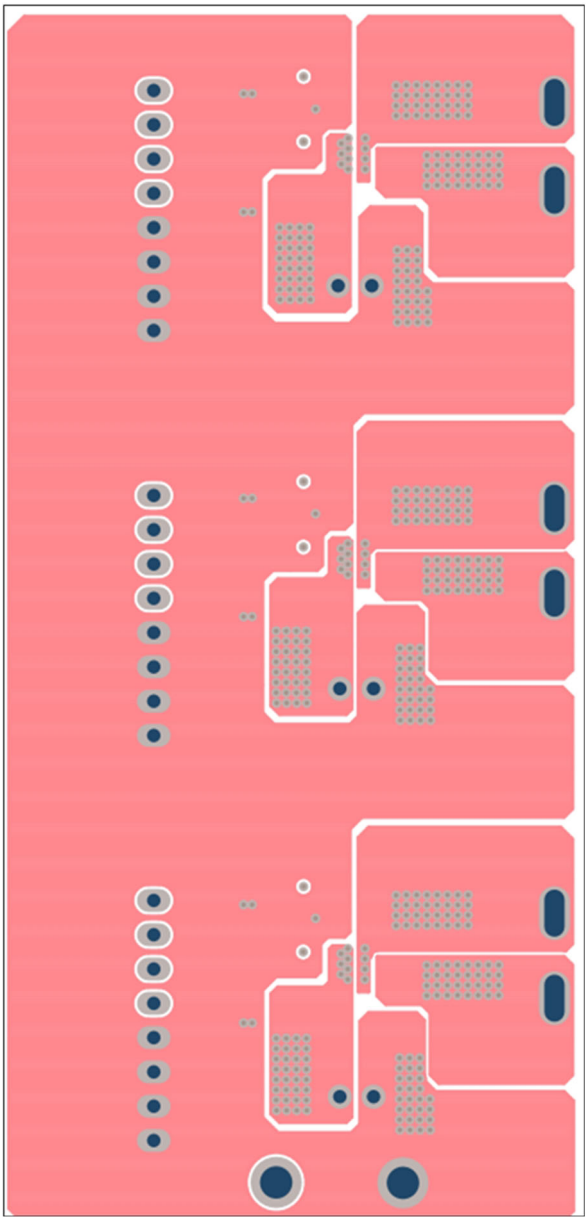


Figure 2. Mid-Layer 1

PCB Layout

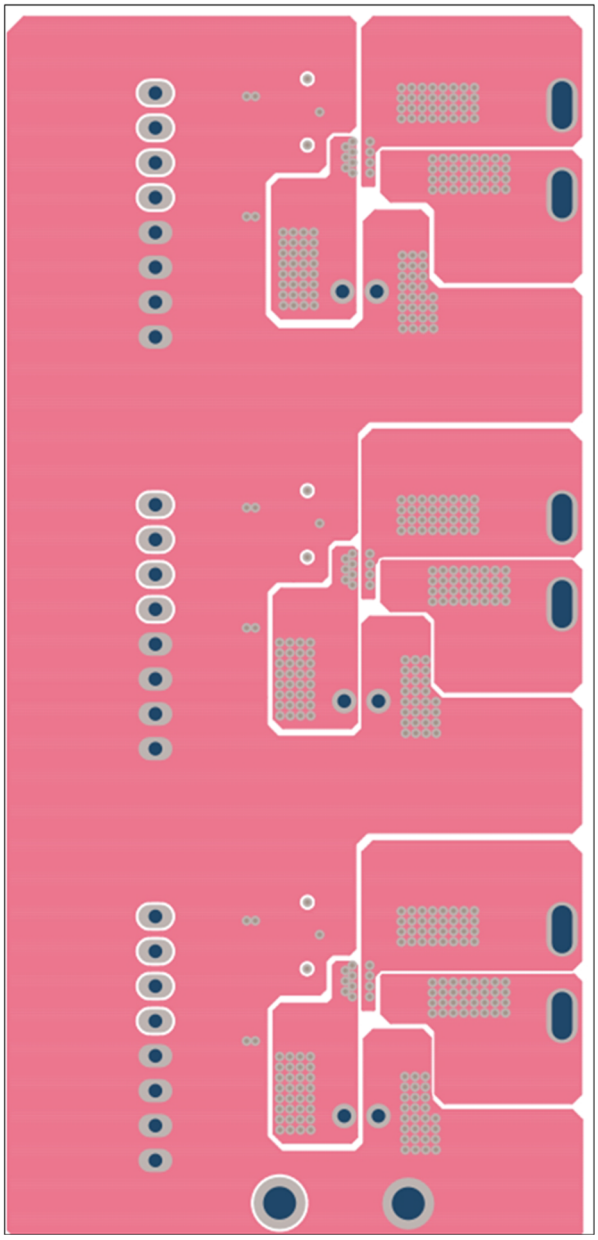


Figure 3. Mid-Layer 2

PCB Layout

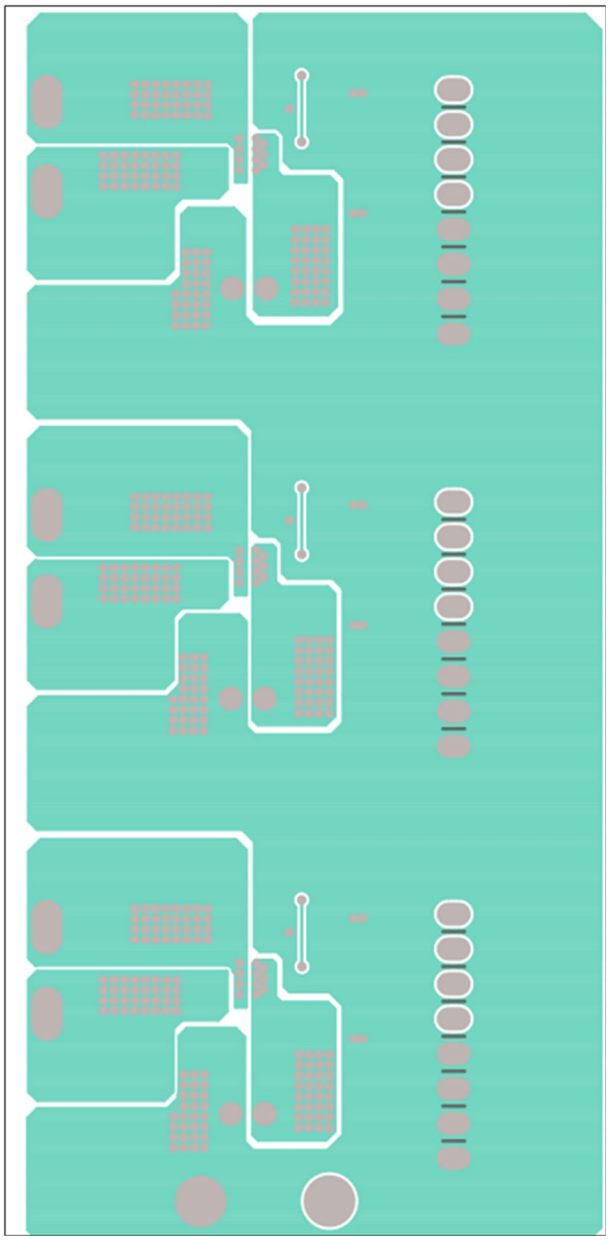


Figure 4. Bottom Layer

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