ALPHA & OMEGA SEMICONDUCTOR

AOZ71026QI

Two Rails Hybrid Low I_Q Intel IMVP Controller for CPU

General Description

The AOZ71026QI is a high performance digital & analog hybrid multiphase buck controller designed in compliance with Intel IMVP8, 9, and 9.1/9.2 platform specifications. It provides two output rails (up to 4 + 2) and supports 3 separate SVID domains. Up to 4 phases for core voltage domain (IA) and 2 phases for graphics voltage domain (GT) as well as the P_{SYS} domain's reporting functions, incorporated into a single SVID interface. AOS offers a novel AOS Advanced Transient Modulator (A^2TM). It combines an advanced variable frequency hysteretic peak current mode control with proprietary phase current sensing scheme for fast transient response and low system cost. The control loop enhances light-load efficiency by seamlessly entering DCM mode of operation.

The AOZ71026QI is equipped with SMBus digital Interface enabling register programming for tuning and configuration to minimize the system components and eliminate the need for manual solder rework on the system board. Programmability can be done either by AOS GUI or customized ECS into the controller's built-in RAM. The controller also provides MTP to store register settings once the configuration is finalized.

Combined with AOS high performance DrMOS, the AOZ71026QI provides a complete power solution for Intel IMVP9.1/9.2 mobile platform VCORE applications. AOZ71026QI comes in a 6 mm x 6 mm 48-pin QFN package.

The AOZ71026QI controller features very low power consumption while still enabling digital interface control. This unique "Hybrid Digital" control scheme enables low quiescent power consumption in all power states as defined by the Intel IMVP9.1 platform to enable long system run times in battery life workloads.

The AOZ71026QI provides complete protection and warning functions including UVP, OVP, OCP and OTP. Fault protection behavior can be easily programmed through SMBus. AOZ71026QI also offers real time telemetry information via SMBus for V_{IN}, V_{OUT}, temperature, output currents, power states as well as PSYS/VSYS/IAUX pins reporting via SMBus.

Features

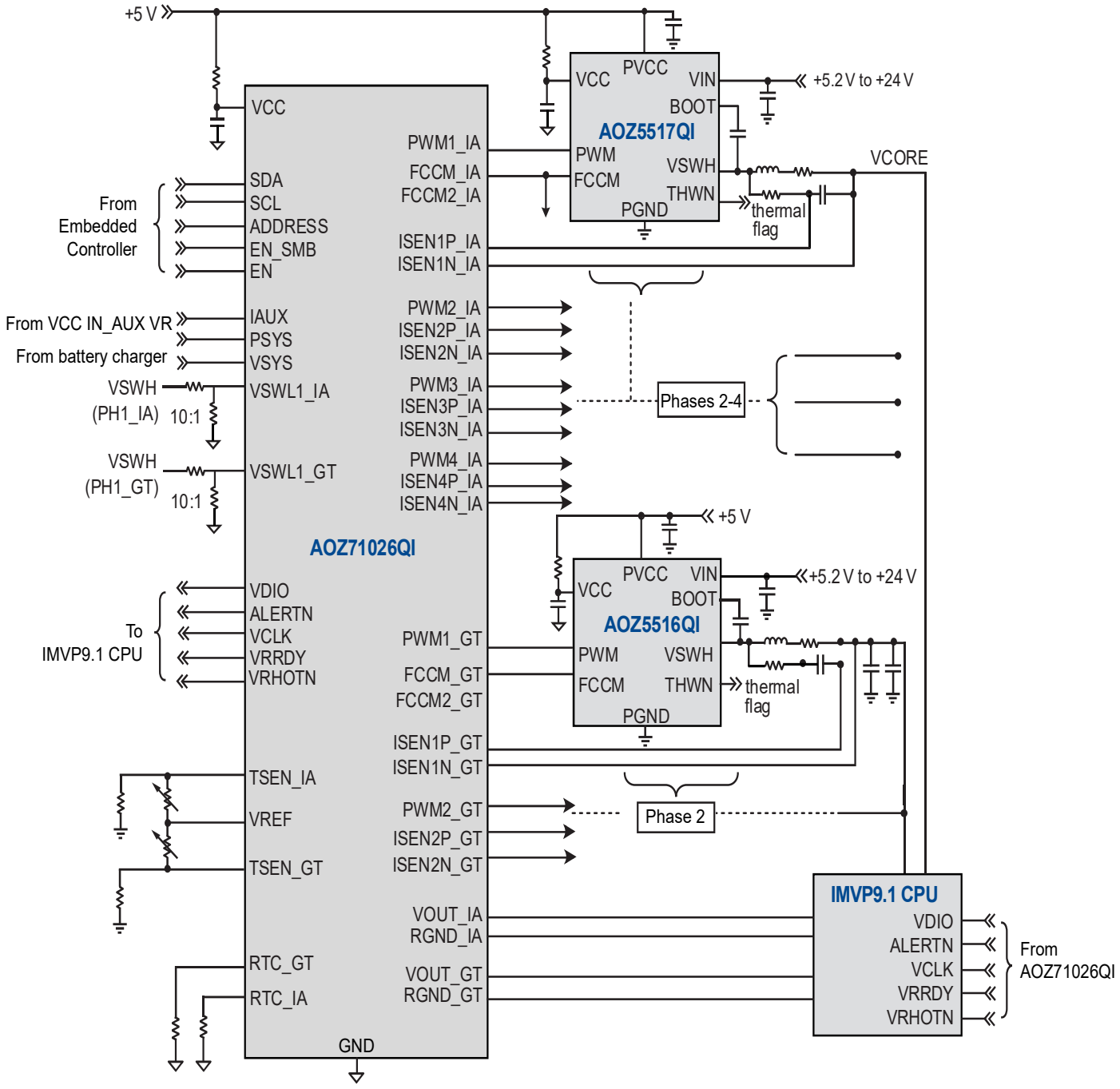
- 5.2 V to 24 V V_{IN} input supply voltage
- Dual output rails: 4/3/2/1 + 2/1 phases
- Digital & analog hybrid controller with SMBus programmability and lowest power consumption
- SVID Interface to CPU compliant with IMVP8, 9, and 9.1 /9.2 specifications
- Differential remote sensing to achieve 0.5% regulated V_{OUT} accuracy
- Low quiescent current: 1.95 mA at PS0 for 2+1 configuration
- 42 µA quiescent current at Intel PS4 state
- FCCM2 pin to lower power loss in unused phases in PS3 mode
- Supports multi-sourced industry standard DrMOS or driver + MOSFET power stages
- User friendly GUI for compensation and configurations with minimal external RC components.
- ECS programmability for configurations with Built-in MTP and RAM
- Proprietary, high performance AOS Advanced Transient Modulator (A^2TM) control scheme:
  - Variable frequency hysteretic peak current mode control gives fast transient response
  - Dynamic phase current balance
  - Excellent load-line control and phase current sensing
  - Seamless CCM to DCM control to maximize efficiency
- System Input Power Monitoring (both P_{SYS} and V_{SYS})
- 400 kHz to 1.1 MHz programmable switching frequency
- Acoustic Noise Suppression
- Output Under-Voltage Protection (UVP)
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- QFN6x6-48L package

Applications

- Notebook computers
- Memory and graphic cards
- Video game console

Green Product

Typical Application



Ordering Information

Part Number[1]	Junction Temperature Range	Package	Environmental
AOZ71026QI-xxx[2]	-40°C to +125°C	QFN6x6-48L	RoHS

Notes:
1. For each customer, the full PN already created for order is on the last page of this DS. Please refer to last page for more information.
2. "xxx" is the configuration code identifier (also called sub-part number) for the register settings stored in the internal non-volatile memory (NVM). Each "x" can be a value between 0 and 9 and A-Z (except I, J, O, Q). Please work with an AOS Sales/FAE to create this unique number. Each project or board might need to use different sub-PN as the register setting might be different.

Contact local sales office for full product datasheet.

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

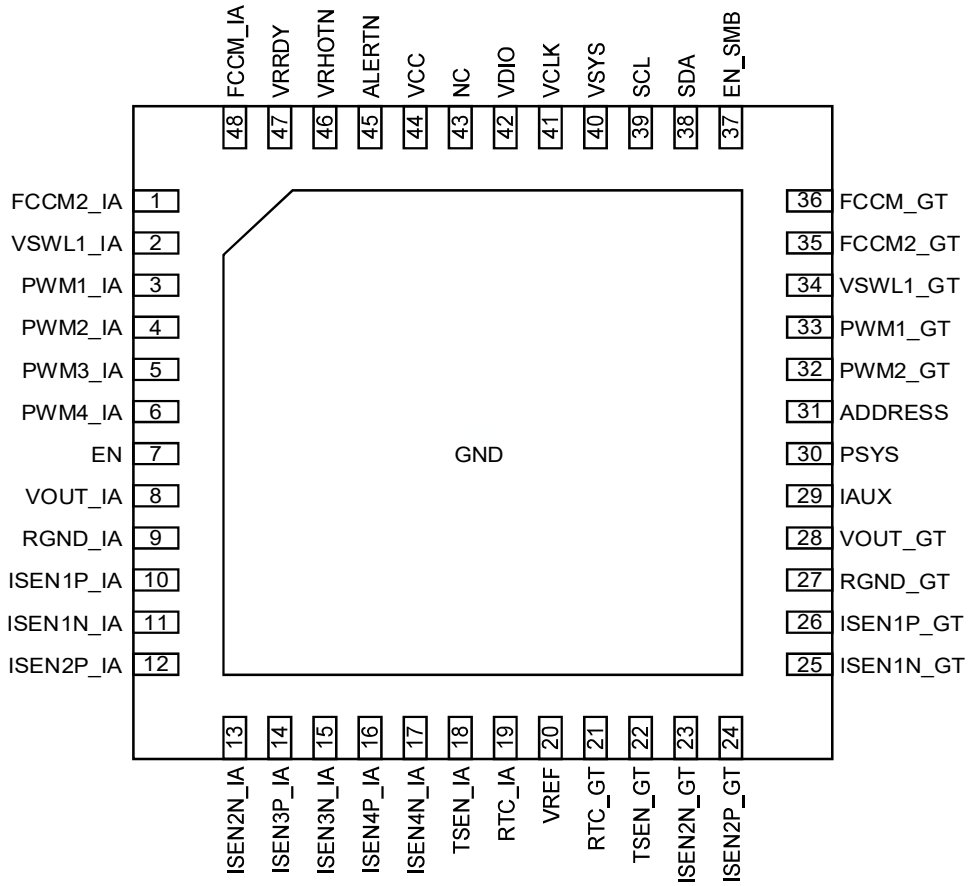


Figure 1. QFN 6x6-48L
(Top View)

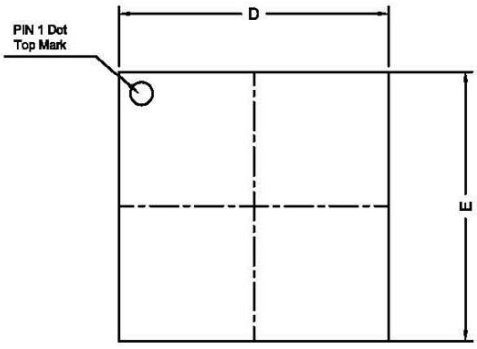
Pin Description

Pin Num	Pin Name	I/O	Pin Function
1	FCCM2_IA	O	Forced Continuous Current Mode for core domain. Connect to FCCM input of individual DrMOS on phases 2-N supplying power for core domain dedicated to low light operation. Continuous mode is active if FCCM is high. DrMOS is disabled if floating.
2	VSWL1_IA	I	Power conversion input voltage sensing for core domain. Connect to the switching node of phase 1 DrMOS through a 10:1 resistor divider.
3	PWM1_IA	O	Core voltage domain PWM signal for Phase 1. Connect to the PWM input of DrMOS.
4	PWM2_IA	O	Core voltage domain PWM signal for Phase 2. Connect to the PWM input of DrMOS.
5	PWM3_IA	O	Core voltage domain PWM signal for Phase 3. Connect to the PWM input of DrMOS.
6	PWM4_IA	O	Core voltage domain PWM signal for Phase 4. Connect to the PWM input of DrMOS.
7	EN	I	Logic input to enable the controller. Active logic high.
8	VOUT_IA	I	Remote CPU core voltage sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
9	RGND_IA	I	Remote CPU core ground sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
10	ISEN1P_IA	I	Positive node of core domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the center RC network across the inductor for DCR sensing.
11	ISEN1N_IA	I	Negative node of core domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the V_{OUT} terminal of the inductor for DCR sensing.
12	ISEN2P_IA	I	Positive node of core domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the center RC network across the inductor for DCR sensing.
13	ISEN2N_IA	I	Negative node of core domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the V_{OUT} terminal of the inductor for DCR sensing.
14	ISEN3P_IA	I	Positive node of core domain current feedback for droop regulation and output current monitoring for Phase 3. Connect to the center RC network across the inductor for DCR sensing.
15	ISEN3N_IA	I	Negative node of core domain current feedback for droop regulation and output current monitoring for Phase 3. Connect to the V_{OUT} terminal of the inductor for DCR sensing.
16	ISEN4P_IA	I	Positive node of core domain current feedback for droop regulation and output current monitoring for Phase 4. Connect to the center RC network across the inductor for DCR sensing.
17	ISEN4N_IA	I	Negative node of core domain current feedback for droop regulation and output current monitoring for Phase 4. Connect to the V_{OUT} terminal of the inductor for DRC sensing circuit.
18	TSEN_IA	I	Core domain temperature sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF.
19	RTC_IA	I	Core domain temperature gain sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF pin.
20	VREF	O	2.56V reference voltage output. Connect NTC thermistors from TSEN_IA and TSEN_GT to this pin.
21	RTC_GT	I	Graphics domain temperature gain sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF pin.
22	TSEN_GT	I	Graphics domain temperature sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF.
23	ISEN2N_GT	I	Negative node of graphics domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the V_{OUT} terminal of the inductor for DCR sensing.
24	ISEN2P_GT	I	Positive node of graphics domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the center RC network across the inductor for DCR sensing.
25	ISEN1N_GT	I	Negative node of graphics domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the V_{OUT} terminal of the inductor for DCR sensing.

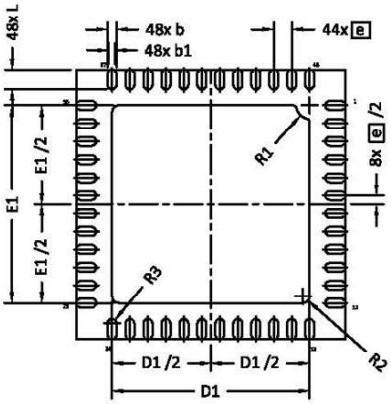
Pin Description

Pin Num	Pin Name	I/O	Pin Function
26	ISEN1P_GT	I	Positive node of graphics domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the center RC network across the inductor for DCR sensing.
27	RGND_GT	I	Remote CPU graphics ground sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
28	VOUT_GT	I	Remote CPU graphics voltage sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
29	IAUX	I	Current monitor input from VCCIN_AUX rail. Input analog signal will be converted to digital signal and communicated to the CPU through SVID Bus via the PSYS domain.
30	PSYS	I	System power monitor input from Battery Charger. Input analog signal will be converted to digital signal and communicate with CPU through SVID Bus via the PSYS domain.
31	ADDRESS	I	SMBus address select pin. Tie high for address 0x62, low for 0x26. Should neither of these be usable, the pin can also be left floating to give a factory configured default.
32	PWM2_GT	O	Graphics voltage domain PWM signal for Phase 2. Connect to the PWM input of DrMOS.
33	PWM1_GT	O	Graphics voltage domain PWM signal for Phase 1. Connect to the PWM input of DrMOS.
34	VSWL1_GT	I	Power conversion input voltage sensing for graphics domain. Connect to the switching node of phase 1 DrMOS through a 10:1 resistor divider.
35	FCCM2_GT	O	Forced Continuous Current Mode for graphics domain. Connect to FCCM input of individual DrMOS on phase 2 supplying power for graphics domain dedicated to low light operation. Continuous mode is active if FCCM is high. DrMOS is disabled if floating.
36	FCCM_GT	O	Forced Continuous Current Mode for graphics domain. Connect to FCCM input of Phase 1's DrMOS supplying power for graphics domain. Continuous mode is active if FCCM is high. Discontinuous mode is active is low. DrMOS is disabled if floating.
37	EN_SMB	I	SMBus enable input. Connect to VCC to allow SMBus register read/write.
38	SDA	I/O	SMBus data line. Open drain I/O. Connect a precision 1% resistor to VCC.
39	SCL	I/O	SMBus clock line, Open drain input. Connect a precision 1% resistor to VCC.
40	VSYS	I	System power monitor input voltage level from battery output. Input analog signal will be converted to digital signal and communicate with CPU through SVID Bus via the P_{SYS} domain.
41	VCLK	I/O	SVID clock line. Open drain input. Communication line to CPU.
42	VDIO	I/O	SVID data line. Open drain I/O. Communication line to CPU.
43	NC		No Connect.
44	VCC	I	Power supply for the controller. Connect a 1µF MLCC capacitor to GND.
45	ALERTN	I/O	VR Alert: Active low open drain output to CPU. Notification signal to indicate all SVID alert conditions.
46	VRHOTN	O	VR HOT: Active low open drain output to CPU. Notification signal to indicate the system temperature is too high.
47	VRRDY	O	VR Ready: Open drain output to CPU. Notification signal to indicate both core and graphics output voltage are ready.
48	FCCM_IA	O	Forced Continuous Current Mode for core domain. Connect to FCCM input of phase 1's DrMOS supplying power for core domain. Continuous mode is active if FCCM is high. Discontinuous mode is active is low. DrMOS is disabled if floating.

Package Dimensions, QFN6X6-48L



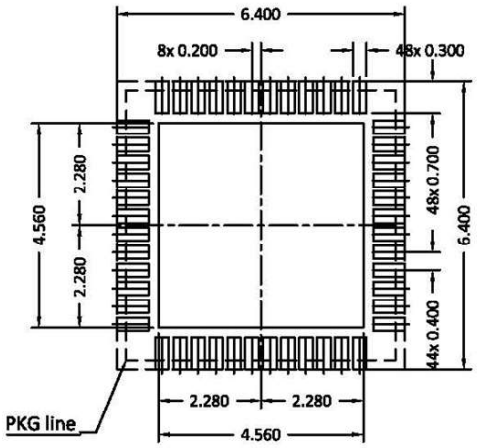
TOP VIEW



BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN



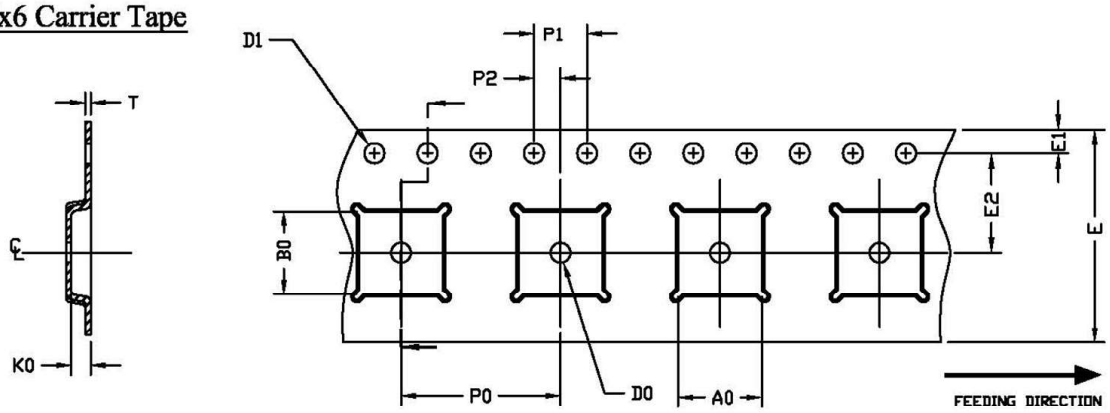
UNIT: mm

SYMBOLS	DIM. IN MILLIMETERS			DIM. IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.850	0.900	0.950	0.033	0.035	0.037
A1	0.000	---	0.050	0.000	----	0.002
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	0.140REF			0.007REF		
c	0.200REF			0.008REF		
D	5.900	6.000	6.100	0.232	0.236	0.240
D1	4.350	4.400	4.450	0.171	0.173	0.175
E	5.900	6.000	6.100	0.232	0.236	0.240
E1	4.350	4.400	4.450	0.171	0.173	0.175
L	0.400	0.450	0.500	0.016	0.018	0.020
R1	0.250	0.300	0.350	0.010	0.012	0.014
R2	0.100	0.150	0.200	0.004	0.006	0.008
R3	0.050	0.100	0.150	0.002	0.004	0.006
e	0.400BSC			0.016BSC		

NOTES:
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN6X6-48L

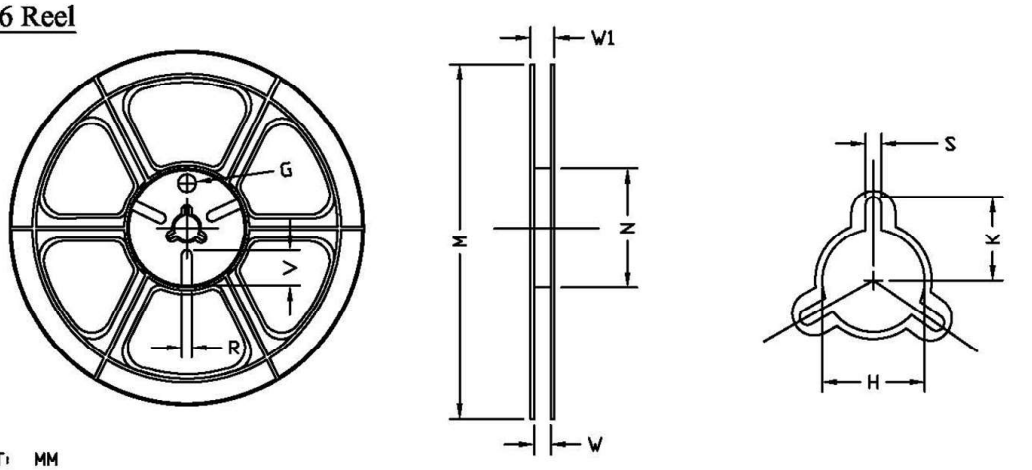
QFN6x6 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN6x6 (16 mm)	6.30 ±0.20	6.30 ±0.20	1.10 ±0.20	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	16.0 ±0.3	1.75 ±0.10	7.5 ±0.1	12.00 ±0.20	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

QFN6x6 Reel

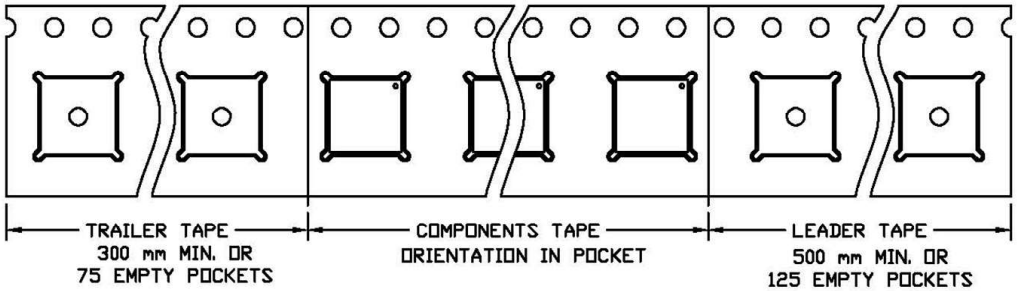


UNIT: MM

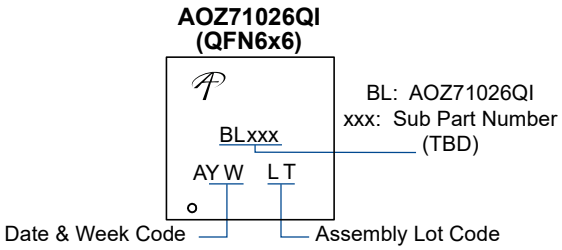
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
16 mm	ø330	ø330 MAX.	ø100 MIN.	16.4 $^{+2.0}_{-0.0}$	22.4 MAX.	ø13.0 $^{+0.5}_{-0.2}$	10.1 MIN.	1.5 MIN.	---	---	---

QFN6x6 Tape

Leader / Trailer & Orientation



Part Marking



Sub PN Marking	SKU	Project Descriptions	Full PN
xxx	ADL 28W Perf (3+2)		AOZ71026QI-xxx

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.