Power Topology and Analysis of 800 VDC Architectures to Support Next Generation AI Factory Infrastructure

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Introduction

Data center power demands are rapidly increasing due to the exponential growth of AI workloads. Traditional 54V in-rack distribution cannot support the megawatt (MW) scale racks expected in modern AI capable data centers. The transition to 800 VDC data center power infrastructure, as shown in Fig. 1, is being aggressively driven by hyperscalers due to its benefits in:

Scalability: Supports racks ranging from 100 kW to over 1 MW

Efficiency: Improves end-to-end efficiency by up to 5% compared to current 54 V systems

Copper Reduction: Less copper is needed due to less conduction current under 800V input.

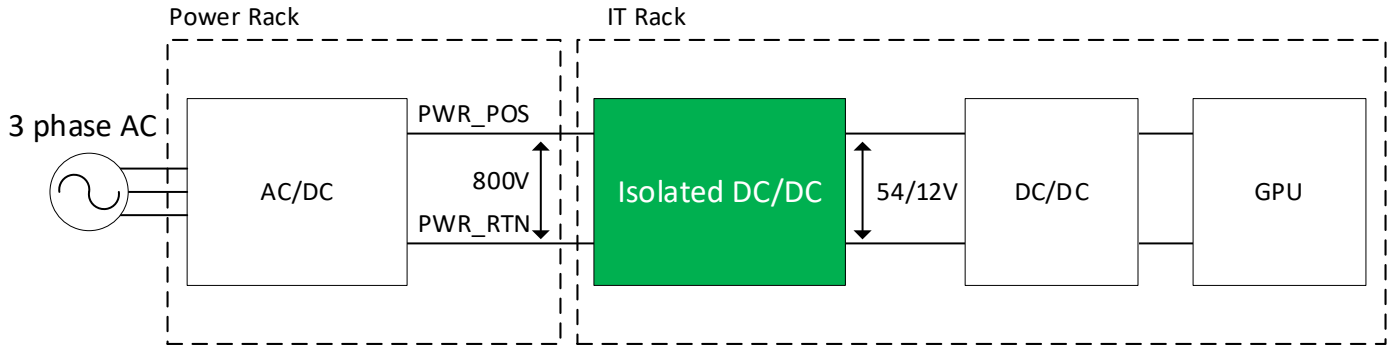

Fig.1 800 VDC distribution to IT racks and DC/DC conversion to 12 V for GPUs

AOS has a large power semiconductor portfolio, ranging from MOSFETs and SiC/GaN to power ICs. AOS has assembled a dedicated task force to provide a comprehensive 800V power delivery board (PDB) solution. In this white paper, we focus on the power stage converting from 800 VDC to 54V/12V bus voltage, which is subsequently used for downstream conversion from 54V to 12V or from 12V to POL. Three different topologies are proposed, each accompanied by AOS GaN, SiC, or MOSFET options. In future work, we will present

simulation results and subsequently provide complete system test results once a PDB hardware prototype is proposed.

I. Three phase half bridge LLC DCX resonant converter

A. Full bridge LLC converter

In the past, LLC resonant converters were widely used in DC/DC converter because of their soft-switching characteristics, namely zero-voltage switching (ZVS) across the full load range, zero-current switching (ZCS) of synchronous rectifiers, and a wide voltage gain range. However, conventional full-bridge LLC converters face challenges in meeting the increasing power requirements above 10 kW for AI servers. The three-phase LLC resonant converter evenly distributes power among three resonant tanks, as shown in Fig. 2, is preferred over full-bridge LLC now. Because of the 120° phase difference among the outputs of the three synchronous rectifiers, the output ripple frequency is six times the switching frequency. The reduced ripple current decreases the required filter capacitance on the output side and increases system power density. Three-phase LLC transformers can be configured with either Y-type or Delta-type connections. The choice between these two connections involves a trade-off between transformer winding loss and core loss. The Y-type connection reduces the transformer winding voltage to two-thirds of the input voltage; therefore, it is more suitable for applications with an 800V input.

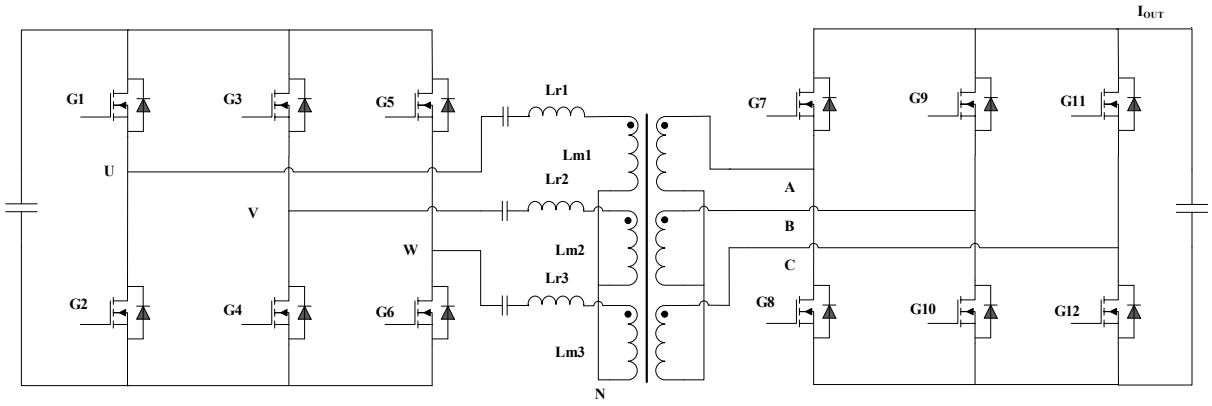

Fig.2. Three phase half bridge LLC with full bridge SSR

B. Operational Principles of the three-phase LLC Converter. The steady-state waveforms are illustrated in Fig.3 for the three-phase LLC resonant converter. The waveforms are based on the conditions below:

(1) Pulse width is 50% and dead time is ignored.

(2) The converter is working at the continuous conduction mode (fs = fr).

(3) The resonant capacitors, resonant inductors and magnetizing inductance are assumed to be the same of each phase.

(4) The phase shift between each phase is 120°.

V_{GS} is the gate-driving signals for the power switches. I_{Lr1}, I_{Lr2}, and I_{Lr3} are the resonant currents. U_{UN}, U_{VN}, and U_{WN} are voltages between the midpoint of each phase and midpoint N of transformer. I_A, I_B, and I_C are phase currents of secondary side. I_{OUT} is the output current of the converter. The waveforms are shown in Fig.3. The detailed descriptions on each working stage are available upon request.

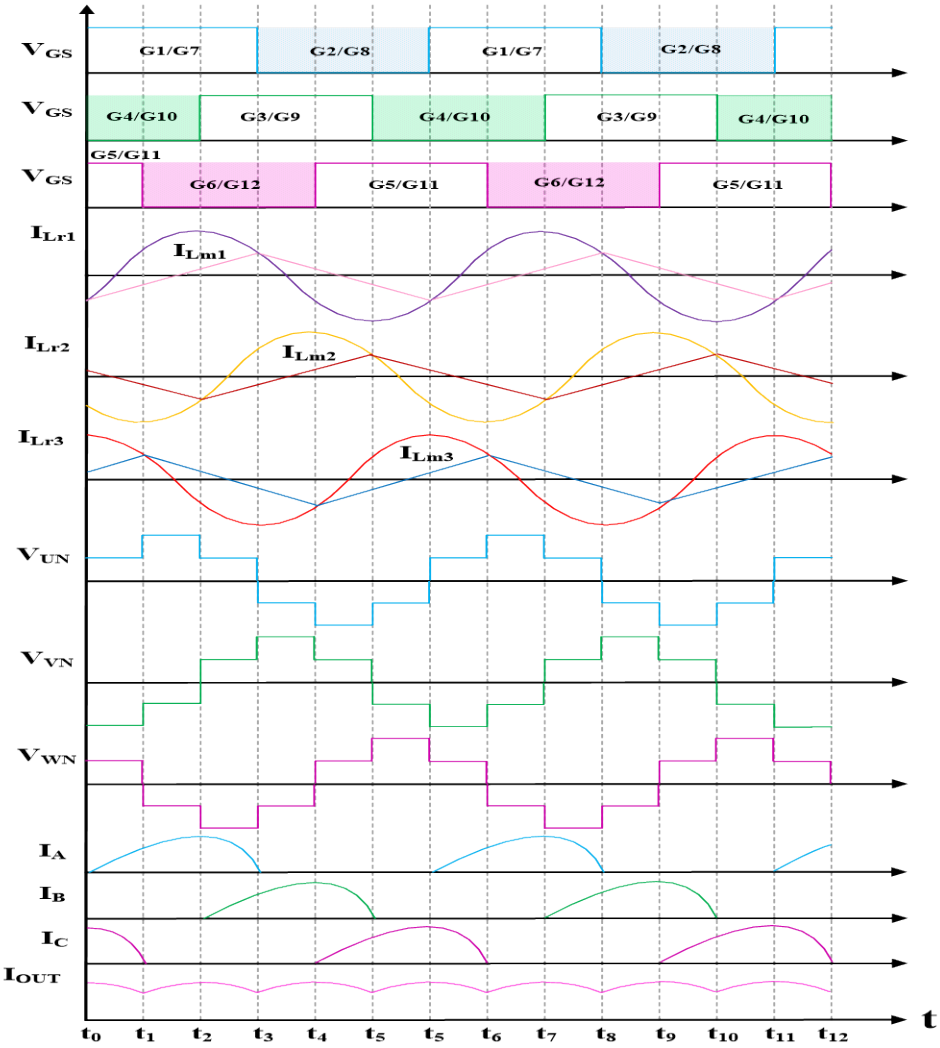

Fig.3 Principal waveforms of three-phase LLC resonant converter

C. Selection of primary MOSFETs

For three phase LLC, the primary side MOSFET voltage stress is equal to Vin which is 800V here. To have enough voltage margin (10% over 800V plus turn-off spikes), 1200V devices are recommended. Of all options, 1200V silicon MOSFET incurs too much switching loss, meanwhile 1200V GaN devices are not widely available and there are not enough commercial use cases. Hence SiC MOSFET is the best candidate for primary MOSFET in three phase LLC application, due to performance and technical maturity.

Primary MOSFET suffers conduction loss and turn off loss in normal operation state. To achieve high efficiency and best thermal performance, the following parameters need to be considered:

(1) Voltage rating - 1200V (with 20% de-rating margin) for voltage spike tolerance.

(2) On-Resistance - 40 mΩ is selected to balance conduction and switching loss.

(3) Output Capacitance (Coss) – Low Coss to easier achieve ZVS.

(4) Reverse Transfer Capacitance (Crss) - Crss is critical due to hard turn off in LLC application. Small Crss allows faster turn-off speed and better efficiency.

(5) Input Capacitance (Ciss) - Smaller Ciss allows faster switching and smaller driving loss.

(6) Package – Top side cooling is recommended for better thermal performance and compact system size.

AOS recommends using GTPAK (TOLT) for the primary switch, which allow thermal dissipation through the top heat sink which reduces thermal resistance significantly. It is a 1200V, 20mohm SiC, the part number is AOGT020V120X2Q and is already released.

AOS is also validating other SiC package options.

D. Selection of SSR Switches

In three-phase LLC SSR application, SSR Switches handle significant current due to large output power. To achieve the best efficiency and thermal performance, the SSR Switches need to have the following features:

(1) Low on-resistance – the resistance comprises of die resistance and package resistance.

(2) Low Qg – low Qg enables low driving loss and allows low dead time.

(3) Low VF – low forward voltage VF minimizes conduction loss during dead time period.

(4) Low Qrr– low Qrr improves body diode reliability and lowers Vds spike during diode reverse recovery.

(5) High UIS capability – During load transient or hot-swap, negative current may incur, combining PCB stray inductance and MOSFET package parasitic inductance, may incur UIS event and cause MOSFET to fail.

AOS solutions for SSR stage are shown in Table I.

Table I. AOS solution for three-phase LLC secondary side

SSR solutions	Solution 1	Solution 2	Solution 4
Part number	AOFG018V10GA1	AOSE018V10GA1	AOPL68801
Package	Standard DFN5*6 Top exposed	FCQFN4x6 Top Exposed	DFN6x5 half bridge FETs 2 in1
Material	GaN	GaN	Silicon
BVdss	100V	100V	80V
Rdson typical Vgs=10V	1.5mΩ at Vgs=5V	1.4 mΩ at Vgs=5V	1.6 mΩ @HS 1.8 mΩ @LS

Here the solution 3 with half-bridge type stacked-die is preferred in this first draft. This solution has two MOSFETs stacking vertically in a half-bridge configuration, hence end customer may parallel less FETs to minimize solution size. Further simulation work is in progress to compare all four options.

Of two GaN options, the solution 2 has lower Rdson and occupies less space comparing to solution 1, but solution 1 has an advantage as the footprint for this GaN device is the same as silicon MOSFETs, that allows more supplier options.

II. Three-level Series Half Bridge (TLSHB) DCX LLC with full bridge SR topology

A. Operational mode

In this topology shown in Fig.4, devices of less voltage rating can be employed on the primary side to allow faster switching. When operating at a fixed switching frequency at the resonant point without frequency modulation, a LLC DCX can achieve maximum efficiency.

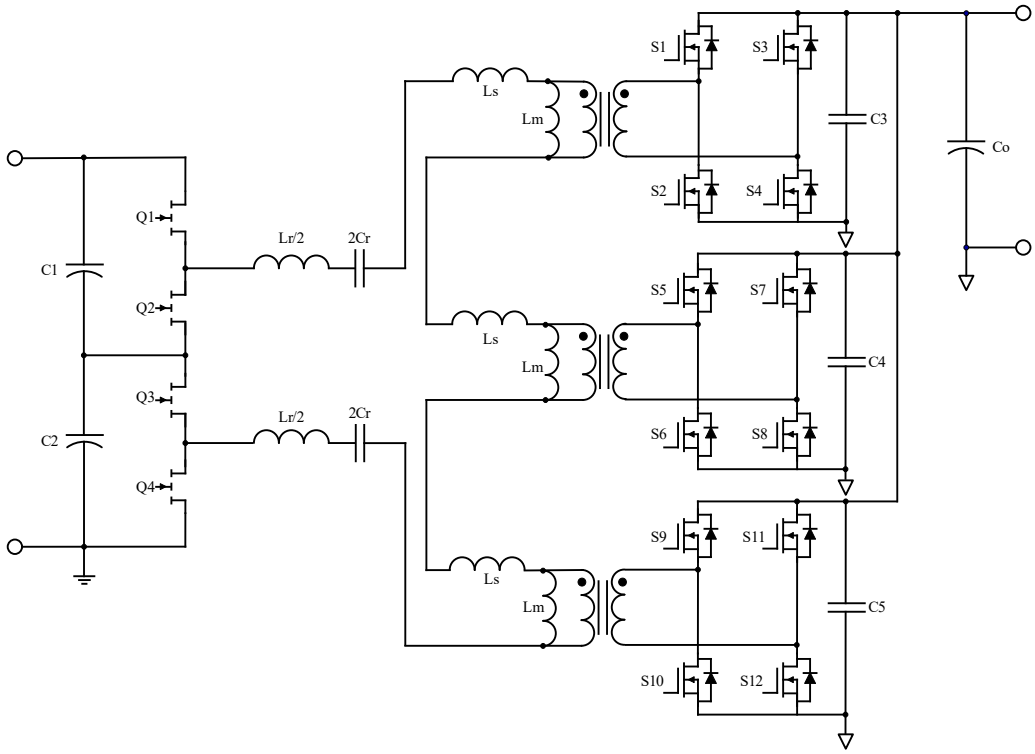

Fig. 4 Three-level LLC with full bridge SR topology

In the three-level LLC full-bridge SR topology, the primary stage operates with two complementary switch pairs (Q1–Q4 and Q2–Q3) driving the resonant tank at approximately 50% duty cycle. The split input capacitors (C1 and C2) each maintain half the input voltage (Vin/2), while the resonant tank voltage remains close to Vin, effectively reducing device voltage stress. Proper voltage balancing between C1 and C2 is essential.

During operation at the resonant frequency, the primary switches achieve zero-voltage switching (ZVS), minimizing switching losses. On the secondary side, the full-bridge synchronous rectifier operates in phase with the resonant current, achieving zero-current switching (ZCS) during turn-off. Fig.5 shows the typical switching waveforms. This soft-switching behavior significantly improves efficiency and reduces EMI.

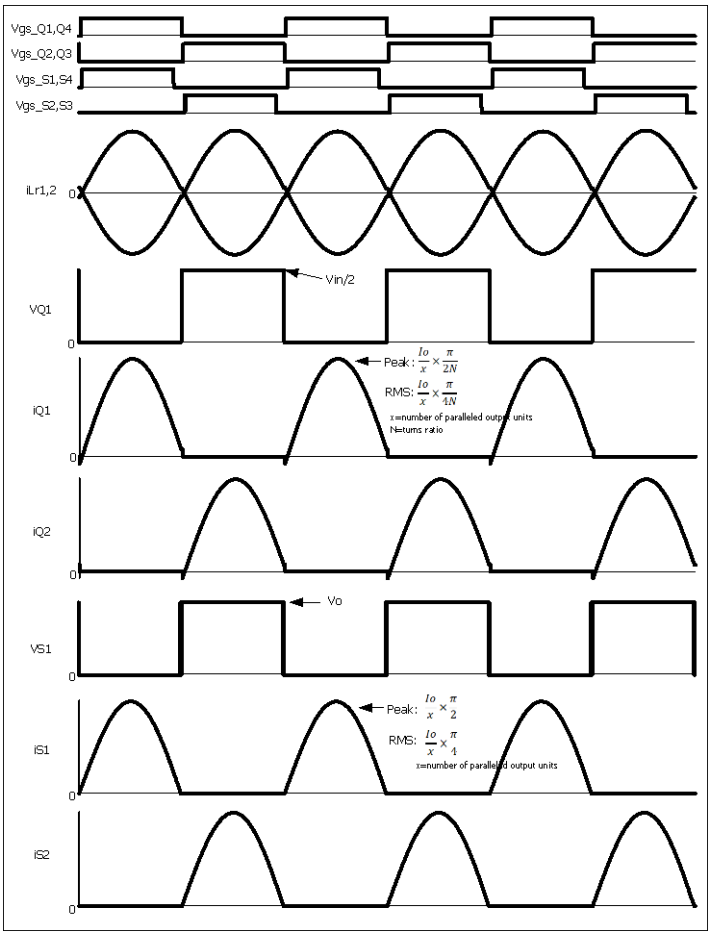

Fig.5 Ideal Circuit Operation of a three-level LLC full-bridge SR converter

B. Primary MOSFET Selection

In a three-level configuration, the primary switch sees only half the voltage stress of a full-bridge LLC stage, so 600V devices can be used. GaN devices offer distinct advantages over conventional Silicon MOSFETs in LLC converters, particularly at high switching frequencies. Their ability to achieve faster transitions with lower switching losses enables the use of smaller magnetic components, resulting in higher power density and overall efficiency.

To maximize efficiency and thermal reliability, the following parameters should be considered:

1) **On-Resistance (RDS(on))** – For GaN, the RDS(on) should be evaluated together with dynamic resistance effects under high-frequency switching.

2) **Gate Charge (Qg)** – Lower Qg reduces gate-drive and switching losses, careful driver selection and optimized layout are critical.

3) **Output Capacitance (Coss)** – Lower Coss eases ZVS operation and minimizes capacitive switching losses.

4) **Reverse Transfer Capacitance (Crss)** – Small Crss supports fast and efficient hard turn-off in LLC applications. GaN devices have negligible reverse recovery charge (Qrr), which can significantly reduce commutation losses compared to Silicon MOSFETs.

5) **Gate Drive & False Turn-On Immunity –** Unlike Silicon MOSFETs, GaN devices have a relatively low VGS(th), making them more susceptible to false turn-on under high dV/dt conditions. Proper driver design, Kelvin source connections, and in some cases negative gate bias are essential for robust operation**.**

6) **Thermal Management & Package Dissipation –** Advanced low-inductance packages with low thermal resistance are essential for GaN devices operating in high-frequency, high-density LLC converters. The package should support the application's power level and enable effective heat dissipation.

Table II offers a comprehensive portfolio of GaN-based primary switch options, combining low RDS(on), negligible Qrr, optimized Coss, and advanced packaging (e.g., TOLL, GTPAK (TOLT), DFN5*6, DFN8*8) to enable high-efficiency, high-density LLC DCX designs. The final choice will made in future work.

Table II. AOS GaN-based primary switch solutions for three-level LLC converters

Three level LLC primary solutions	Solution 1	Solution 2	Solution 3	Solution 4
Package	GTPAK (TOLT)	TOLL	DFN5*6	DFN8*8

Part number	AOGT035V65GA1	AOTL035V65GA1	AONS140V70GA1	AONV070V65GA1
Si/GaN	GaN	GaN	GaN	GaN
BVdss	650V	650V	700V	700V
RDS(on),max @ VGS = 6 V	35mΩ	35mΩ	140mΩ	70mΩ
QG,typ @ VDS = 400 V	14nC	16nC	3.5nC	8.5nC
ID,pulse	127A	127A	32A	60A
QOSS @ VDS = 400 V	155nC	155nC	33nC	94.7nC
Qrr @ VDS = 400 V	0nC	0nC	0nC	0nC

C. Synchronous Rectifier (SR) Device Selection Considerations

In high-input-voltage LLC DCX applications, the secondary-side SR devices in the 48 V stage generally operate under soft-switching conditions. However, during commutation intervals—particularly when operating away from the resonant point, under heavy load, or during reverse conduction transitions— high current slew rates (di/dt) can incur. In these cases, package parasitics and PCB layout directly influences voltage overshoot and ringing. For higher current capability, stacked-die packages improve current sharing, reduce conduction loss, and increase power density in SR implementations.

When selecting SR MOSFETs or GaN devices, the following parameters are critical:

1) **On-Resistance and Thermal Resistance** – Select devices with low RDS(on) in thermally efficient packages (e.g., **DFN, source-down stacked die**), and evaluate RDS(on) at the actual operating temperature.

2) **Output Capacitance (Coss, Qoss) –**Although most Coss-related energy is recycled by the resonant tank under ZCS operation, these parasitics still affect commutation waveforms, ringing, and device voltage stress. Therefore, SR devices with low Qoss and well-behaved Coss are preferred for stable operation.

3) **Package Parasitics** – Low-inductance source leads and Kelvin Source configurations improve ringing suppression and enhance current-sensing accuracy in SR control schemes.

AOS offers a comprehensive portfolio of SR-optimized MOSFETs and GaN devices, refer to Table I, combining low conduction loss, fast switching performance, and advanced package technologies for high-density 48 V secondary designs.

III. TLDNPC three phase LLC DCX resonant Converter

A. Operation mode

The diode-neutral-point-clamped (**DNPC**) topology provides an alternative method of implementing a three-level (**TL**) primary-side circuit in DCX LLC converters. In the DNPC configuration, each leg consists of four switches and two clamping diodes. All primary-side devices have a voltage stress of ½ Vin. As shown in Fig.6, a three-level, three-phase DCX LLC converter can be realized using the DNPC structure. Its operating principle is similar to a two-level three-phase LLC converter. The primary-side switches operate at fixed 50% duty cycle, and 120° phase shift is applied between the PWM signals of the three phases. ZVS can be achieved for all primary-side switches by selecting an appropriate magnetizing current and dead time. The circuit operation waveforms are illustrated in Fig.7.

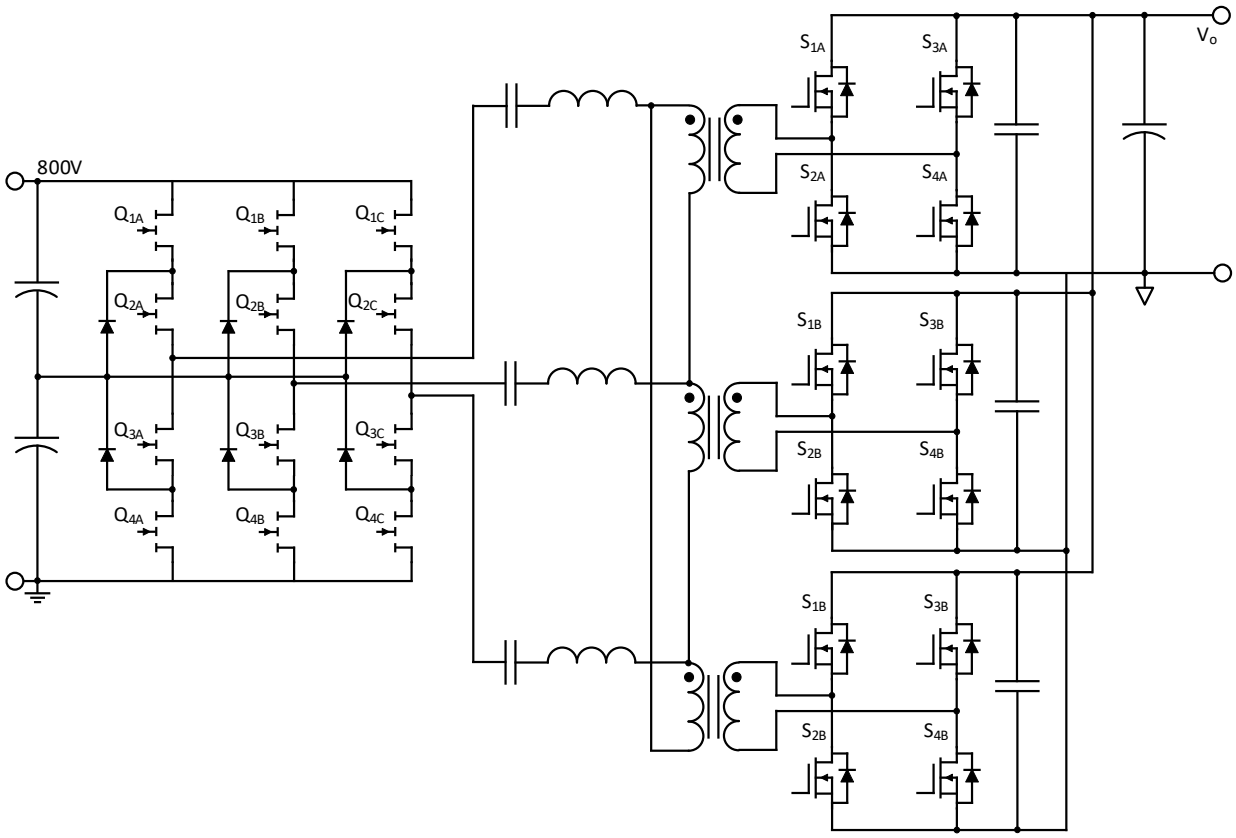

Fig.6 TLDNPC three phase DCX LLC resonant converter

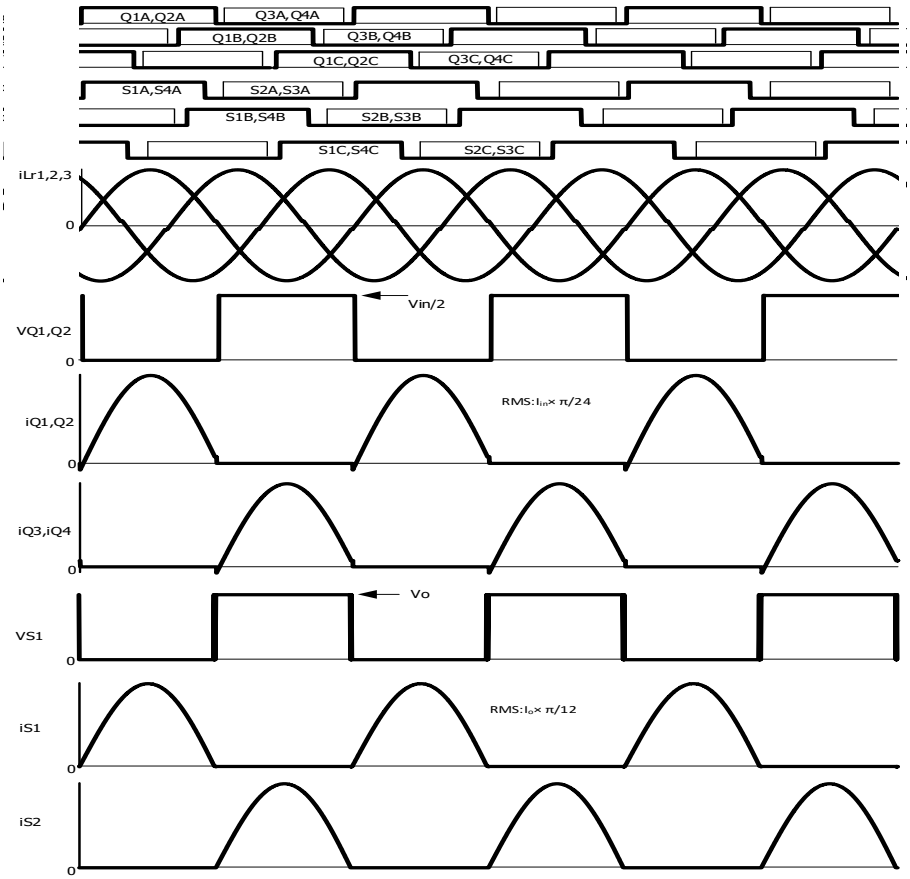

Fig.7 Ideal circuit operation of three-level three-phase DCX LLC converter

B. Selection of primary power device

Due to the three-level nature, the primary switch voltage stress is half of input voltage. Hence, we may refer to the GaN options recommended in Table III.

C. Synchronous Rectifier (SR) Device Selection Considerations

Full bridge synchronous rectifier is used for 50V output, voltage stress of SR power device is clamped by output voltage. So, 80V silicon-based power MOSFET can be used in addition to GaN. The product selection can refer to Table II.

IV. Comparison of different topologies

According to the previous analysis for three different topologies, current &voltage stress comparison is shown in Table III. Further work will decide the optimal operating frequency and number of total devices to parallel for each topology, to fit in the desired space. Meanwhile, the secondary stages are full-bridge based for all three different topologies, their voltage & current stresses are the same, so we may recommend identical devices on the SR side that apply to all three topologies.

Table III. Power device current/voltage stress comparison with different topology

Topology	Three phase half-Bridge LLC	TLSHB LLC	TLDNPC three phase LLC
Primary Device Voltage Stress	V_{in} (800V)	$V_{in}/2$ (400V)	$V_{in}/2$ (400V)
Primary Device Current Stress	π/24×Iin (7.8A)	$\pi/8\times I_{in}$ (23.4A)	$\pi/24\times I_{in}$ (7.8A)
Number of Primary Devices (paralleling may be required)	6	4	12
Secondary Device Voltage Stress	V_o (50V)		
Secondary Device Current Stress	$\pi/12\times I_o$ (63A)		
Number of Secondary Devices	12		

Based on table V, a recommendation table is provided for three different topologies, for AOS first study of 800V PDB design.

On the three-phase half-bridge LLC option, a 1200V, 20 mohm SiC MOSFET in GTPAK (TOLT) package is proposed. Further work is in progress to optimize the frequency choice, thermal management and other details. Other SiC package options are also under validation.

On the Three-level SHB LLC and Three-level DNPC three phase LLC option, two different 650V GaN devices in DFN5*6 and GTPAK (TOLT) are first proposed for comparisons. Further work is in progress to decide the best option, based on compromises across frequency / efficiency / solution size / thermal / EMI results and other

details. For DFN5*6, multiple devices may need to be paralleled. Other GaN products like TOLL and DFN8*8 (the sizes are between DFN5*6 and GTPAK) are also under further comparison studies.

For full bridge rectifier (SSR) configuration, two power devices are listed for further comparison. One is AOS unique silicon-based two-die-in-one-package product AOPL66801 in DFN5*6 package, its benefits in smaller switching loop and lower Rdson are well proven on AOS 12kw PSU SR side in prior design. In addition, by stacking two die vertically, AOS makes the industry-wide lowest Rdson MOSFET with only 0.65mohm in a DFN5*6 package. The other one is a 100V GaN for further comparison study.

Of all devices listed in Table IV, they are either released to the market already, or the engineering samples are available and release will be soon.

Table IV. Power device recommendations for 12kW 800V-48V DCX LLC converters

Primary power device

Topology	Three phase half-Bridge LLC	Three-level SHB LLC		Three-level DNPC three phase LLC	
Primary device part number	AOGT020V120X2Q	AONS140V70GA1	AOGT035V65GA1	AONS140V70GA1	AOGT035V65GA1
Package	GTPAK (TOLT)	DFN 5x6	GTPAK (TOLT)	DFN 5x6	GTPAK (TOLT)
Material	SiC	GaN	GaN	GaN	GaN
BVdss	1200V	650V	650V	650V	650V
Rdson_typ	20mΩ	140mΩ	35mΩ	140mΩ	35mΩ

SSR power device

Secondary device part number	AOPL68801	AOSE018V10GA1
Package	DFN 6x5 half-bridge device	FCQFN4x6 Top Exposed
Material	Si	GaN
BVdss	80V	100V
Rdson_typ	1.6mΩ +1.8mΩ (two-in-one)	1.4 mΩ

Summary

This whitepaper compared three different topologies; the three phase half bridge LLC, the TLSHB LLC, and the TLDNPC three phase LLC. Due to the high-power-density requirement on HV PDB, it is critical to save power device area both on the primary and secondary sides. AOS has recommended suitable devices for each topology for further comparison studies. For Topology I-three phase half bridge, AOS offers 1200V SiC and multiple SR options. For topologies II and III, on the primary side, 650V GaN is chosen but various package options are to be further explored. On the secondary side, both GaN and stacked-die MOSFET options are introduced and will be compared.

Future work

AOS will conduct further studies on the optimized frequency of each topology to in order to fit the proposed solutions into the PDB size limit. AOS will also present trade-offs in efficiency / thermal / EMI and other details that must be considered in a complete design. AOS will also design the magnetic component and entire PDB system, based on the final topology choice and device selection.