Application of Power MOSFETs in Battery Management Charge-Discharge Systems

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Introduction

Power MOSFETs are required to be connected in series between the lithium-ion battery pack and the output load. At the same time, a dedicated IC is used to control the on and off of the MOSFET for managing the charge and discharge of the battery, as shown in Figure 1. In consumer electronic systems such as cell phones, laptops, etc., the complete circuit system with control IC, power MOSFET, and other electronic components is called the Protection Circuit Module (PCM).

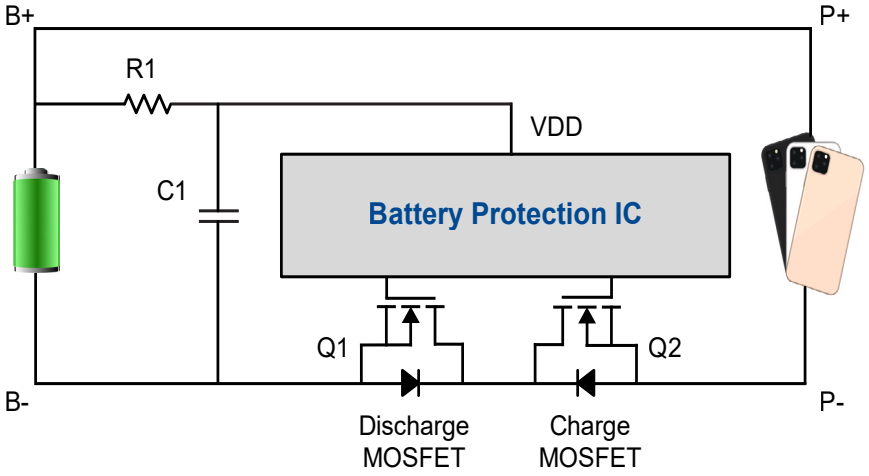


Figure 1. Battery Protection Board Circuit Diagram

In the PCM, one power MOSFET is used for charging and another for discharging. These Power MOSFETs are connected in series, back-to-back, in one of two configurations. The first configuration is when the two power MOSFET drains are connected together. In the second configuration, the two power MOSFET sources are tied together.

Similarly, there are two ways to place the power MOSFET in series with the battery. One is to it on the negative end of the battery, called the “ground end” or low-side; the other one is to place it at the positive end of the battery, called the high-side. The two different power MOSFET back-to-back connection modes and their different placements each have their own unique advantages and disadvantages, corresponding to different system requirements.

Given that PCMs require a low on-resistance MOSFET, engineers usually use N-channel power MOSFETs instead. Some applications utilize P-channel MOSFETs on the positive end due to their simplicity and driving flexibility. However, P-channel MOSFETs exhibit a higher on-resistance than N-channel solutions, and their selection is comparatively limited.

In today’s technological landscape, advances in smartphone, tablet PC, and mobile device technology has led to an increased demand for improved functionality and performance. For example, Figure 2 illustrates the trend in battery charging current for smartphones. To meet these demands, die package designers must prioritize a thin, low resistance, compact, and lightweight structure or incorporate high voltage capabilities for rapid charging applications.

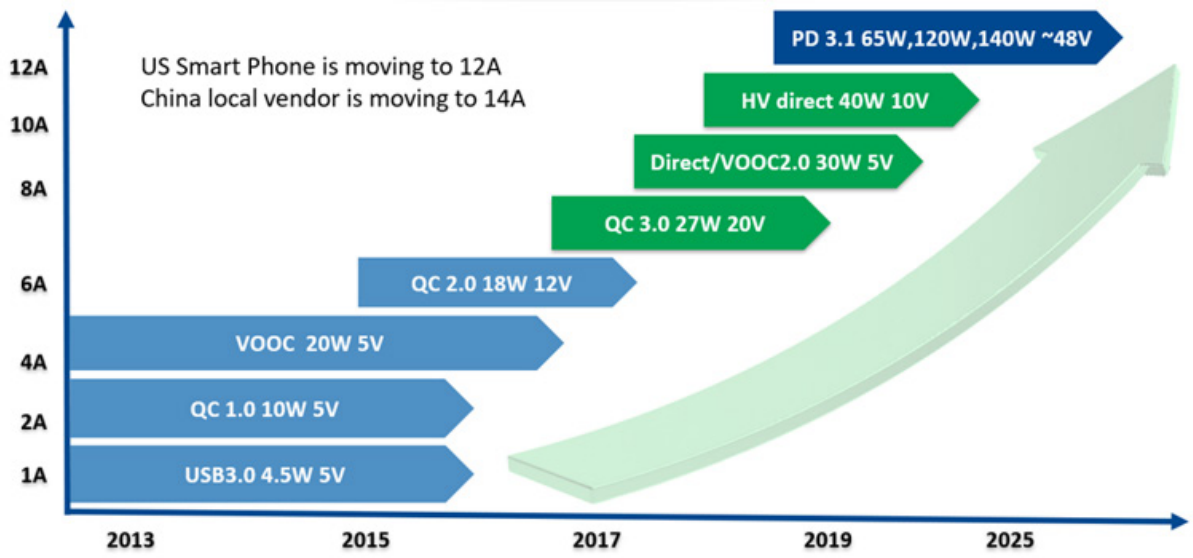


Figure 2. Battery Charging Current Trend

Engineers design lithium-ion battery management systems (BMS) to monitor voltage, current, and temperature as well also to assess the state of charge and overall health of the battery. Precise control of cell voltage is essential for guaranteeing safe operation, fulfilling safety standards, and prolonging battery life. In consumer electronics such as smartphones, tablets, and ultra-thin notebooks, the PCM is attached to the battery pack to oversee the its charging and discharging processes. The PCM is composed of various elements, including a battery-protection integrated circuit (IC), power MOSFETs, and additional electronic components.

To cater to specific customer requirements, AOS has introduced ultra-thin MOSFET technology and a molded type of MOSFET (MRigidCSP™), designed specifically for lithium-ion battery protection needs. The molded MOSFT design delivers superior electronic performance, such as low on-resistance (Rss(on)), and features a robust mechanical structure that improves bending strength and minimizes warpage during reflow processes. AOS is committed to the ongoing development of ultra-thin backside grinding processes and wafer-level molding to support customer applications with a thinner and more durable package design, aimed at providing more efficient and powerful battery management solutions.

AOS' MRigidCSP technology is meant for battery management applications, particularly emphasizing ultra-low Rss to facilitate fast charging capabilities. This innovative technology significantly reduces on-resistance while improving mechanical strength. One of the key features of MRigidCSP is its ability to reduce on-resistance in battery management circuits. As a lower on-resistance means less power loss, MRigidCSP also unlocks new levels of fast charging performance. It also features a common-drain configuration design which translates into space savings for the slim PCBs normally found in portable electronic devices.

In this article, we discuss the primary benefits of an additional molding layer for enhancing warpage control and mechanical strength.

One prevalent design approach to mitigate warpage in a chip involves increasing the silicon thickness. However, this may also lead to an increase in the series resistance (Rss) at certain points. AOS has introduced a "molded-die" configuration, wherein a mold layer is directly affixed to the chip backside surface. This effectively modifies the chip's coefficient of thermal expansion (CTE) to align more closely with that of the substrate, thereby reducing warpage induced by temperature variations during surface mount technology (SMT) processes. Further optimization can be achieved by meticulously regulating the molding thickness in accordance with the specific materials of the chip and substrate. Package structure considerations for minimizing warpage include the molding layer design, process management, and material selection.

- A molding layer that is directly bonded to the chip backside surface allows for precise adjustments to the effective CTE through thickness modification.
- A thicker molding layer can effectively counterbalance warpage arising from the silicon and metal layers.
- Selecting a mold material with a CTE that closely matches that of the chip and backside metal is preferred.
- Ensuring strict tolerances during manufacturing can help reduce variations in chip thickness and the molding process, thereby alleviating internal stresses generated during production.
- Employing an appropriate underfill material to fill the gaps between the chip and substrate can further diminish stress and warpage.
- Increasing the chip's thickness can inherently enhance its resistance to bending, while integrating internal reinforcement structures within the chip can provide additional mechanical stability.

Figure 3 provides a schematic representation of the typical vertical structure for MRigidCSP, which includes typical values of 1.35 mils of silicon, 30 micrometers of backside metal, and 235 micrometers of molding compound. The choice of 1.35 mils of silicon is preferred due to its lower Rdson. Figure 4 illustrates the standard vertical structure of an AlphaDFN™. The silicon thickness is set at a value to achieve Rdson in accordance with customer requirements. The AlphaDFN features a different silicon thickness design, with the standard being 2.5 mils, in contrast to the thinner 1.35 mils used in MRigidCSP. When thickness is reduced from 2.5 mils (as in AlphaDFN) to 1.35 mils (as in MRigidCSP), RSS is improved by 20%.

Vertical Structure - MRigidCSP™

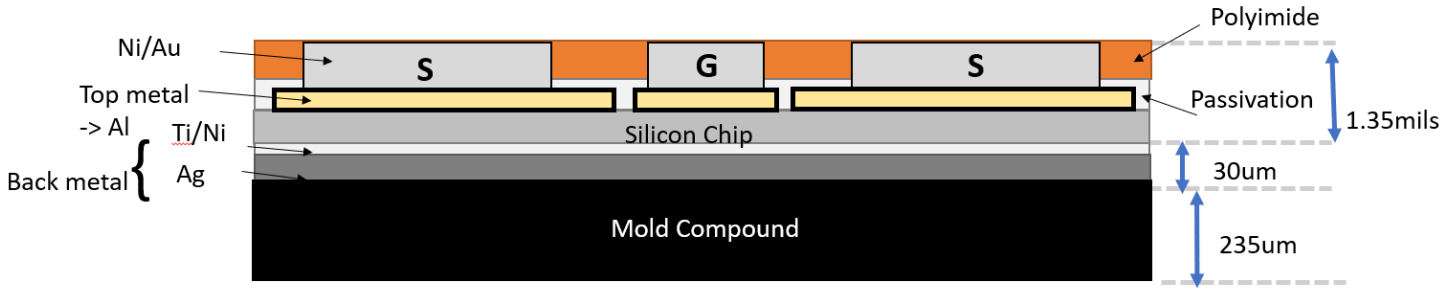


Figure 3. Example of Vertical Structure for AOS MRigidCSP™

Vertical Structure - AlphaDFN™ (2.5mils Si)

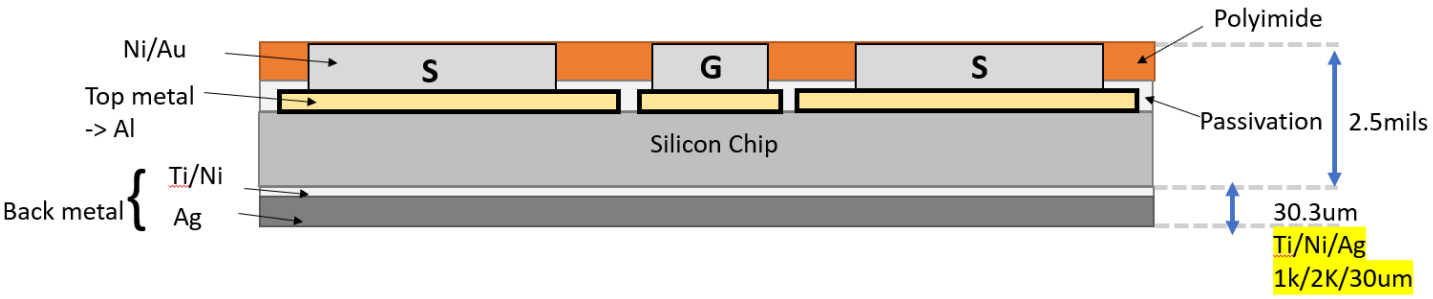


Figure 4. Example of Vertical Structure for AOS AlphaDFN™ 2.5mils

Modern MOSFET components demand ultra-low electrical resistance, but traditional WLCSPs can introduce significant resistance, particularly when employing back-to-back MOSFETs. Although reducing substrate thickness can lower resistance, it may compromise mechanical strength and lead to potential issues during PCB assembly reflow processes, such as warpage or handling difficulties, which can be addressed by incorporating a molding layer. Ultimately, the main factors that influence warpage and mechanical strength include material thickness and structural design. AOS MRigidCSP (molded WLCSP) offers an optimal solution to balance mechanical strength and warpage.

Power MOSFET Connected Back-to-Back

The Working Principle

The two N-channel power MOSFETs used to manage the charge and discharge are placed at the ground end, and their drains are connected back-to-back, which is a common scheme for PCMs (Figure 5). In this configuration

- Q1 is the power MOSFET for battery discharge
- Q2 is the power MOSFET for battery charge
- B+ is the positive end of the battery
- B- is the negative end of the battery
- P+ is the positive end of the battery pack
- P- is the negative end of the battery pack
- VSS is the ground of the battery protection management IC,
- The negative end of the battery, VSS, and the source of Q1 are connected together.

Before the PCM board is operational, Q1, Q2 are both off.

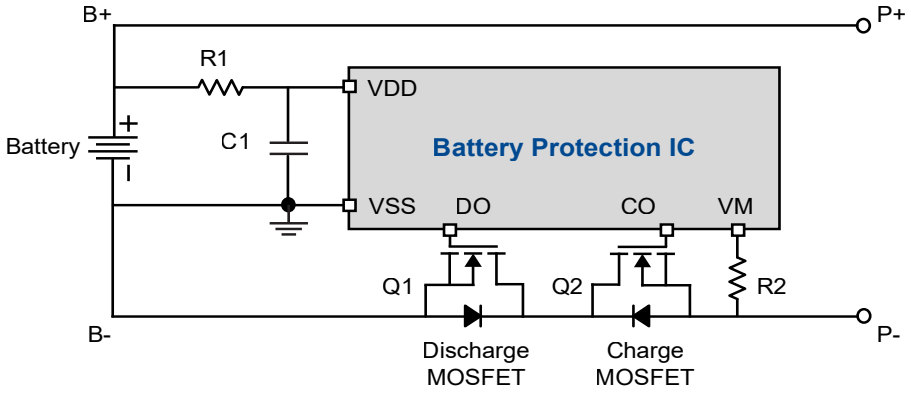


Figure 5. Power MOSFET Ground End and Drain Back-to-Back Circuit Diagram

Charging

When charging, the control IC gate provides the driving signal CO to the charging power MOSFET(Q2), and the driving signal path of Q2 gate is: the positive end of the external charging circuit→P+→B+→R1→VDD→CO→Q2 Source→P-→the negative end of the external charging circuit. A complete driving loop is shown in Figure 6.

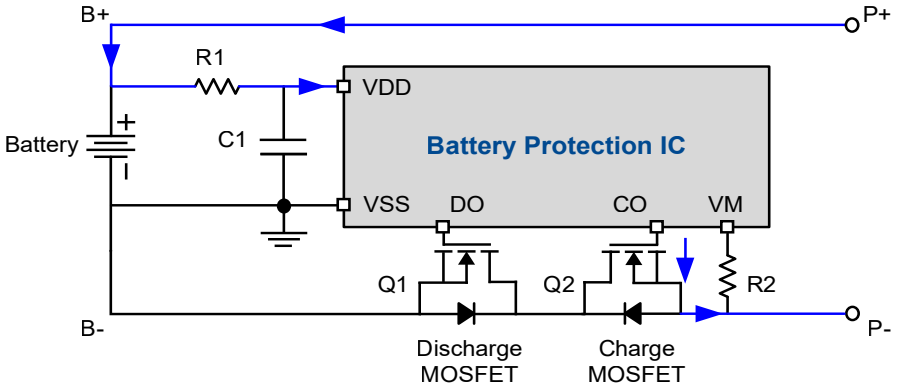


Figure 6. Charging, the Driving Signal Loop of Q2 Gate

When Q2 is on, the charging current path is: P+→B+→B-→Q1 internal parasitic diode→Q2 channel→P-. The battery can then be charged as shown in Figure 7.

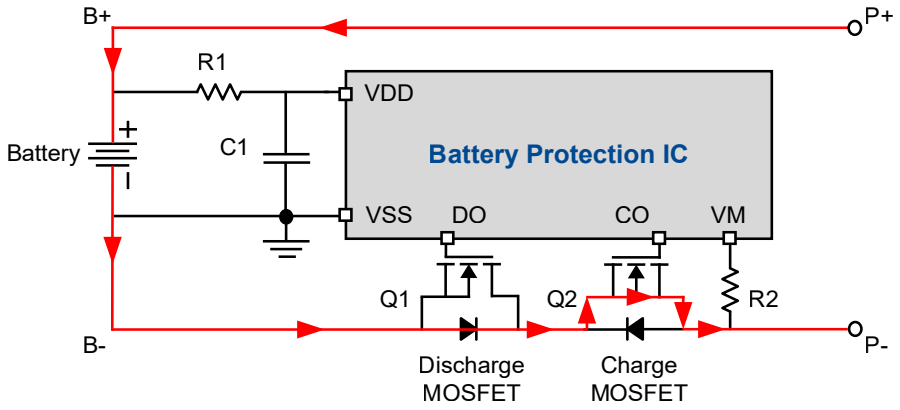


Figure 7. Charging Loop when Q2 is On

In order to reduce the loss of Q1 when Q2 is turned on, the DO pin of the control IC is pulled high to make the discharge power MOSFET Q1 turn on. Due to the low $R_{DS(ON)}$ of Q1, its conduction loss is far lower than that of the parasitic diode, and the efficiency of charging can be improved. The current driving path of Q1 is: VDD→DO→Q1 gate→Q1 Source→B- →VSS, as shown in Figure 8.

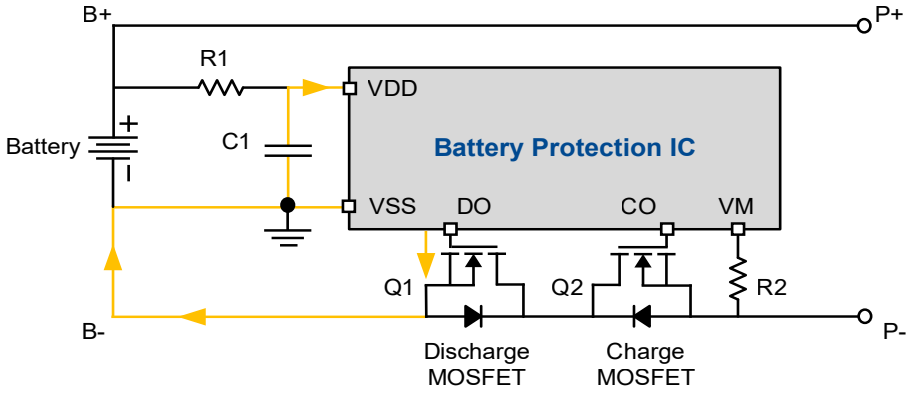


Figure 8. During the Charging, Q1 Drive Signal Loop Output by DO when Q2 is On

When Q2 and Q1 are in the on-state at the same time, the charging current path is: P+→B+→B-→Q1 channel→Q2 channel→P-, as shown in Figure 9.

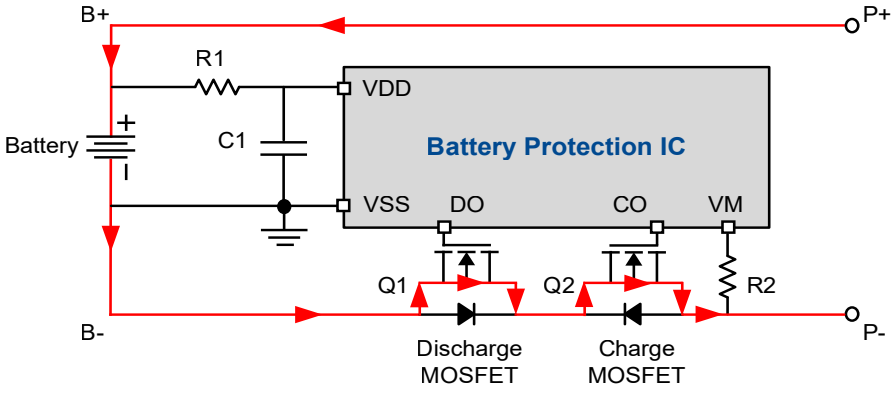


Figure 9. Charging Loop when Q2 and Q1 are On

Discharging

When discharging, the control IC provides the gate drive signal DO to the discharging power MOSFET(Q1), and the gate drive signal path of Q1 is: VDD→DO (Output of driver)→Q1 gate→Q1 Source→B- →VSS, as shown in Figure 10.

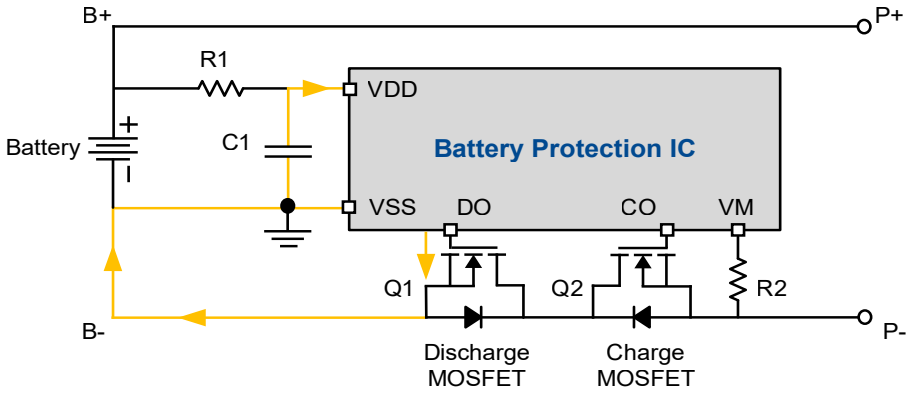


Figure 10. Discharge, Driving Signal Loop of Q1 Output by DO

When Q1 is on, the current path of discharge is: P-→Q2 internal parasitic diode→Q1 channel→B-→B+→P+. The battery can then be discharged, as shown in Figure 11.

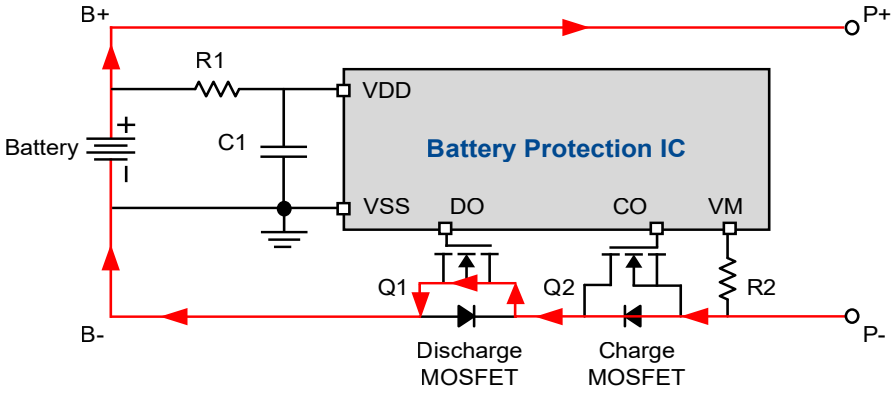


Figure 11. Discharge Loop when Q1 is On

In order to reduce the loss of Q2, when Q1 turns on, the control IC provides the gate drive signal CO to the charging power MOSFET Q2 so that Q2 is turned on. Due to the low conduction resistance of Q2, the conduction loss is far lower than that of the parasitic diode so as to improve the battery service time. The path of Q2 driving current is: VDD→CO→Q2 Gate→Q2 Source→Q2 internal parasitic diode→Q1 channel→B-→VSS, as shown in Figure 12.

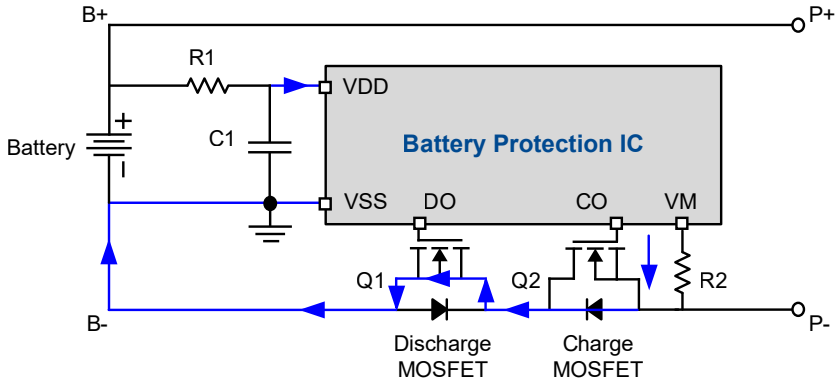


Figure 12. Discharge, Driving Signal Loop of Q2 Output by CO

Q1 and Q2 are in the on-state at the same time, and the path of the discharge current is: P-→Q2 channel→ Q1 channel→B-→B+→P+, as shown in Figure 13.

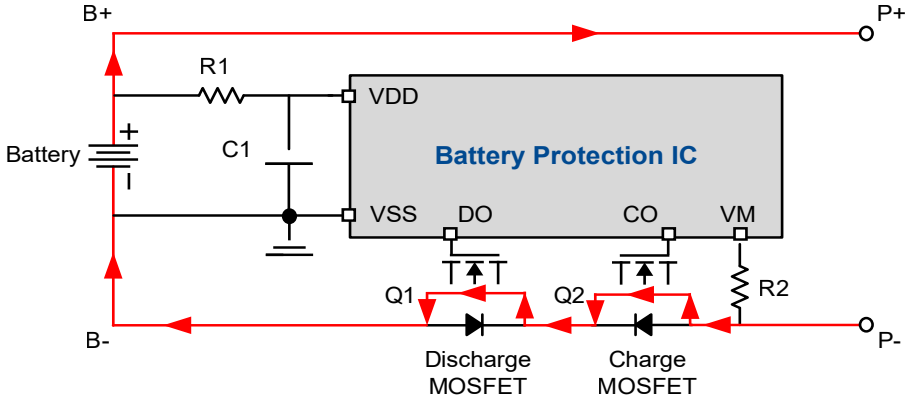


Figure 13. Discharge Loop on Q1 and Q2

Ground End, Source Back-to-Back

The two N-channel power MOSFET sources are connected back-to-back and placed on the ground, as shown in Figure 14. This structure is rarely used in PCM, but is sometimes used in load switches and hot-swap circuits for communication systems.

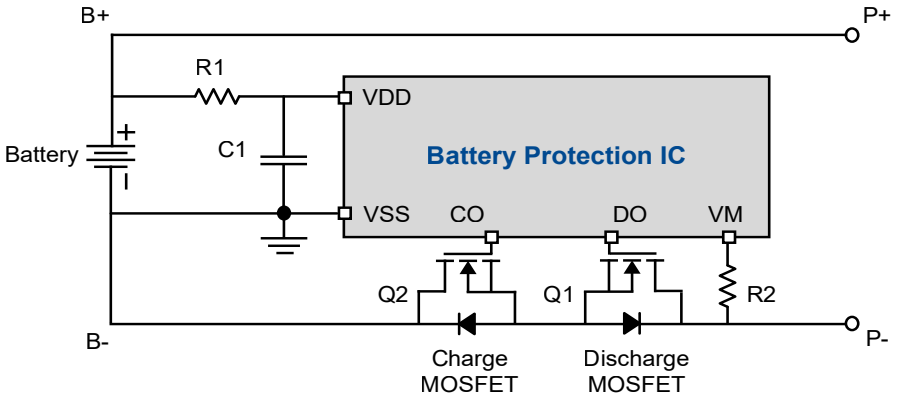


Figure 14. The Source of Power MOSFET are Connected Back-to-Back

Positive End, Drain Back-to-Back

A common PCM scheme is charging and discharging two N-channel power MOSFETs at the power supply end (high-side) with drains connected back-to-back (Figure 15). Q1 is the power MOSFET for battery discharge, and Q2 is the power MOSFET for battery charge.

The two N-channel power MOSFETs are placed at the positive end. As a result, two charge pumps are needed to enable a floating drive.

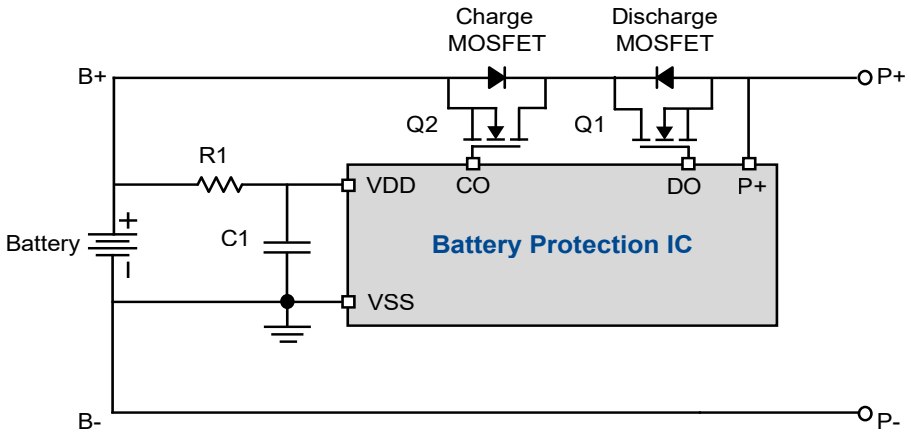


Figure 15. Power MOSFET at High-End, with Drain Connected Back-to-Back

Positive End, Source Back-to-Back

Charging and discharging two N-channel power MOSFETs placed at the power supply end (high-side) with their sources connected back-to-back is shown in Figure 16. The two N-channel power MOSFETs are the common source, so a charging pump is required for driving. This structure is also used in load switches.

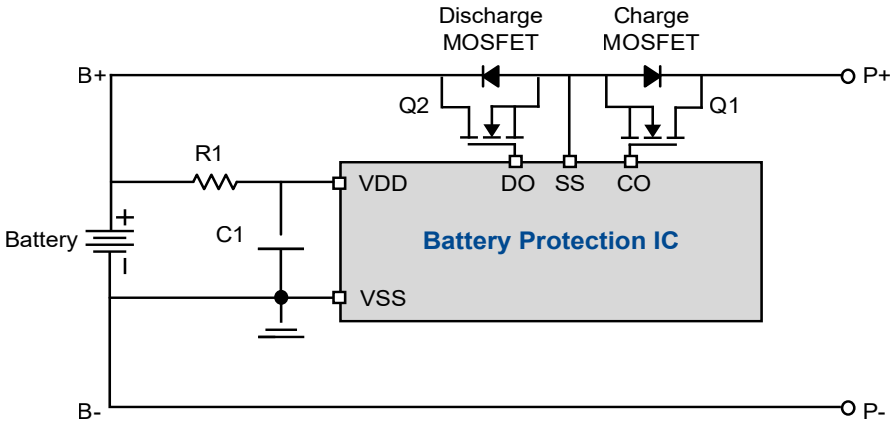


Figure 16. Power MOSFET at High End, with a Source Connected Back-to-Back

Multiple MOSFETs in Parallel with Large Current

At present, in order to improve the service time and standby time of the electronic system, battery capacities are increasing to 5000mAh, or even larger. As such, engineers have begun adopting fast charging to shorten the charging time. In fast charging, the battery receives a larger charging current, such as 4A, 5A, 6A, or even as large as 8A. At these currents, the PCM's internal MOSFETs consume significant power and experience elevated temperatures. In order to reduce the temperature rise and ensure the reliable operation of the power MOSFET, two or more MOSFETs can be used in parallel, as shown in Figure.17.

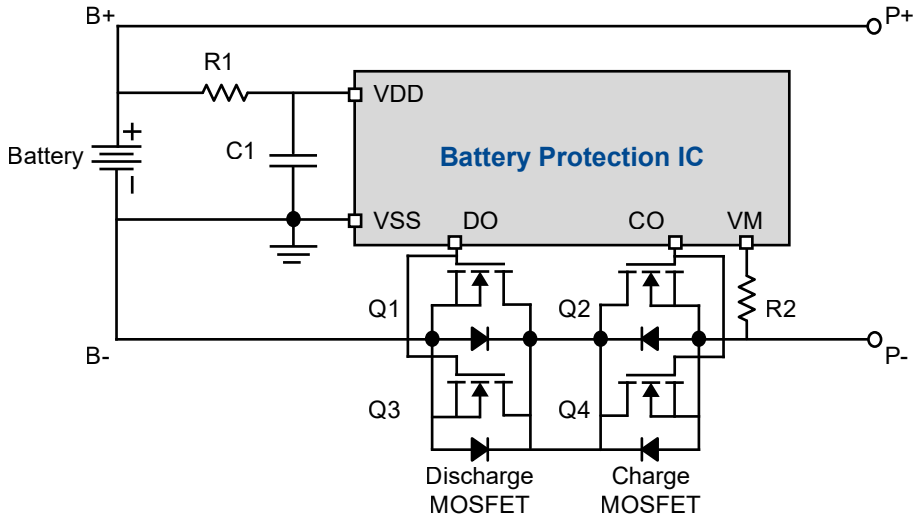


Figure 17. Multiple MOSFETs in Parallel with Large Current

Redundant Design

According to the requirements of the LPS safety regulations, if the power MOSFET inside the PCM is damaged or short when plugged into the charger, the input voltage is applied directly to the battery, which can be dangerous. In order to improve the safety of the system, another set of back-to-back power MOSFET can be connected in series, or other schemes can be used to form redundant design. When the primary protection fails, there is another protection, as shown in Figures 18 to 21.

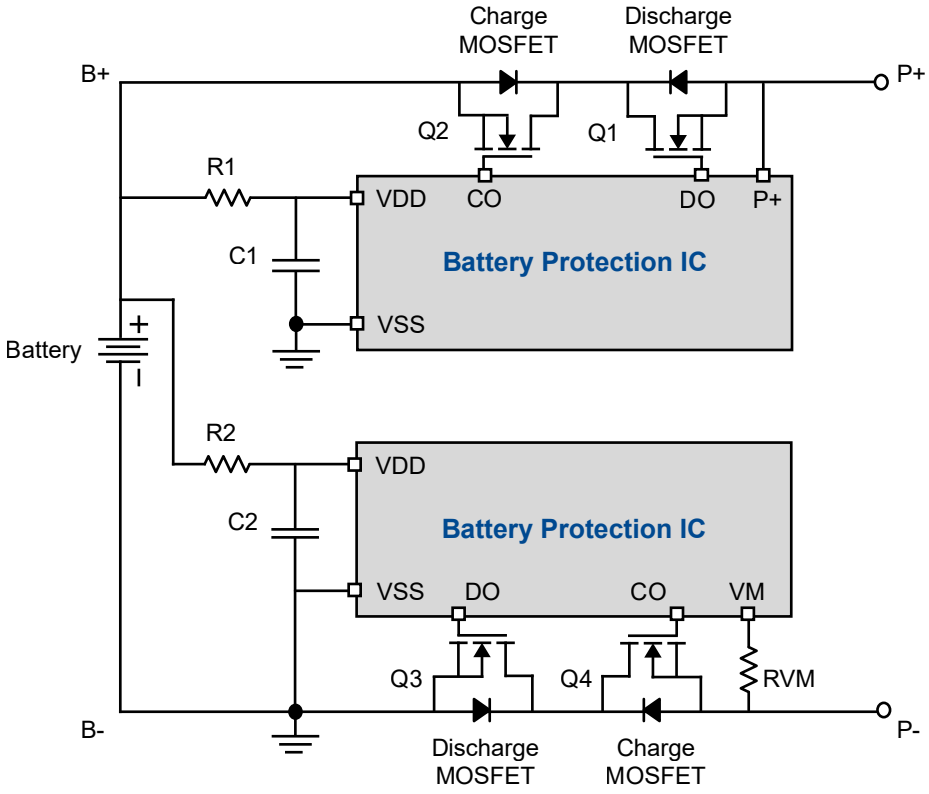


Figure 18. Two Sets of Power MOSFET, One at the High-End and the Other at the Low-End

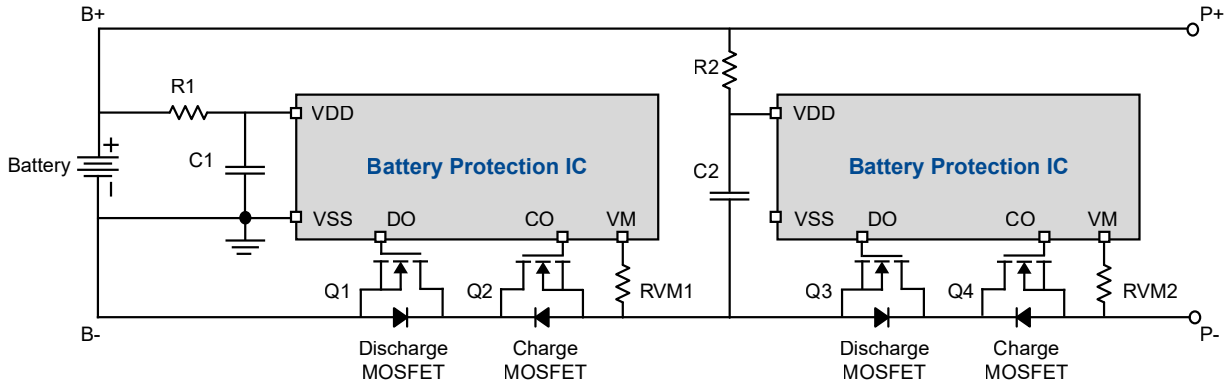


Figure 19. Two Sets of Power MOSFETs at the Low-End

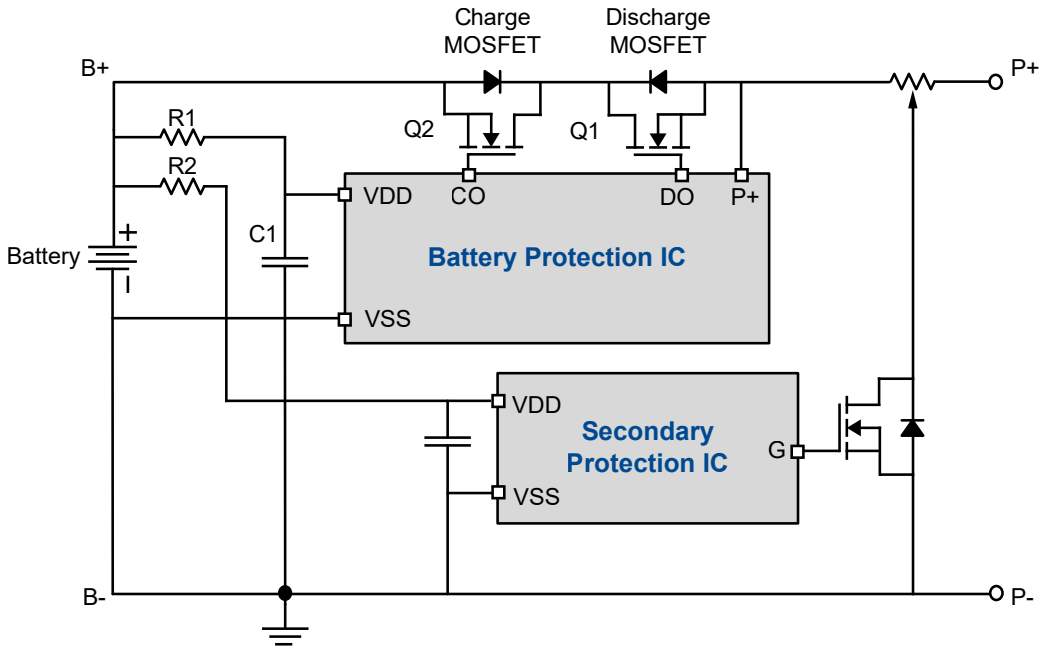


Figure 20. Power MOSFET Placed at the High-End with Electronic Fuse

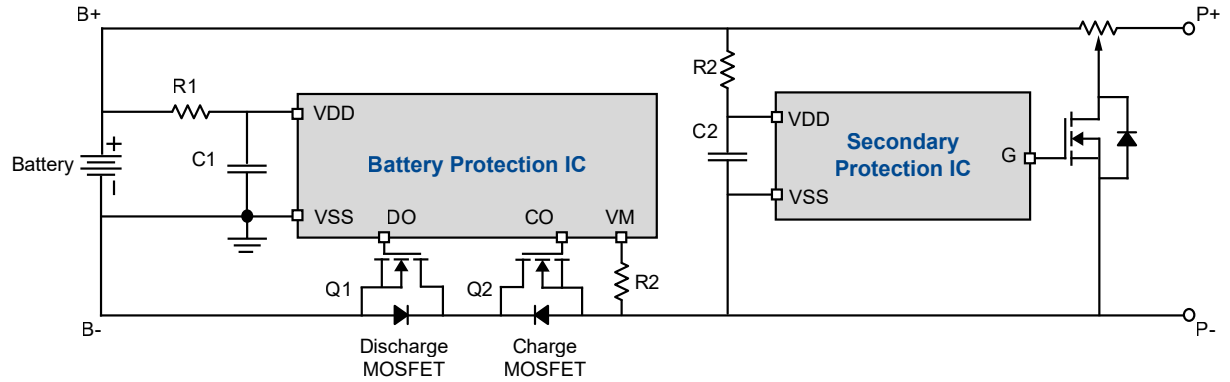


Figure 21. Power MOSFET Placed at the Low-End with Electronic Fuse

Performance Requirements of Power MOSFET

The larger charging currents used in fast charging introduces stringent technical requirements for the battery pack's power MOSFETs as well as for the large-capacity lithium-ion batteries, both on the production line and in the field. All of these factors pose technical design challenges for managing the battery's charge and discharge cycles.

High Power Density, Low Power Consumption, Good Heat Dissipation

The primary requirement for designing a large-capacity lithium-ion battery pack is to maximize the battery's capacity within a specified volume and weight, thereby achieving higher power density. Therefore, the charge and discharge management circuit PCM, including the above power MOSFET, is also required to be smaller. Meanwhile, due to the large current during fast charging, the power MOSFET on the PCM needs a minimal on-resistance $R_{DS(ON)}$ under size limitations, such as 1.2 mm * 1.2 mm. In theory, a smaller $R_{DS(ON)}$ requires a larger chip size. Therefore, the design can be optimized in two ways

(1) Wafer Technology

Achieving lower on-resistance requires improvements in MOSFET cell density. Other techniques, such as thick metal and thin wafers, can reduce resistance. N-channel power MOSFETs can also achieve lower on-resistance RDS(ON) in a reduced form factor.

(2) Packaging Technique

Power MOSFET packages usually use leads. To further reduce PCM on-resistance, designers can completely remove the package wire resistance by switching to chip-level CSP packaging technology. CSP also has better thermal conductivity, thus reducing the temperature rise of the power MOSFET, which helps to improve its reliability.

MOSFETs using CSP packaging technology without the external plastic shell or other material protections will be affected by various thermal stress and mechanical stress in the PCM production process which could crack the die. Therefore, techniques such as surface coating the chips can be employed to resist mechanical and thermal stress.

Short Circuit Capability

Large-capacity lithium-ion battery in the field can experience extremely large current draw, especially under extreme conditions. When protection ICs detect over-current conditions, they will delay the system. During the delay, the MOSFET will be under very large current load, which requires robust construction to withstand. This is one reason why all lithium-ion batteries must undergo short circuit tests.

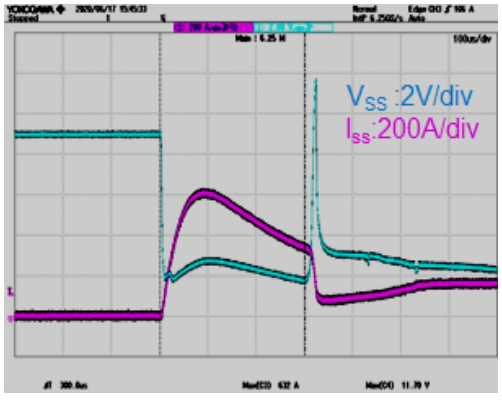


Figure 22. Pass of the Short Test

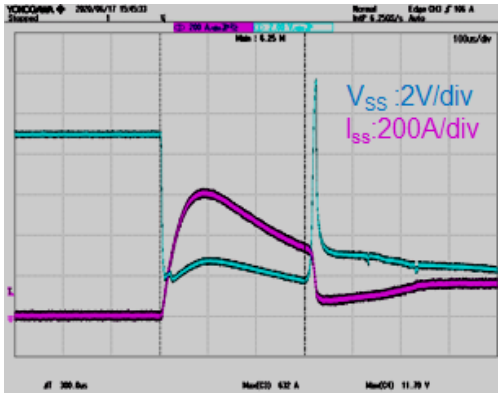


Figure 23. Fail of the Short Test

In theory, the larger the chip size, the stronger the robustness for short circuit current. However, with the trend of smaller form factors, there will be a limit to the capability. Thus, the application circuit design must consider the requirements necessary to ensure a robust design that can resist the impact of a large short-circuit.

Avalanche Robustness

The MOSFET Avalanche capability is important when the output end of the battery pack is a short circuit, and the switch is off. The selection of the power MOSFET should include a sufficient avalanche capability determined by the application conditions.

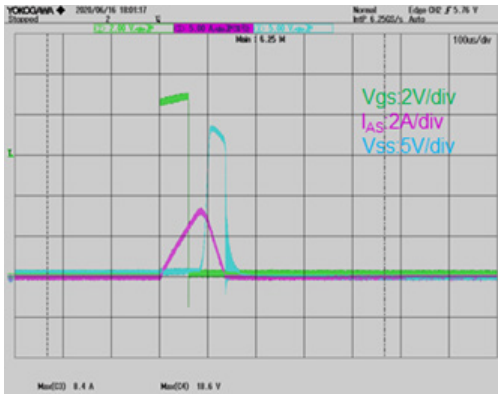


Figure 24. Pass of the Avalanche Test

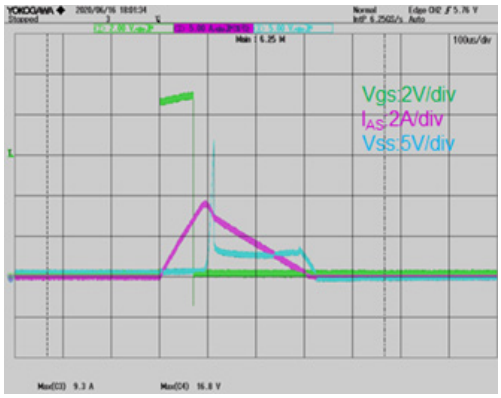


Figure 25. Fail of the Avalanche Test

dv/dt Protection

During a reverse connection test, the maximum per-cell operation voltage is 4.4V, while the maximum charge voltage is 4.4V. In the production process of large-capacity lithium-ion batteries, the external DC power supply will directly touch the two output ends of the battery pack during the test. For this reason, the MOSFET will experience 8.8V of high dv/dt stress.

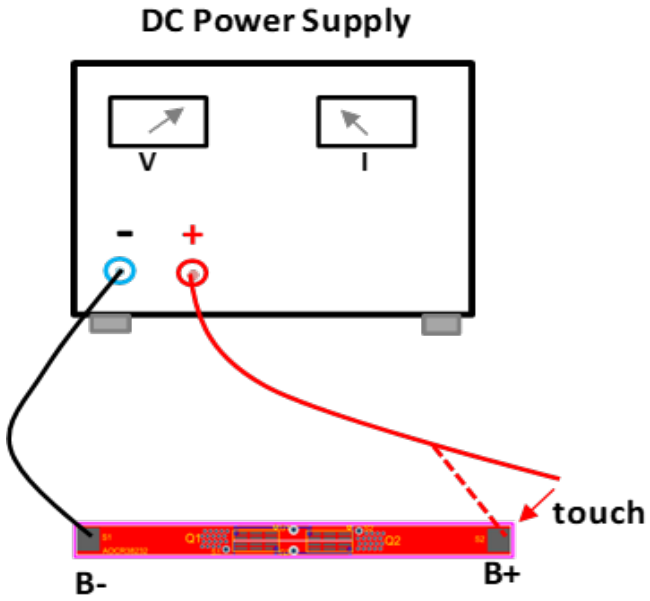


Figure 26. Touch Test Diagram

If the MOSFET experiences a high dv/dt across the drain to source, the parasitic capacitance CDS will have a charging current of I = CDS * dv/dt. If the current is large enough, it will trigger the parasitic npn bipolar to turn-on and the MOSFET can be easily damaged.

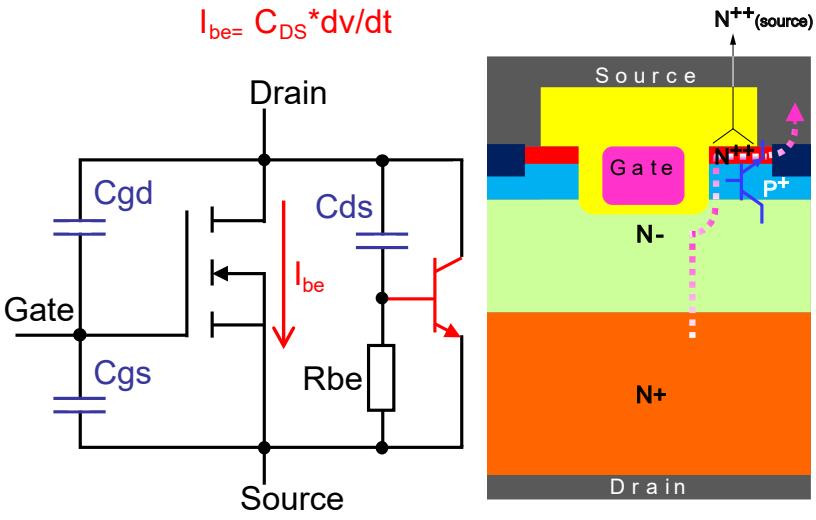


Figure 27. High dv/dt Bipolar Turn On Diagram

To avoid damage to the circuit, the higher the voltage directly touched, the most robust the battery pack should be. Figure 28 shows the actual measurement of MOSFET tolerance to dv/dt. Usually, the large dynamic dv/dt will also be generated in the process of the battery pack output short and protection shutdown. The excessively high dv/dt will cause dynamic avalanche damage to the power MOSFET. Therefore, it is necessary to optimize the power MOSFET's structure to ensure that it has sufficient immunity against high direct touch voltage and high dv/dt..

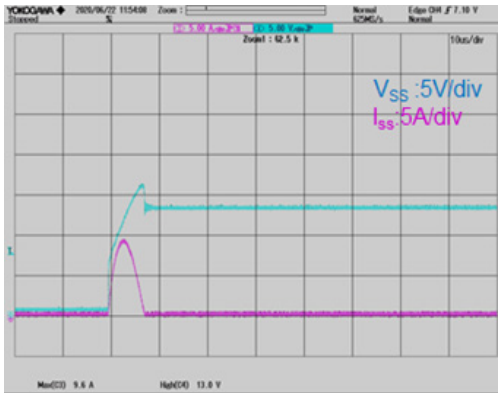


Figure 28. Pass of the 13 V Direct Touch Voltage Test

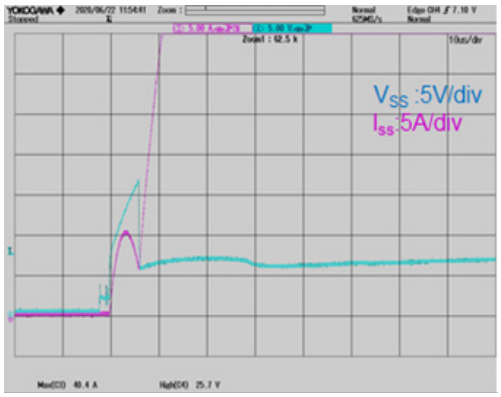


Figure 29. Fail of the 14V Direct Touch Voltage Test

The below test result shows that competitor-B does not meet the minimum requirement of the reverse connection test: 8.8V direct touch test. AOCA33104E passes the 17V direct touch test and it shows stronger robustness in high dv/dt stress.

Table 1. Direct Touch Voltage Test Results

Part Number	Direct Touch Pass Voltage (V)
AOCA33104E_1#	17
AOCA33104E_2#	18
AOCA33104E_3#	17
CompetitorA_1	14
CompetitorA_2	14
CompetitorA_3	14
CompetitorB_1	7
CompetitorB_2	7
CompetitorB_3	7

Key Points of PCB and Thermal Design

The temperature of the MOSFET usually does not exceed 65°C in normal environment temperature. The PCM control board is generally assembled together with the battery, and the PCB size is a constraint and typically high thermal resistance. Thus, special considerations may be needed on the thermal design for the system.

For example, the charging voltage of the single-cell phone quick charger of 47W is 5V, and the maximum charging current is 9.4A. The typical $R_{DS(ON)}$ of AOCR38232 is about 0.8mΩ, and two pieces of AOCR38232 are needed in parallel to reduce the resistance further. The current path is symmetrical between the top and the bottom of the board to maintain the current balance. In this example, the distance between two MOSFETs is about 3 mm to avoid heating each other. Maximizing the copper area of the power path and adding some vias for dissipation on the copper pads near the MOSFET are good design tips to improve the heat dissipation capacity and to reduce the rising temperature of the MOSFET.

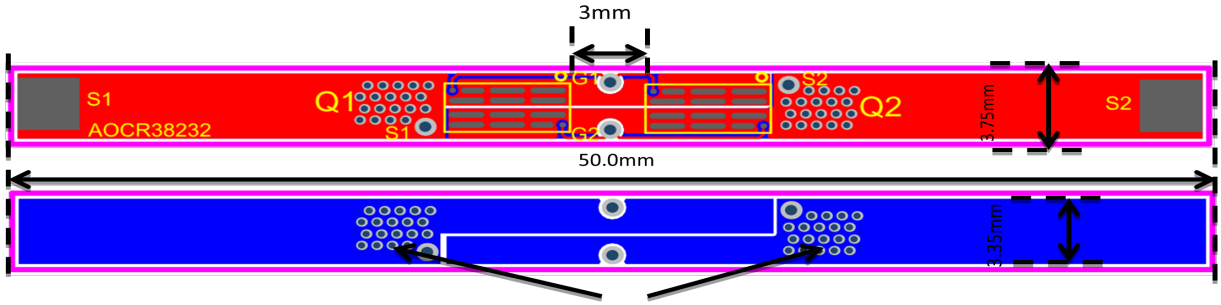
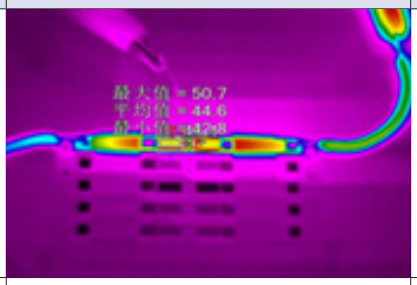
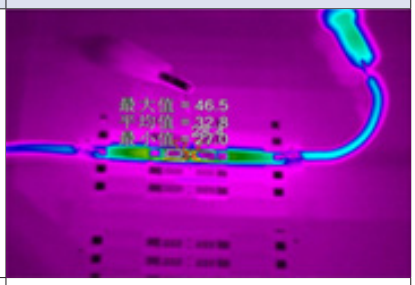
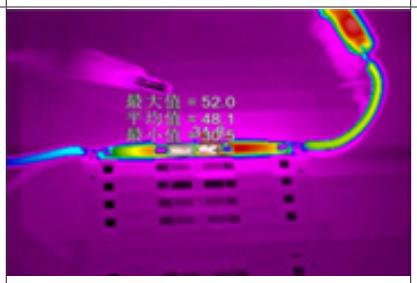
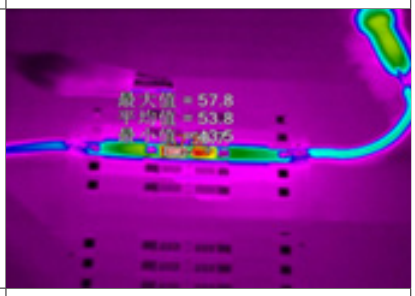


Figure 30. Heat Sink: Aperture 12 mil, Spacing 25 mil

When using an infrared (IR) thermometer to measure the surface temperature rise of the MOSFET, you will need to ensure proper usage of the IR thermometer since the surface emissivity can be different between different MOSFETs. Therefore, the optical refractive indices are also different. Metal has a lower optical refractive index than silicon. If the thermal measurement shows a lower temperature with higher $R_{DS(ON)}$ compared with lower $R_{DS(ON)}$, under the same conditions. Intuitively, these measured results are incorrect.

In order to most accurately capture the MOSEFT's temperature rise with an infrared thermometer, it is best to coat its surface with a high-optical refractive index black paint. In this way, a more accurate temperature rise can be obtained without needing to account for different material considerations. When black paint was used on the surface of AOCR38232, the measured temperature rise was only 1.3°C. Without any coating on the surface, the measured temperature rise was 11.3°C. The results are shown in Table 2.

Table 2. Temperature Rise with and Without Coating

Part Number	9.4A for 10 Minutes	Part Number	9.4A for 10 Minutes
AOCR38232 without Coating		Competitor without Coating	
Max	50.7°C	Max	46.5°C
AOCR38232 with Coating		Competitor with Coating	
Max	52°C	Max	57.8°C
Difference With/Without	+1.3°C	Max	+11.3°C

Output Leakage Current

In the battery pack production process, even though the charge MOSFET and discharge MOSFET are both off, when the battery voltage imposes on the MOSFET, sometimes it still causes the output leakage current through the MOSFET. Usually, the leakage current is very small and has no effect on the system. However, if the leakage current is higher, up to 100 nA, which is still within the limits of the datasheet, this leakage current will have a certain voltage on the output impedance.

Usually, the output impedance is around 10 MΩ. The voltage is equal to the product of the output impedance and the leakage current. In the above conditions, the output voltage is 1V, 100nA*10MΩ. Using BQ20Z45, when the output voltage is between P+ and P- is higher than 0.8V, the IC will judge that the charging voltage is imposed on the P+ end. The charge MOSFET is turned on by the pre-charging function of the IC attempting to charge the battery. As a result, the IC starts to operate, and the static power loss of the battery will be increased. In critical cases, the battery will run out of power.

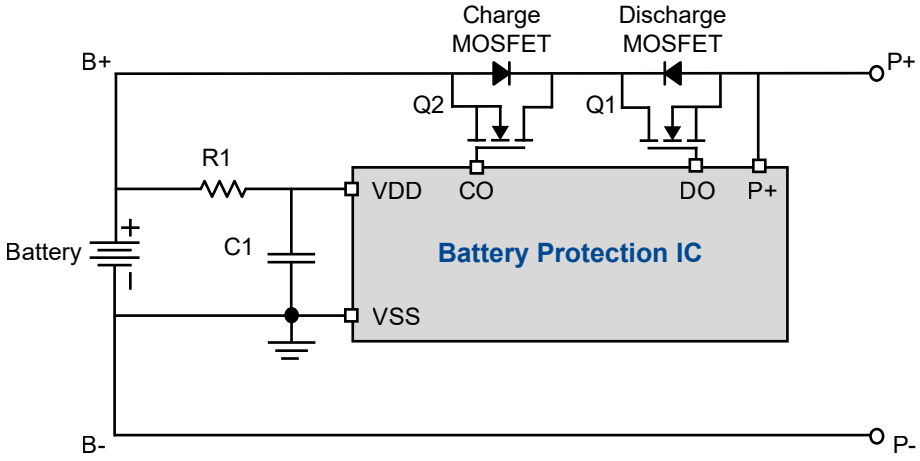


Figure 31. Battery Protection Board Circuit Diagram

Usually, IDSS of 30V MOSFET is less than 1μA in the datasheet. In a practical notebook battery application, the battery voltage is usually from 9V to 13.2V. It is unknown whether the leakage current IDSS of the discharge MOSFET is higher than 100nA or not under the battery voltage of 13.2V.

Solutions to Avoid Output Leakage Current

In an actual system, the output terminals of the battery are connected to the motherboard, which includes capacitors, resistors, and many other devices. These components could enable a certain leakage current. The measured impedance of the interfaces of the motherboard battery is generally less than 1MΩ. The above leakage current through 1MΩ impedance should not result in any issue in the system after the battery pack is connected.

There are two solutions to avoid output leakage current impact when the battery pack is not connected to the motherboard during any stage of manufacturing steps.

Solution: It is recommended to place a 1MΩ resistor in parallel with the output terminals of the battery pack P+ and P-, as shown in Figure 28. The issue can be removed effectively after testing the actual application of customers.

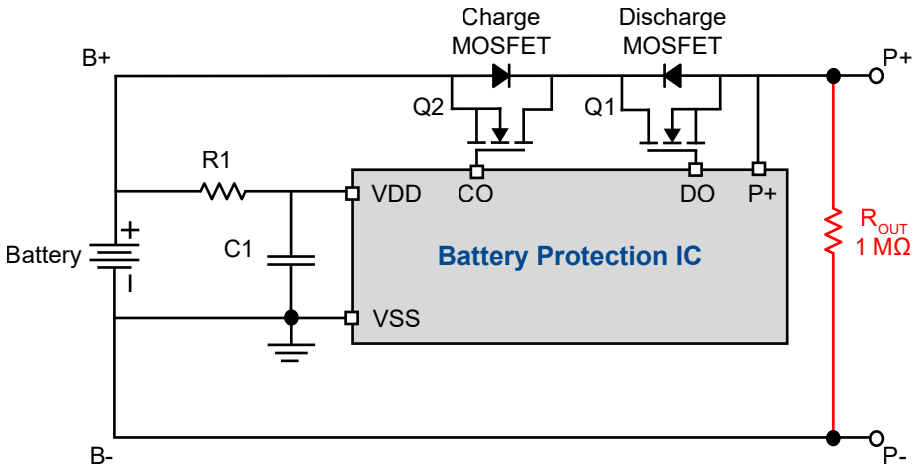


Figure 32. Parallel Output Resistor

After adding a 1MΩ resistor, the P+ terminal voltage caused by the leakage current will drop to 0.46V, and the MOSFET is not turned on by BQ20Z45.

Table 3. P+ Voltage vs. Output Resistance

Leakage Abnormal Board					
Parallel Resistance	None	8.2M	6.2M	2.7M	1M
P+ Voltage	5.5V	1.03V	0.92V	0.81V	0.46V

The disadvantage of placing this resistor is that is causes the battery to lightly discharge. For example, if the leakage current through this resistor is 0.46μA=0.46V/1M. The total energy consumed by the resistor during ten years of battery pack storage time is equal to 0.46μA*24 hours*365 days*10 years=40.3mA*hours. It is only less than 1 percent of the normal 4100mA*hour battery energy of the notebook. It is not a problem.

The output 1MΩ discharge resistor can also be placed on the test station of battery pack manufacturing lines.

Solution B: It is recommended that the detection threshold value of the P+ terminal voltage for the IC's pre-charging function should be increased from 0.8V to 2V for a single battery and to 6V for three battery cells in serial. With these values, the system could operate normally, even though the leakage current is larger.

The Future MOSFET of and WLCSP Technology

Figure 33 presents the roadmap for CSP silicon technology. The trend in chip technology indicates a reduction in cell pitch towards finer dimensions. Currently, power MOSFET devices predominantly utilize Wafer Level Chip Scale Packaging (WLCSP), which is characterized by the integration of circuits at the wafer-level.

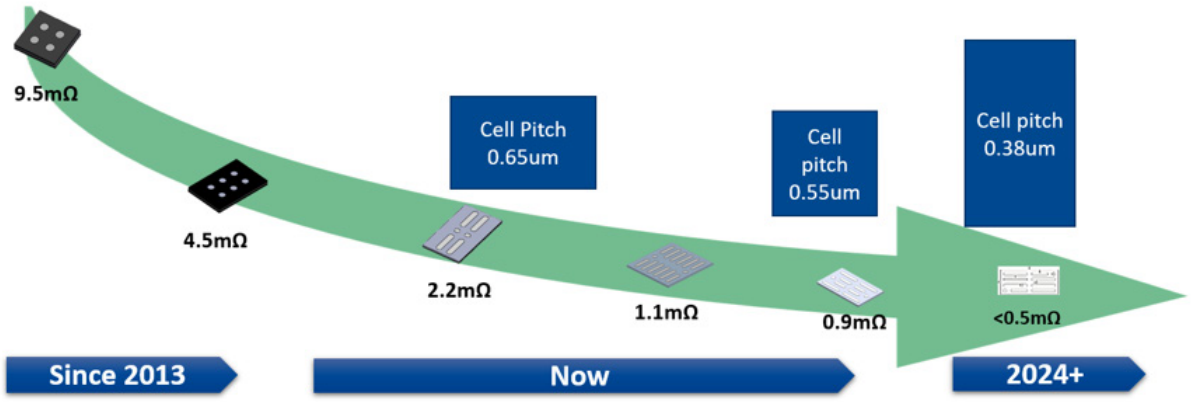


Figure 33. CSP Silicon Technology Roadmap

When WLCSP dies are regarded as devices that connect directly to the PCB, the primary benefits include minimized inductance, reduced package size, and improved thermal conduction properties. This interconnection technology presents numerous advantages, such as enhanced electrical performance characterized by lower inductance, achieved by eliminating wire bonds and leads typically found in conventional plastic packaging. Additionally, WLCSP offers a lighter and thinner package profile, as it does not require a lead frame or molding compound. Furthermore, the self-aligning nature of the low mass die during solder attachment contributes to high assembly yields for WLCSP.

AOS MRigidCSP™ products deliver exceptional solutions for compact form factors in mobile devices, featuring lower resistance and enhanced mechanical strength. The MRigidCSP™ technology is also advantageous for larger MOSFETs used in single or common-drain configurations, accommodating various aspect ratios. This process provides increased mechanical strength compared to the standard WLCSP method, facilitating solutions for thin notebooks where the maximum device height of standard packages is not feasible.

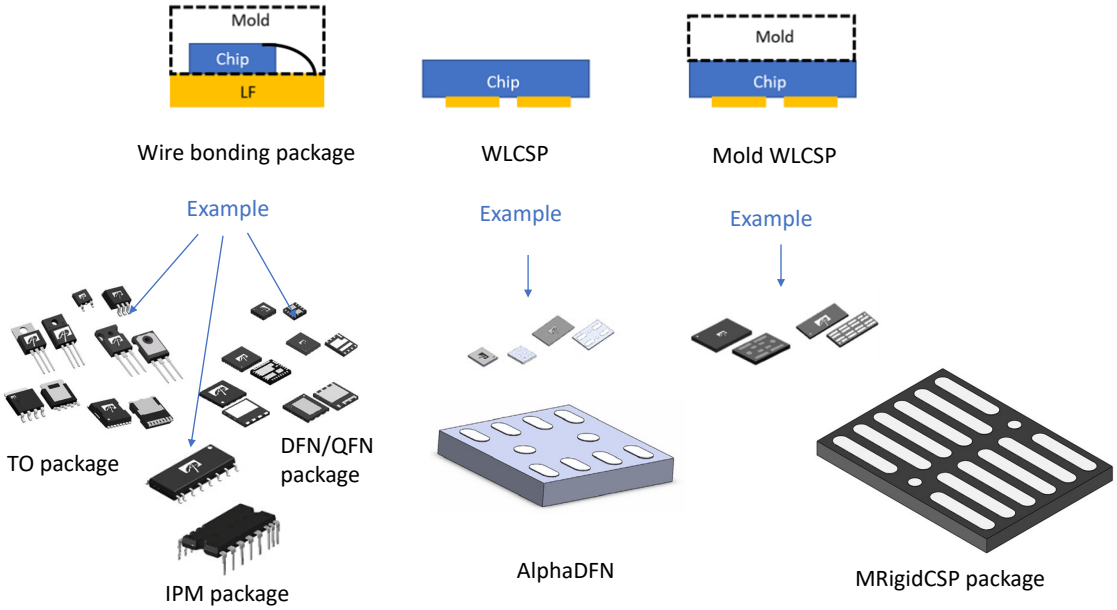


Figure 34. Comparison Between Traditional Package, WLCSP and AOS MRigid

Die Mechanical Strength Test

The point-load bending test (described in the following session) is a widely utilized method for assessing the die strength, primarily influenced by the surface characteristics of the die, such as the direction of grinding marks and surface roughness, as well as the presence of edge cracks, commonly referred to as chipping, which occurs during the dicing process. In response to the demands of microelectronics circuits, advancements in integrated circuit (IC) manufacturing technology and enhancements in assembly process capabilities have been propelled by the trend towards smaller die sizes and reduced wafer thickness. Given the inherently brittle nature of silicon, high stress concentrations on the die can lead to challenges in packaging, assembly, and reliability testing. The primary challenge faced by the latest generation of packaging materials is the production of large die with high aspect ratio and thinner dies. Due to their diminutive dimensions and thin profiles, accurately determining the fracture strength of silicon wafers may not suffice for ensuring robust packaging, assembly, and reliability testing.

The impact of die thickness on die strength has been extensively examined in both the AOS experiment and mechanical studies. Findings indicate that die strength is significantly influenced by its geometry, thickness, and structural composition. A series of bending force values, which correlate with die thickness and structure, has been derived from three-point bending tests. The accompanying illustration compares the bending forces of the typical AlphaDFN™ and MRigidCSP™, in Figure 35.

For AlphaDFN, the bending force will strongly depend on the silicon substrate thickness while for MRigidCSP™ the bending force is less depending on the silicon substrate thickness since the silicon die is supported by molding compound. Notably, MRigid exhibits 6-7 times greater mechanical strength than competitor's parts at the same die size (Figure 36). AlphaDFN represents our standard MOSFET product, characterized by a straightforward chip structure (die plus backside metal) without an additional molding layer. In contrast, MRigidCSP™ is our latest offering, which incorporates a new molding layer into the original MOSFET WLCSP package devices. This molding layer significantly enhances the mechanical strength of the die. Figure 37 illustrates the advantages of AOS MRigidCSP™, including superior mechanical strength, reduced warpage, and enhanced electrical optimization. This is achieved through AOS' innovative packaging technology, which involves grinding the die to 1.35 mils while simultaneously adding the molding layer.

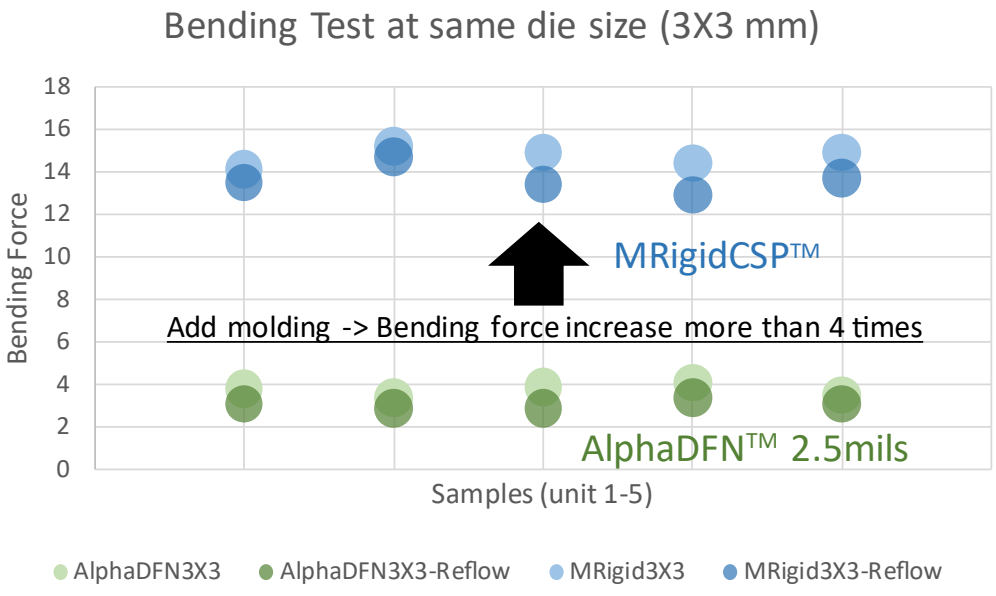
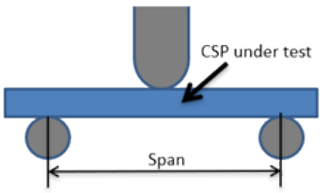


Figure 35. Typical Bending Force Comparison Between MRigid and AlphaDFN

MRigidCSP™ ~7X Stronger on Mechanical Stress



AOCR33135A	Bending Test
Average (N)	7.46
Average strength per unit width (N/mm)	5.3
Competitor	
Average (N)	0.97
Average strength per unit width (N/mm)	0.7

Figure 36. Bending force comparison between AOS MRigid and competitor (for similar package size and aspect ratio)
No need to specify AOCR, just use MRigidCSP™

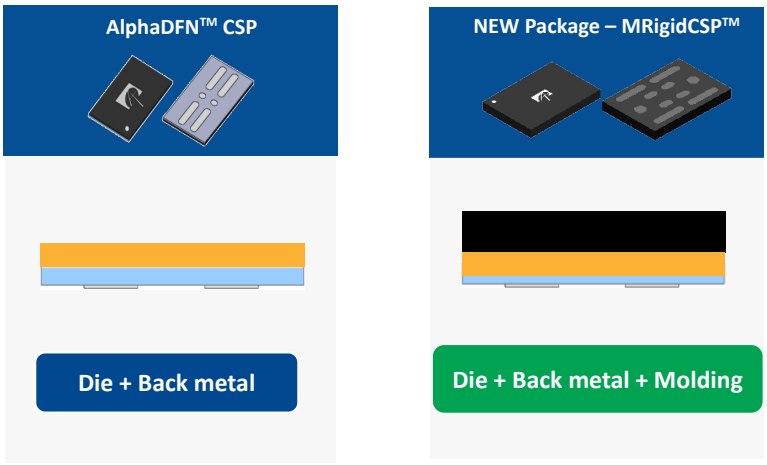


Figure 37. Structure Comparison Between MRigid and 2.5mils AlphADFN

The three-point bending test is widely recognized as the standard method for assessing the mechanical strength properties of a sample. This procedure induces a bending moment within the specimen, resulting in both compressive and tensile stresses.

The AOS bending test protocol in Figure 38, specifies the distance between supports and the position of the bending head. Each test sample is accurately positioned, and an appropriate speed is employed for the downward application of force. Following the test, the force reading in Figure 39 at the point of fracture is recorded. This information is essential for calculating the material's flexural stress, strain, and modulus. Additionally, the fractured specimen undergoes examination to analyze the failure characteristics. The following elements are critical for establishing the parameters of the bending test.

- Support span: The distance between the two parallel supports, which is determined by the material and test parameters
- Alignment: The supports and loading edge must be aligned properly to apply the load uniformly
- Sample placement: The specimen must be placed on the supports so that it protrudes at the sides
- Loading: The load is applied at the midpoint of the specimen using the loading edge
- Speed: The crosshead speed of the machine can be set to a specific value

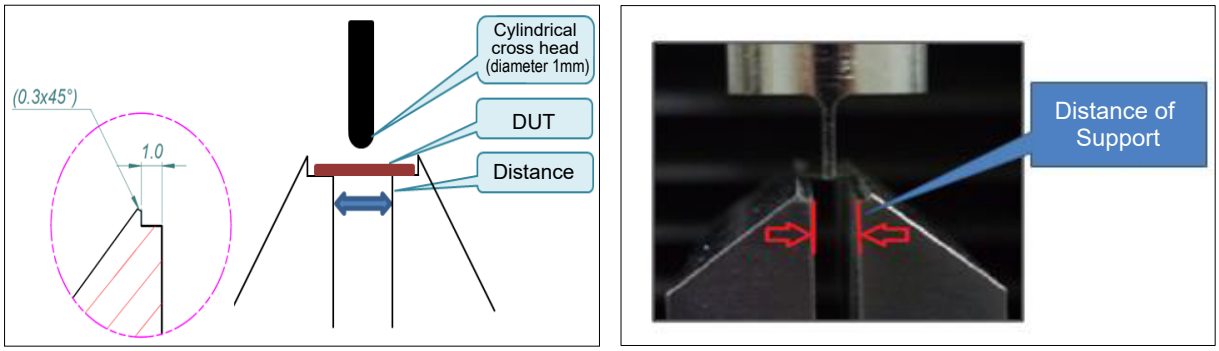
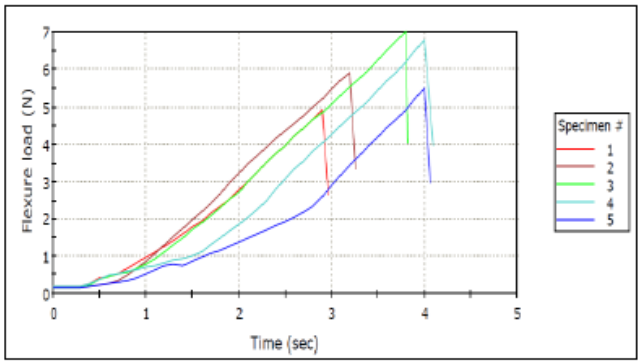


Figure 38. AOS Bending Test Procedure for a Sample Placement Position and Support Span Distance



	Maximum Flexure load (N)
1	4.89349
2	5.91748
3	6.99658
4	6.77664
5	5.48158

Figure 39. AOS Bending Test Result

Die Warpage

In Flip Chip semiconductor packaging, the warpage of the component in relation to the warpage of the PCB at different temperatures will have a considerable impact on the yield and reliability of the post-reflow assembly. As technology advances in smartphones, tablet PCs, and mobile electronic devices, there is a trend towards reducing chip thickness and size to achieve lower resistance. This reduction exacerbates the warpage issue, particularly in thin dies, leading to potential misalignment of components, incomplete solder coverage, increased stress on the components, or subpar solder joints. When warpage occurs, the solder paste may fail to adequately contact all solder pads, resulting in weak or incomplete solder connections that can cause open circuits or intermittent failures. Additionally, warpage may cause chips to shift slightly from their intended positions on the PCB, which can lead to misaligned connections with other components or even solder bridges forming between adjacent pads. The deformation force resulting from warpage can impose stress on the solder leads of the chip, heightening the risk of damage or reliability issues. Severe warpage complicates the precise placement of components on the PCB, potentially leading to increased rejection rates and production challenges. Therefore, it is essential for quality control processes to include checks for die warpage.

Die warpage represents a significant challenge within the semiconductor sector, primarily arising from discrepancies in the coefficient of thermal expansion (CTE) among various material layers. It can also result from thermal stress, uneven cooling, or internal stresses encountered during manufacturing. It is commonly assumed that the warpage of a newly fabricated die is negligible under ideal flat conditions, though this may not be a correct assumption. However, at elevated temperatures of 250°C, the unbalanced expansion forces between the backside metal and silicon generate a deformation force that causes the die to bend towards the silicon side (cry face). Upon cooling to 25°C, the backside metal exhibits a greater contraction force compared to silicon, which results in the die bending towards the metal side (smile face). The deformation phenomenon illustrated in Figures 40 and 41 is attributed to the differences in Coefficient of Thermal Expansion (CTE) among various materials, which results in an unbalanced force during the processes of shrinking and expanding, ultimately leading to warpage of the die.

The warpage behavior after SMT process on PCB board (called on-board warpage) is a bit complicate processes which involves the unit warpage behavior, PCB characteristics and solder melting and re-solidification.

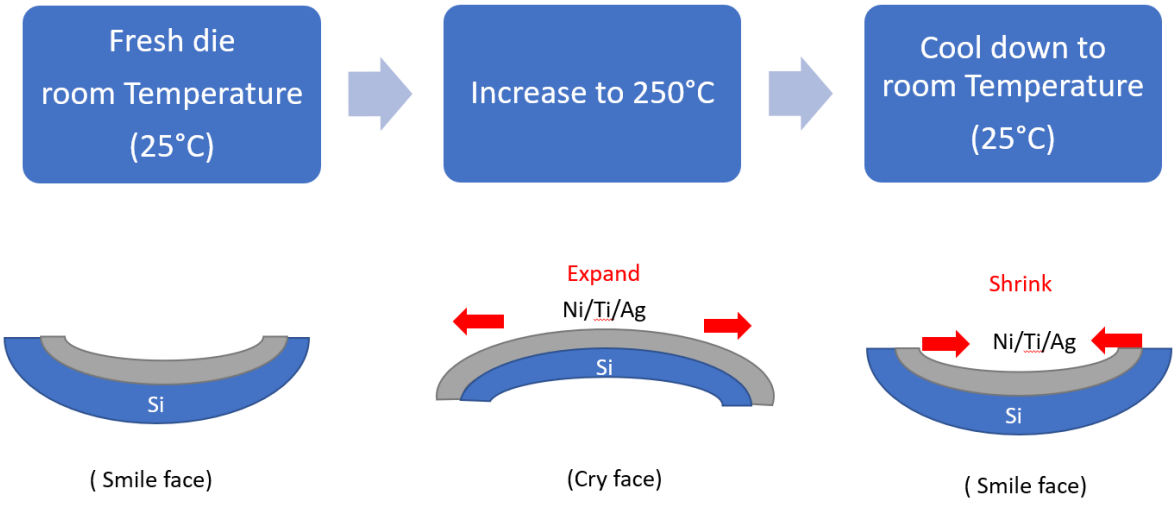


Figure 40. Unit die warpage under different temperature. The assumption of zero at room temp is an idea case. In the real case, the unit die level warpage is normally smile face.

Reflow

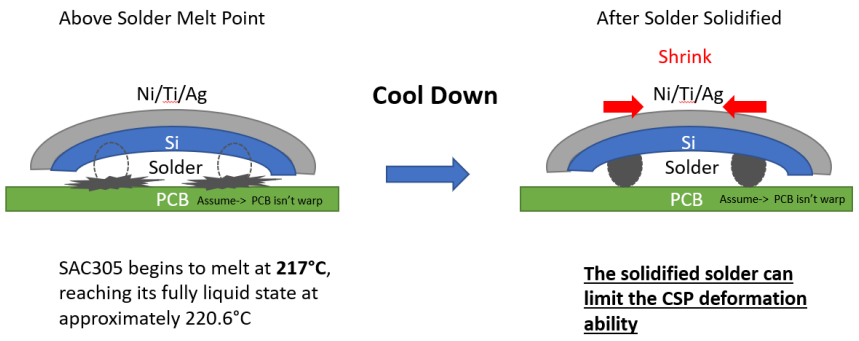


Figure 41. Die warpage illustration on SMT process, after cooling down to room temp, the die warpage normally stays as crying face since the unit is locked by solder.

Measuring warpage across the entire surface can be a labor-intensive task, often requiring point-to-point height measurements. Various measurement techniques exist for this purpose. AOS employs the Keyence 3D measurement tool to assess the varying height values across three cross lines of the sample. The maximum reading obtained from these three cross lines is utilized to determine the warpage value. Figure 42 illustrates the procedure for measuring warpage at AOS. The difference between the maximum and minimum values along this cross line is defined as the warpage reading. Figure 43 illustrates the AOS warpage specifications for several current components, both prior to and following the reflow process, along with supplementary on-board data.

To evaluate die warpage at elevated temperatures, AOS directly mounts our devices onto the coupon PCB board using surface mount technology (SMT). Figure 44 and Figure 45 illustrate an example of a coupon PCB board with dimensions of 35 mm in length, 14.7 mm in width, and 1.6 mm in thickness, constructed from FR-4 material and featuring NiAu pads. The reflow profile is illustrated in Figure 46. After following the reflow process, measurements of die warpage are taken, and the solder coverage is examined using an X-ray machine. An example of an X-ray image (Figure 47) is provided for our current MRigidCSP™ devices to assess solder coverage. The evaluation of solder coverage and warpage post-SMT is crucial in mitigating potential risks related to SMT assembly yield loss and solder joint quality issues.

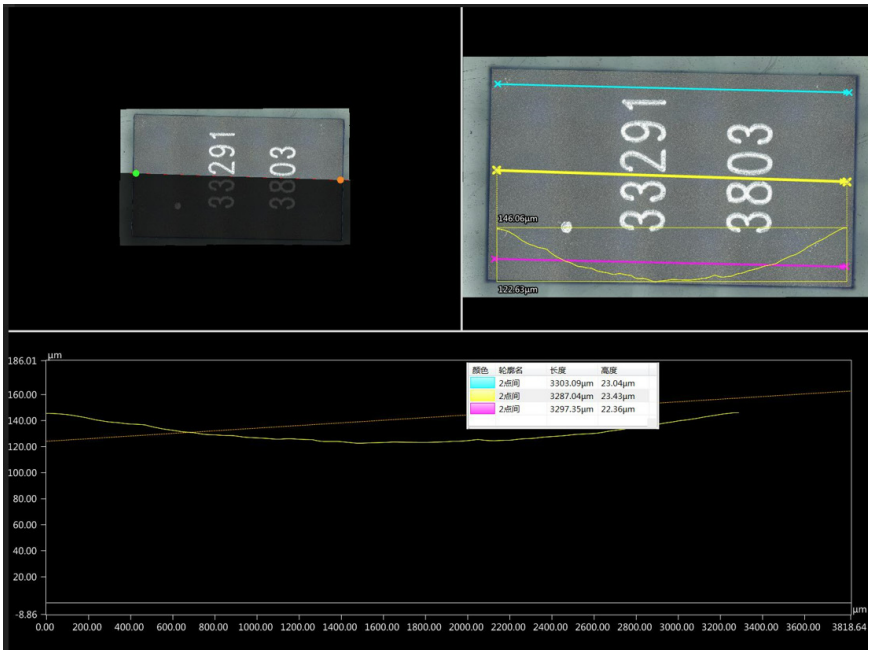


Figure 42. AOS warpage measurement procedure for fresh samples under room temperature

AOS Warpage Specifications

This list serves solely as a reference to illustrate the variations in warpage specifications across different devices. For precise and comprehensive information, please reach out directly to the AOS sales team.

- For AOCA
  - Fresh: 20μm
  - On board: 30μm
- For some special AOCA, such as thinner silicon and large aspect ratio
  - Fresh: 40μm
  - On board: 30μm
- For AOCR:
  - Fresh: 20μm
  - On board: 30μm

Figure 43. Example of AOS Warpage Specifications

(This list serves solely as a reference to illustrate the variations in warpage specifications across different devices. For precise and comprehensive information, please reach out directly to the AOS sales team).

Figure 44. Example of Coupon PCB Board for on-board Warpage Measurement

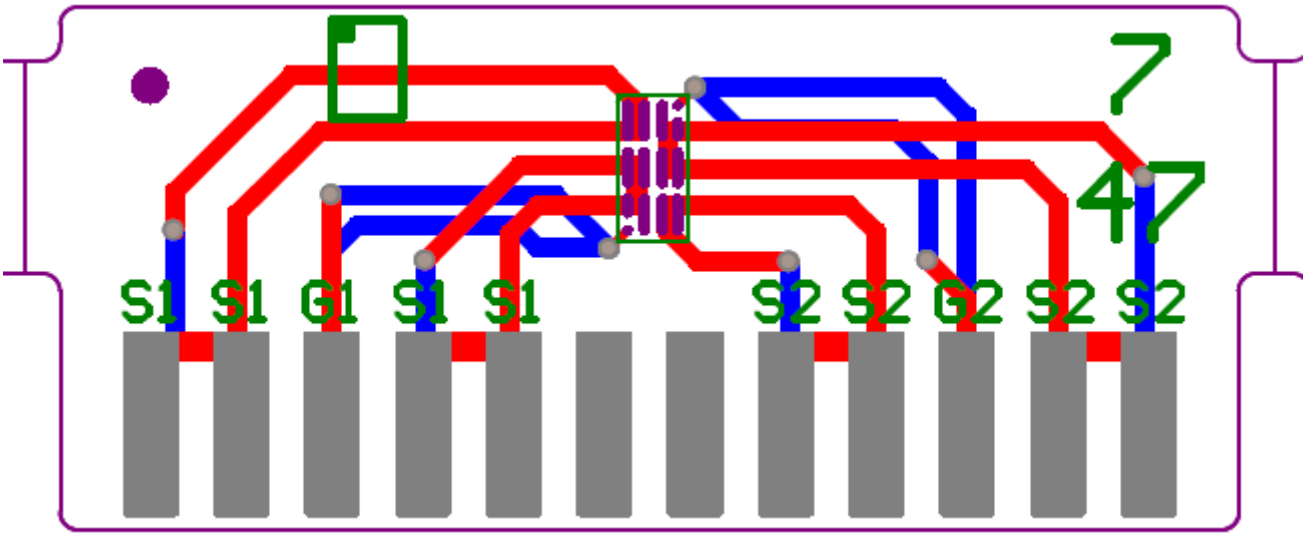
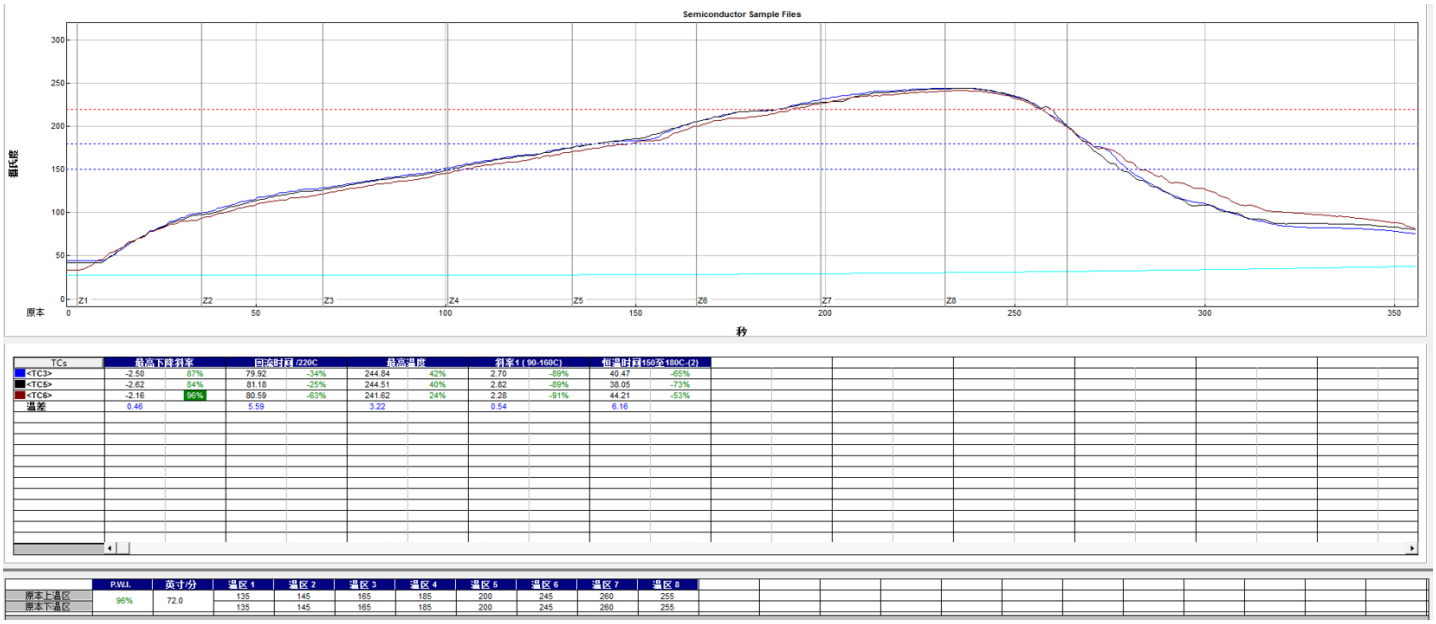


Figure 45. Example of PCB Board for Warpage Measurement



TCs	最高下降斜率		回流时间 /220C		最高温度		斜率1 (90-160C)		恒温时间150至180C-(2)	
<TC3>	-2.59	87%	79.92	-34%	244.84	-42%	2.70	-89%	40.47	-55%
<TC5>	-2.62	84%	81.18	-25%	244.51	40%	2.82	-89%	38.05	-73%
<TC6>	-2.16	90%	80.59	-63%	241.62	24%	2.28	-91%	44.21	-53%
温差	0.46		5.59		3.22		0.54		6.16	

	P.W.I.	英寸/分	温区 1	温区 2	温区 3	温区 4	温区 5	温区 6	温区 7	温区 8
原本上温区	96%	72.0	135	145	165	185	200	245	260	255
原本下温区			135	145	165	185	200	245	260	255

Figure 46. Example of Reflow Profile

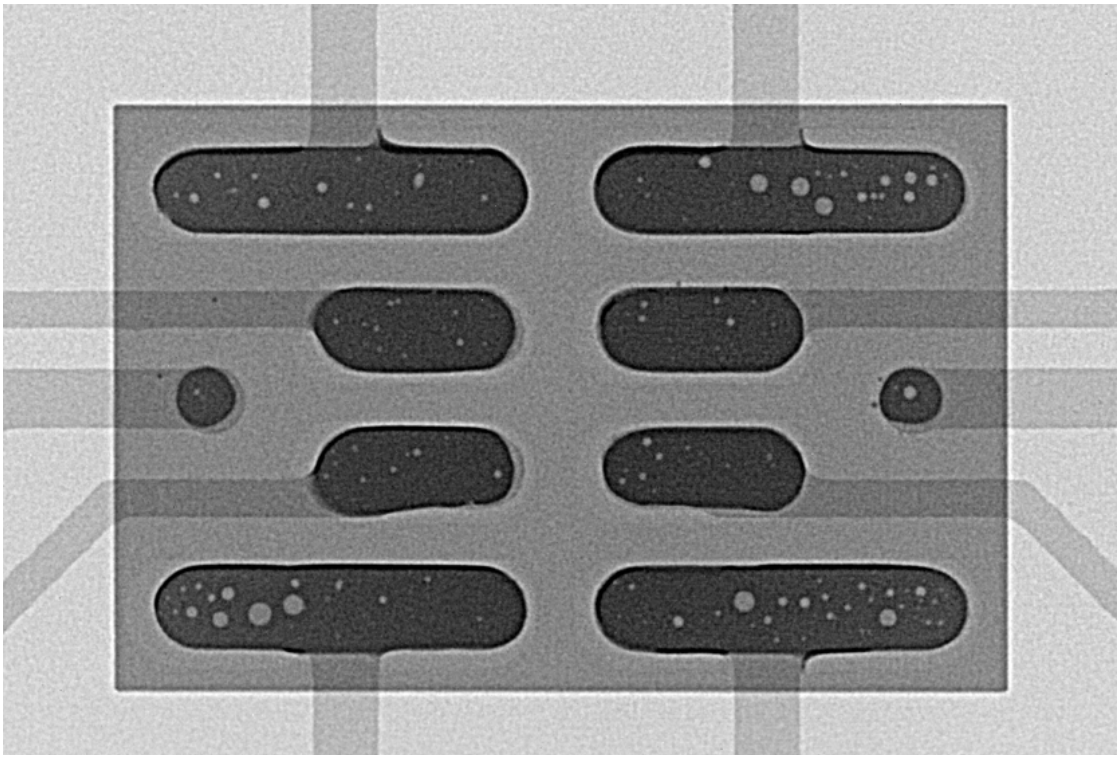


Figure 47. AOS X-ray Checking for Solder Cover on the Sample Parts on the Coupon PCB Board

One notable method is the Shadow Moiré technology, a full-field optical inspection technique widely employed in the semiconductor industry for assessing flatness, particularly under conditions of significant warpage at different temperatures. Observations on fresh AOS samples, prior to reflow, indicate that warpage increases as the die thickness decreases. Thinner dies exhibit greater susceptibility to temperature-induced warpage. A viable solution to mitigate this issue involves incorporating an additional molding layer to counterbalance the warpage effects associated with thinner dies. Consequently, the measured warpage of MRigidCSP at approximately 250°C is only 20 micrometers, which is one-third of the value reported by competitors, as shown in Figure 48. This reduced warpage enhances the yield during Surface Mount Technology (SMT) assembly and contributes to improved reliability and superior quality of solder joints.

AOS Warpage: 1/3 of the Competitor

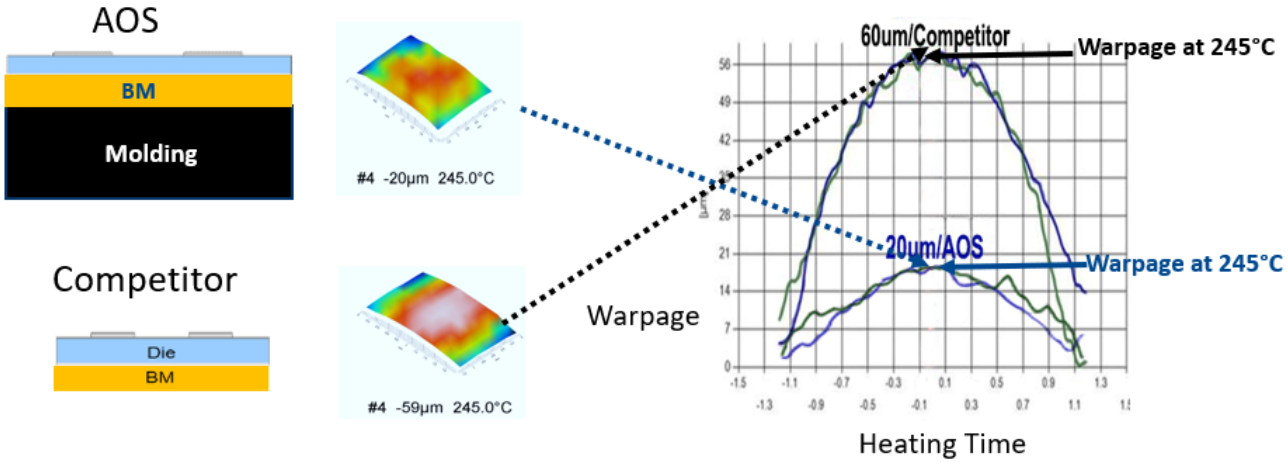


Figure 48. Warpage Comparison Between AOS MRigid and Competitor

Warpage is influenced not only by discrepancies in the coefficient of thermal expansion (CTE) among different material layers but also by factors such as layer thickness, device structure, die size, and aspect ratio. For power MOSFET products such as AphaDFN with a thickness exceeding 3 mils, warpage is not regarded as a concern during the surface mount technology (SMT) process. Conversely, for thinner products with a thickness of 2.5 mils or less, warpage presents a more significant challenge that necessitates the implementation of specialized structural solutions.

Factors impacting warpage:

- Assembly environment temperature
- Material CTE
- Layer thickness
- Package structure
- Die size
- Aspect ratio

AOS' MRigidCSP™ technology enhances both electrical performance and mechanical strength. Furthermore, it addresses production challenges linked to battery management applications, aiming to control warpage in scenarios involving higher aspect ratios, larger die sizes, and thinner die thicknesses.

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.