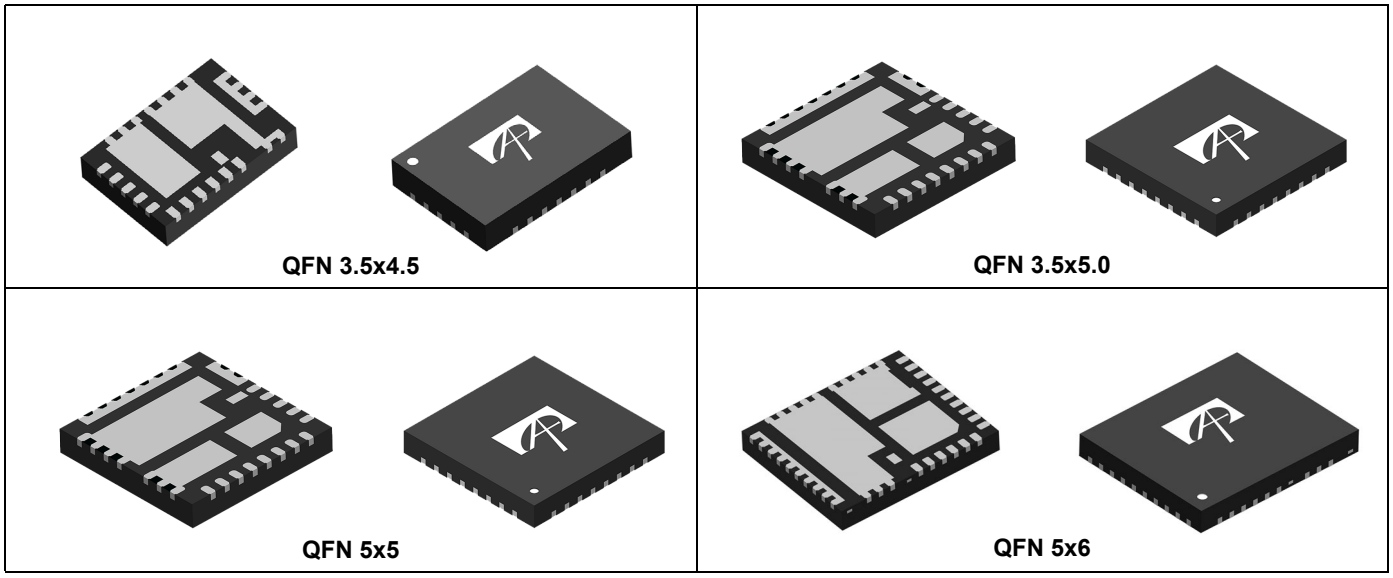
Board Assembly Guideline for AOS DrMOS and Smart Power Stage

Introduction and Packaging Description

Multiple silicon devices packed into Quad Flat No-Lead (QFN) packages are being used in system power delivery applications. AOS's DrMOS and smart power stage (SPS) products offer multiple package sizes such as QFN3.5x4.5, QFN3.5x5, QFN5x5 and QFN5x6 to fit various power requirements. They offer high efficiency, high power density, and high switching frequency in synchronous buck DC-DC converter applications in high-performance computing, telecom, high-end graph cards, etc. This application note is to provide board assembly guidelines. These guidelines cover printed circuit board attributes and design, stencil pattern design, and assembly process.

Board Assembly Challenges for DrMOS and SPS

Various QFN package sizes are listed below. These packages have similar features such as fine pin pitch and exposed pads for IC, high-side and low-side die paddles and low-side gate. We will use the QFN5x5 package as an example to illustrate the challenges and how to address them during SMT assembly.



The leads for the QFN packages are designed to have fine pitch with 0.25mm distance between leads. It is recommended to use the SMD pad design to avoid shorts caused by solder bridging between leads.

PCB Pad Design and Design Guideline

PCB Design

- AOS follows the generic requirements for Surface Mount Design and Land Pattern standards from the Institute for Printed Circuits (IPC), IPC-7351B.
- All AOS DrMOS and Smart Power Stage QFN5x5products will be surface mounted on PCB and require reflow soldering to form a good solder joint with PCB. During the reflow process, the solder surface tension will help the device self-aligned to the land pads in case there are any unintended misalignments at the SMT process. It is suggested to follow the recommended land pattern design; however, the customers might have some modifications based on their own application needs.

Solder Mask Defined (SMD) and Non-solder Mask Defined (NSMD) PCB

- Both SMD and NSMD PCB are supported for applications, depending on the PCB designer, target application and board design.
- For the same PCB layout rule, NSMD has the advantage of offering larger PCB pad openings which allow the solder to wet and adhere to the sidewall of the PCB pads. The solder joint integrity will be improved.
- On the other hand, SMD will help prevent a potential solder bridging issue since the solder will not wet on the solder mask and will be contained within the pads during solder reflow
- The lead pitch/spacing of the QFN5x5 is 0.50mm/0.25mm. This is considered a fine pitch PCB layout design and it is recommended to use SMD pad design to avoid solder bridging, resulting in lead-to-lead shorts.

Figure 1. Cross Section of Non-solder Mask Defined (NSMD) and Solder Mask Defined (SMD) Land Patterns

PCB Pad Surface Finish

PCBs have Copper (Cu) on their surface, and the bare Cu will oxidize without further surface protection layer. Oxidized Cu surface will make the circuit boards unusable. It is critical to have a final surface layer on the Cu to protect the Cu from oxidation. The surface finish layer also provides a solderable surface when assembling (soldering) the components to the PCB.

There are several types of surface finishes used in the industry, depending on the application and manufacturing factors, such as cost, lead pitch, surface flatness, multiple reflow, reworkability, shelf life, bondability, etc.

The widely used surfaces are:

- Immersion Tin (ISn) – Flat surface, re-workable, but easy to cause handling damage
- OSP (Organic Solderability Preservative) – A water-based organic compound that selectively bonds to copper surfaces to provide an organometallic layer. This thin organometallic layer protects the copper prior to soldering. It offers a flat surface, is cost-effective and good for fine pitch application, but short shelf life exposes Cu during the final assembly.
- Electroless Nickel Immersion Gold (ENiG) – a two-layer metallic coatings of Ni and Au to protect Cu with Ni being a barrier between Cu and Au. The Au layer protects Ni during storage and offers good solder wetting and low contact resistance. Although it is relatively expensive, it offers a very flat surface and long shelf life. ENiG is now the most widely used finish in the PCB industry.

It is well known that the type of surface finish affects solder wetting, solder joint strength, voiding and board-level reliability. No specific type of finish is required for AOS QFN5x5 package; however, the choice of the surface finish shall consider the optimum compatibility of the solder paste with respect to the board surface finishes.

Land Pattern Design

The general pin-out of QFN5x5 DrMOS shows:

- If Pin6/8 (VIN) shorts to pin7 (PHASE) in the PCB board by solder bridge, the pin7 wire bonds will fuse and cause high-side MOSFET to operate in the linear mode and become damaged.
- If Pin5 (BOOT) shorts to Pin4 (PGND)/Pin6 (VIN), it will cause high-side MOSFET damage.
- If Pin27 (GL) shorts to Pin28 (PGND) or Pin26 (VSWH), the high-side and/or low-side MOSFETs have the chance of becoming damaged.

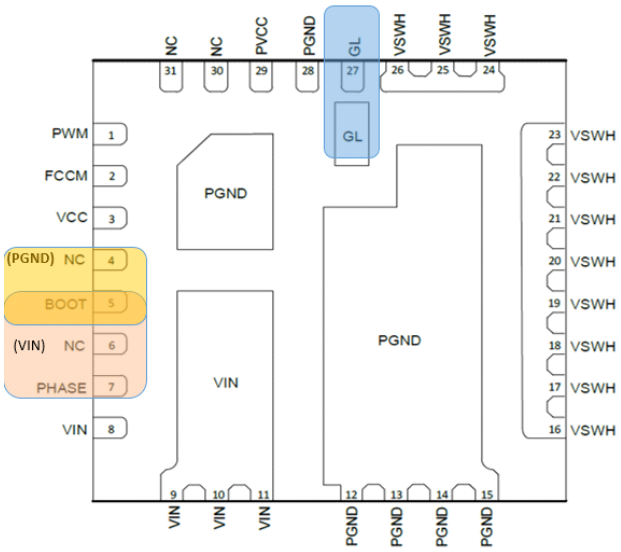


Figure 2. General Pin Out of QFN5x5 DrMOS

- The recommended land pad pattern for QFN5x5 is shown below.
- Hiding Pin4 (PGND) can reduce the risk of Pin5 (BOOT) shorting to PGND.
- Hiding Pin6 (VIN) can reduce the risk of Pin7 (PHASE) and/or Pin5 (BOOT) shorting to VIN.
- Hiding Pin27 and GL can avoid GL shorts to GND and VSWH.

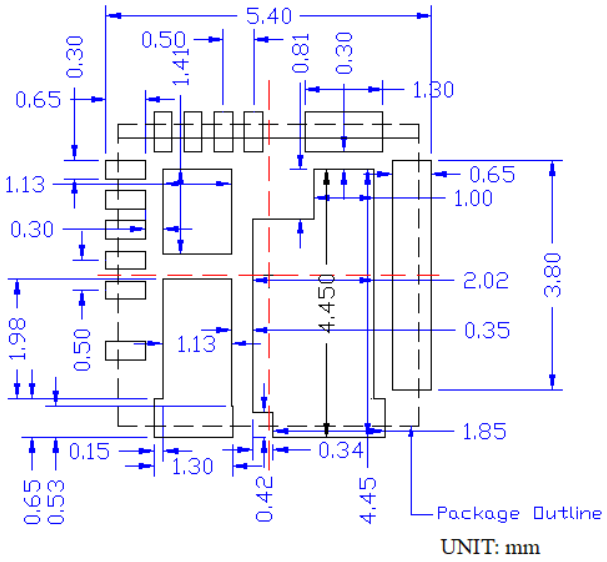


Figure 3. Recommended Land Pattern for QFN5x5 DrMOS

The recommended land pad pattern considers the tolerances of the PCB fabrication and the DrMOS placement during assembly. This tolerance can vary up to a maximum of 0.10 mm to avoid misalignment after reflow.

PCBA Consideration

Solder Paste

The commonly used solder pastes for mounting DrMOS and SPS packages are the Type 3 and Type 4 pastes with metal loading from 88% to 90%. No-clean flux is recommended for DrMOS and SPS mounting such as ROL0 rosin-based, low-activity and halide free. No-clean flux eliminates the need for cleaning trapped flux residue under the package due to the low standoff heights of the solder joints.

Solder pastes are sensitive to storage conditions and exposure time. If the paste is beyond its exposure limit, issues such as voiding and solder joint reliability can occur. The storage condition also affects the solder paste quality. Following the handling and storage recommendations from the solder paste manufacturer is important.

The most common solder alloys in board mounting assembly is 96.5Sn/3.0Ag/0.5Cu (SAC305) since it is the lead-free solder paste alloy choice for electronics today. The aperture design of the stencil and board surface finish should be evaluated first to avoid rejects such as solder balling, voiding and wettability issues.

Stencil Design

The aperture for leads and exposed die pad should be designed relatively smaller than the board pads.

The Apertures for Exposed Pad

The apertures for the exposed pad are about 50 to 60% of the land pad size.

The Apertures for Leads

The apertures for the leads are smaller than the land pads to balance the thickness of the solder joint from the exposed die pad.

The Recommended Stencil Thickness

The recommended stencil thickness is 0.125 mm.

The stencil is usually manufactured by laser cut. For the recommended apertures, the area ratios and aspect should meet the typical minimum acceptable value for stencil manufacture. The formula are:

$$Area\ Ratio = \frac{Area\ of\ Pad}{Area\ of\ Aperture\ Walls} > 0.66$$

$$Aspect\ Ratio = \frac{Width\ of\ Aperature}{Thickness\ of\ Stencil\ Foil} > 1.5$$

Board Mount Assembly

Optimize the coverage of the printed solder paste is important for board mount assembly. An insufficient solder paste print can cause irregular solder joints. The irregular solder joints can be smaller than desired or partially formed joints. Relatively large voids can also be caused by insufficient solders. Large voids can also be caused by the surface finish, solder paste alloy, reflow profile and substrate condition.

Too much solder paste, however, may also cause problems. Excessive solder can cause solder balling around the perimeter or underneath the package. The situation can be even worse when the solder paste out gases more. The physical reason is: the out gassing of the flux during reflow pushes the solder out of the pads, which results in solder balls. Solder balls can lead to solder bridges between exposed pads and leads to form.

Component Placement

Mounting the package manually is not recommended since poor solder joints can be formed due to inaccurate placement of the package on the board. Depending on the placement accuracy of the pick & place machine, the DrMOS and SPS packages can tolerate up to a certain amount of placement offset and still achieve acceptable solder joints. This realignment of the package with the board depends on solder pastes. To confirm the limits of the realignment, the assembly process needs to be characterized.

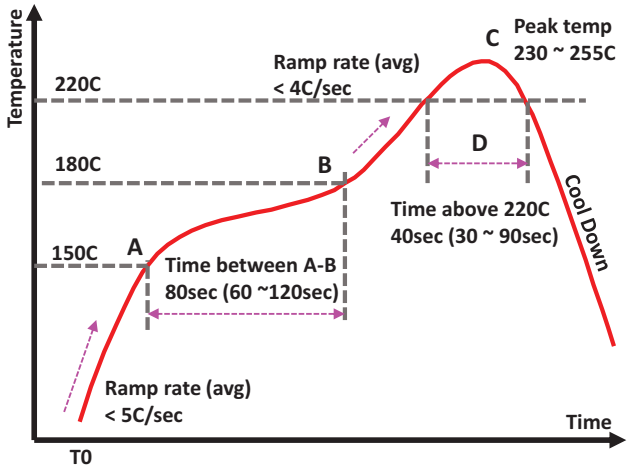
Placement pressure is also an important factor for component placement. Too much pressure exerted on the package may cause the solder to spread excessively, producing solder balls and bridges during reflow. Controlling the placement height is recommended. Component bond machines with the ability to control the height or the amount of bonding force during component placement are recommended. Also, process characterization is necessary to achieve sufficient adhesion between the pad and the solder to avoid package fall-off or misalignment during transport from the bond machine to the reflow oven.

Solder Reflow

The soldering oven temperature profile is one of the most critical controls in reflow soldering for achieving quality solder joints. The temperature profile parameters depend on the solder paste used in the PCBA processes. The actual reflow temperature settings need to be determined by the end-users, based on the thermal loading effect, recommendations from the solder paste manufacturers and the reflow oven. The reflow temperature shown below is a suggested profile for SAC305 paste. The table associated with the profile shows the recommended temperature range and time duration for each temperature zone:

- Ramp-up to soak (pre-heating, T0 to point A)
- Pre-heating and soak time (Point A to point B)
- Ramp up and reflow (Point C to the peak reflow temperature)
- D is the time duration above 220°C

After the peak temperature, the PCB will be cooled down. Fast cooling will prevent the excess formation of the intermetallic compound (IMC) and results in a finer grain structure of the solder alloy. The cool down rate shall not be faster than 6^{o}C/sec to avoid overstress. The maximum cool down rate should also be verified by the PCB material suppliers.



Point		Standard	Upper	Lower
A	Pre-heat start point	150C	160C	140C
B	Pre-heat end point	180C	200C	160C
A-B	Pre-heat time	80sec	100sec	60sec
C	Peak temperature	240C	255C	230C
D	Time above 220C	40sec	90sec	30sec

Figure 4. SMT Solder Reflow Profile for SAC305 Solder Paste