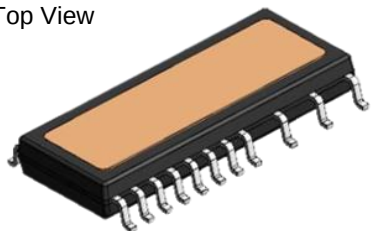
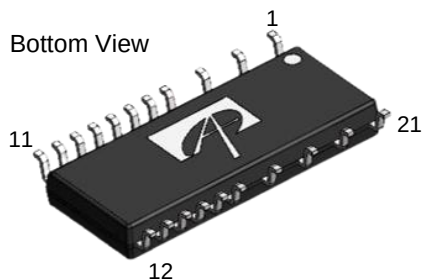


External View

Top View



Bottom View



Features

- 600V-3A with the latest AOS IGBT and FRD technology
- DBC-embedded SMD type
- 3-phase inverter module including HVIC gate drivers
- Built-in bootstrap diodes with current-limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Over-temperature protection (OT)
- Short-circuit current protection (CSC)
- Bi-functional CF/EN pin for fault signal output and IPM enable / disable
- Input interface: 3.3V and 5V line, Schmitt trigger receiver circuit (Active high)
- Isolation rating of 1500Vrms/min

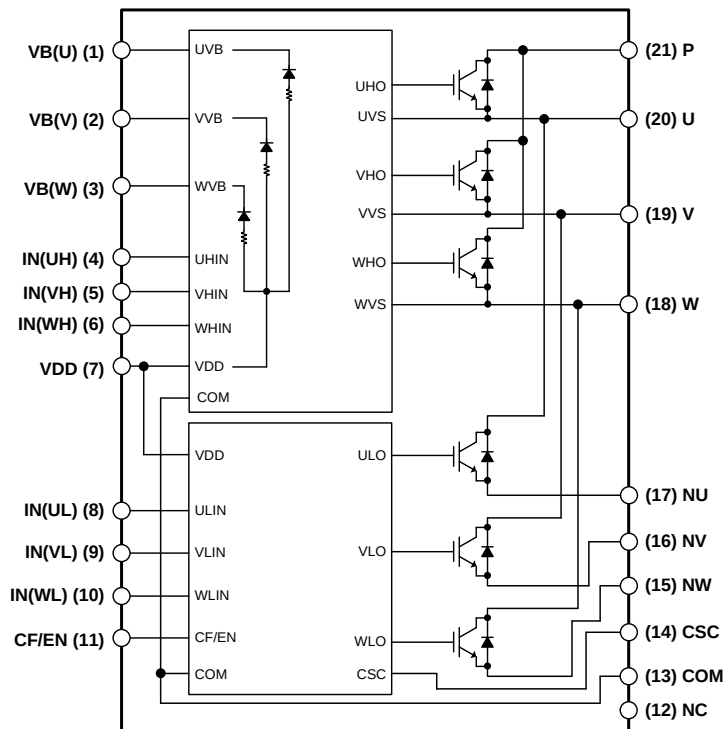
Applications

- AC 100~240Vrms low power motor drives
- Fan motors

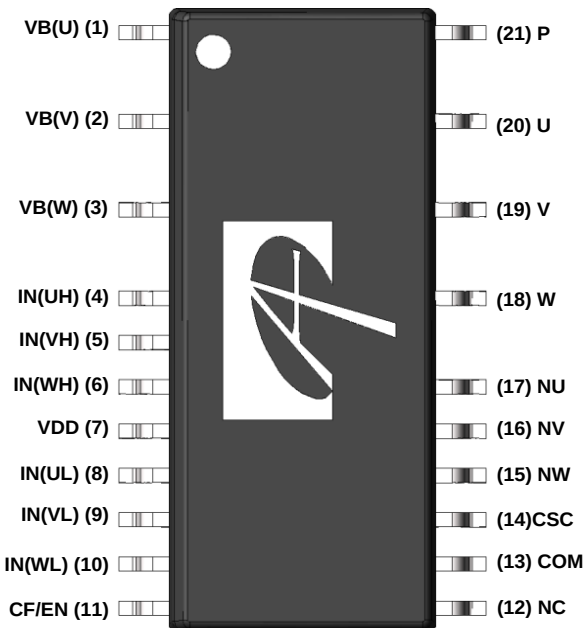


Size: 17.9 x 7.5 x 2.5 mm

Internal Equivalent Circuit



Bottom View



Ordering Information

Part Number	Package	Description
AIM7DT3AB60V3	IPM-7DA	N/A



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Please visit <https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf> for additional information.

Pin Description

Pin Number	Pin Name	Pin Function
1	VB(U)	High-side bias voltage for U-phase IGBT driving
2	VB(V)	High-side bias voltage for V-phase IGBT driving
3	VB(W)	High-side bias voltage for W-phase IGBT driving
4	IN(UH)	Signal input for high-side U-phase
5	IN(VH)	Signal input for high-side V-phase
6	IN(WH)	Signal input for high-side W-phase
7	VDD	Control supply voltage
8	IN(UL)	Signal input for low-side U-phase
9	IN(VL)	Signal input for low-side V-phase
10	IN(WL)	Signal input for low-side W-phase
11	CF/EN	Fault signal output with controllable duration and external enable or disable all low-side IGBTs
12	NC	No connection
13	COM	Common supply ground
14	CSC	Short-circuit current detection Input
15	NW	Negative dc-link input for W-phase
16	NV	Negative dc-link input for V-phase
17	NU	Negative dc-link input for U-phase
18	W	Output for W-phase
19	V	Output for V-phase
20	U	Output for U-phase
21	P	DC-link positive input

Absolute Maximum Ratings

$T_J=25^{\circ}\text{C}$, unless otherwise specified

Symbol	Parameter	Conditions	Ratings	Units
Inverter				
V_{PN}	Supply voltage	Applied between P-Nx, x=U, V, W	450	V
$V_{PN(surge)}$	Supply voltage (surge)	Applied between P-Nx	500	V
V_{CES}	Collector-emitter voltage	$T_J=25^{\circ}\text{C}$	600	V
I_C	IGBT collector current (continuous)	$T_C=80^{\circ}\text{C}$, $T_J<150^{\circ}\text{C}$	3.0	A
I_{CP}	IGBT collector current (pulsed)	$T_C=25^{\circ}\text{C}$, <100 μs pulse width	4.5	A
P_D	Maximum power dissipation	$T_C=25^{\circ}\text{C}$	37.8	W
T_J	Operating junction temperature		-40 to 150	$^{\circ}\text{C}$
Control (Protection)				
V_{DD}	Control supply voltage	Applied between VDD-COM	-0.3 ~ 20	V
V_{BS}	High-side control bias voltage	Applied between VB(x)-x	-0.3 ~ 20	V
V_{IN}	IN input voltage	Applied between IN(xH), IN(xL)-COM	-0.3 ~ $V_{DD}+0.5$	V
$V_{CF/EN}$	Fault output supply voltage	Applied between CF/EN-COM	-0.3 ~ 5.5	V
$I_{CF/EN}$	Fault output current	Sink current at CF/EN terminal	1	mA
V_{CSC}	Current sensing input voltage	Applied between CSC-COM	-0.3 ~ 5.5	V
Total System				
$V_{PN(PROT)}$	Self-protection supply voltage limit (Short-circuit protection capability)	$V_{DD}=13.5\text{--}16.5\text{V}$, Inverter part Non-repetitive, less than 2 μs	400	V
T_C	Module case operation temperature	Measurement point of T_C is provided in Figure 1	-40 to 125	$^{\circ}\text{C}$
T_{STG}	Storage temperature		-40 to 150	$^{\circ}\text{C}$
V_{ISO}	Isolation voltage	60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

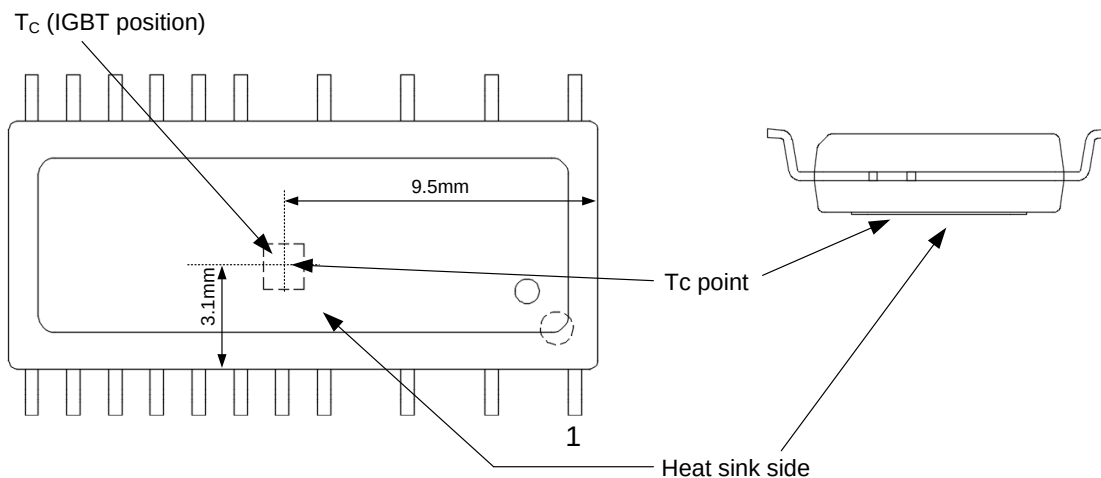


Figure 1. T_C Measurement Point

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 1)	Single IGBT	-	-	3.3	K/W
$R_{th(j-c)F}$		Single Diode	-	-	10.3	K/W

Note:

1. For the measurement point of case temperature (T_C), please refer to Figure 1.

Electrical Characteristics

$V_{DD}=15V$, $V_{BS}=15V$ and $T_J=25^{\circ}C$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Inverter							
V _{CE(SAT)}	Collector-emitter saturation voltage	V _{IN} =5V	I _C =2A, T _J =25°C	-	1.8	2.3	V
			I _C =2A, T _J =125°C	-	2.0	-	V
V _F	FWD forward voltage	V _{IN} =0V	I _F =2A	-	1.8	2.4	V
t _{OFF}	Switching time	V _{PN} =300V, I _C =2A, T _J =25°C, V _{IN} =0V ↔ 5V, Inductive load (high-side)		-	1.20	-	μs
t _f				-	0.17	-	μs
t _{ON}				-	1.10	-	μs
t _r				-	0.08	-	μs
t _{rr}				-	0.12	-	μs
I _{CES}	Collector-emitter leakage current	V _{IN} =0V, V _{CE} =600V	T _J =25°C	-	-	1	mA
			T _J =125°C	-	-	10	mA
Control (Protection)							
I _{QDD}	Quiescent VDD supply current	V _{IN(xL)} =V _{IN(xH)} =0V, VDD-COM		-	-	1.5	mA
		V _{IN(xL)} =5V, V _{IN(xH)} =0V, VDD-COM		-	-	2.6	mA
I _{QBS}	Quiescent VBS supply current	V _{IN(xL)} =V _{IN(xH)} =0V, VB(x)-X		-	-	0.1	mA
		V _{IN(xL)} =0V, V _{IN(xH)} =5V, VB(x)-X		-	-	1.0	mA
UV _{DDT}	VDD supply under-voltage protection	Trip level		10.3	11.4	12.5	V
UV _{DDR}		Reset level		10.8	11.9	13.0	V
UV _{BST}	VBS supply under-voltage protection	Trip level		8.0	9.0	10.0	V
UV _{BSR}		Reset level		9.0	10.0	11.0	V
I _{IN}	Input bias current	V _{IN} =5V		-	0.72	-	mA
V _{IN,TH(ON)}	ON threshold voltage	IN(xL), IN(xH)-COM		-	2.3	2.6	V
V _{IN,TH(OFF)}	OFF threshold voltage			0.8	1.2	-	V
V _{CSC(REF)}	Short-circuit trip level	CSC-COM (Note 2)		0.455	0.480	0.505	V
T _{OT}	Over-temperature protection (Note 3)	Trip level		115	135	145	°C
T _{OT(HYS)}		Reset hysteresis		-	30	-	°C
V _{CF/ENH}	Fault output voltage	V _{CSC} =0V		4.9	-	-	V
V _{CF/ENL}		V _{CSC} =1V		-	-	0.5	V
V _{CF/EN+}	CF/EN positive going threshold			-	1.9	2.2	V
V _{CF/EN-}	CF/EN negative going threshold			0.8	1.1	-	V
t _{FO}	Fault output pulse width	No C _{CF/EN} connected (Note 4)		20	-	-	μs
Bootstrap Diode							
V _{F(BSD)}	Bootstrap diode forward voltage	I _F =10mA including voltage drop by limiting resistor and bootstrap diode		-	2.5	-	V
R _{BSD}	Bootstrap diode equivalent resistance			-	250	-	Ω

Note:

- Short-circuit protection works only for low-side IGBTs.
- When the LVIC temperature exceeds OT Trip temperature level (T_{OT}), OT protection is triggered and fault outputs.
- Fault signal ($V_{CF/EN}$) outputs when SC, UV or OT protection is triggered. Its duration time can be controlled by using the capacitor (see Figure 2). It is noted that CF/EN output has min. 20 μs of t_{FO} pulse width when SC protection works.

Recommended Operation Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PN}	Supply voltage	Applied between P-Nx	0	300	450	V
V_{DD}	Control supply voltage	Applied between VDD-COM	13.5	15.0	16.5	V
V_{BS}	High-side bias voltage	Applied between VB(x)-x	13.5	15.0	18.5	V
dV_{DD}/dt , dV_{BS}/dt	Control supply voltage variation		-1	-	1	V/ μ s
t_{DEAD}	Dead time	For each input signal	1.5	-	-	μ s
f_{PWM}	PWM input frequency		-	16	-	kHz
$PW_{IN(ON)}$	Minimum input pulse width	(Note 5)	0.7	-	-	μ s
$PW_{IN(OFF)}$			0.7	-	-	μ s
COM	COM variation	Between COM-Nx (including surge)	-5.0	-	5.0	V

Note:

5. IPM may not respond if the input pulse width is less than $PW_{IN(ON)}$, $PW_{IN(OFF)}$.

CF/EN: Controllable Fault Output

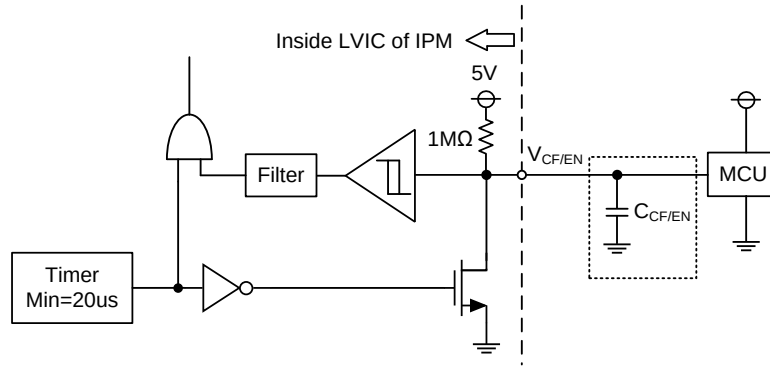


Figure 2. CF/EN Circuit

- (1) CF/EN provides controllable fault output signal duration time and enables MCU to shut down all low-side IGBTs.
- (2) When CF/EN is in the high state, the IPM operates normally, whereas CF/EN is in a low state, the low-side IGBTs are turned off until CF/EN recovers to the high state.
- (3) CF/EN pin provides fixed or adjustable pulse width of fault output signal. No external capacitor generates t_{FO} of minimum 20μsec.

If the external capacitor $C_{CF/EN}$ (1nF) is connected as shown in Figure 2, t_{FO} is adjusted as the following equation;

$$t_{FO} = -\left(1M \cdot C_{CF/EN}\right) \cdot \ln\left(1 - \frac{V_{CF/EN+}}{5V}\right) + 20\mu\text{sec}$$

$$\approx 0.48(1M \cdot C_{CF/EN}) + 20\mu\text{sec}$$

for example, Using $C_{CF/EN}=1\text{nF}$, $t_{FO}\approx 500\mu\text{s}$.

Short-Circuit (SC) Protection and Timing Chart

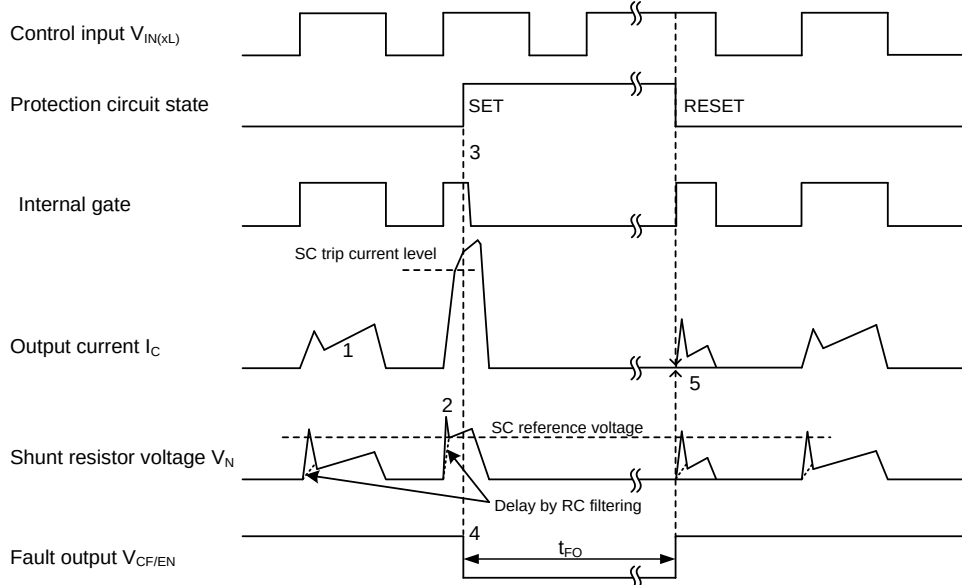


**Figure 3. Short-Circuit Protection
(Low-side Operation Only with External Shunt Resistor and RC Filter)**

- (1) Normal operation: IGBT turns on and output current.
- (2) Short-circuit current is detected when sensed I_C is exceeds $V_{CSC(REF)}$.
- (3) Fault signal ($V_{CF/EN}$) becomes low.
- (4) Accordingly, all low-side IGBTs gate are turned off.
- (5) Fault signal outputs $V_{CF/EN}$ duration time (t_{FO}) is minimum 20μs.
- (6) Fault output finishes Normal operation starts according to the input signal.

VDD Under-voltage Lock-out (UVLO) Protection and Timing Chart

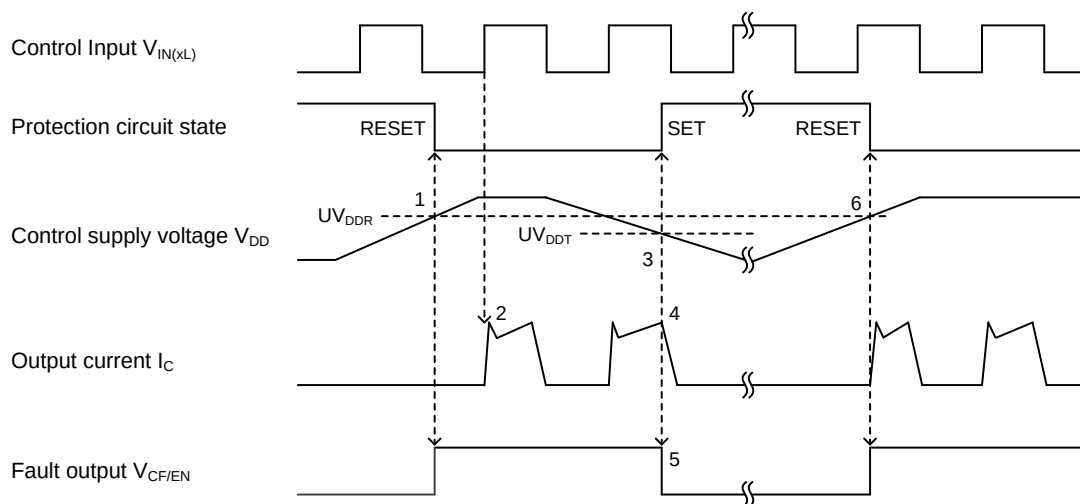


Figure 4. Under-Voltage Protection (Low-side, V_{DD})

- (1) Supply voltage V_{DD} becomes higher than under-voltage reset level (UV_{DDR}), and IGBTs are turned on by the next ON signal.
- (2) Normal operation: IGBTs turn-on and output current.
- (3) V_{DD} level drops to under-voltage trip level (UV_{DDT}).
- (4) All low-side IGBTs are turned off regardless of control input condition.
- (5) CF/EN output is generated, and $V_{CF/EN}$ stays low as long as V_{DD} is below UV_{DDR} .
- (6) V_{DD} level reaches UV_{DDR} . Normal operation starts according to the input signal.

VBS Under-voltage Lock-out (UVLO) Protection and Time Chart

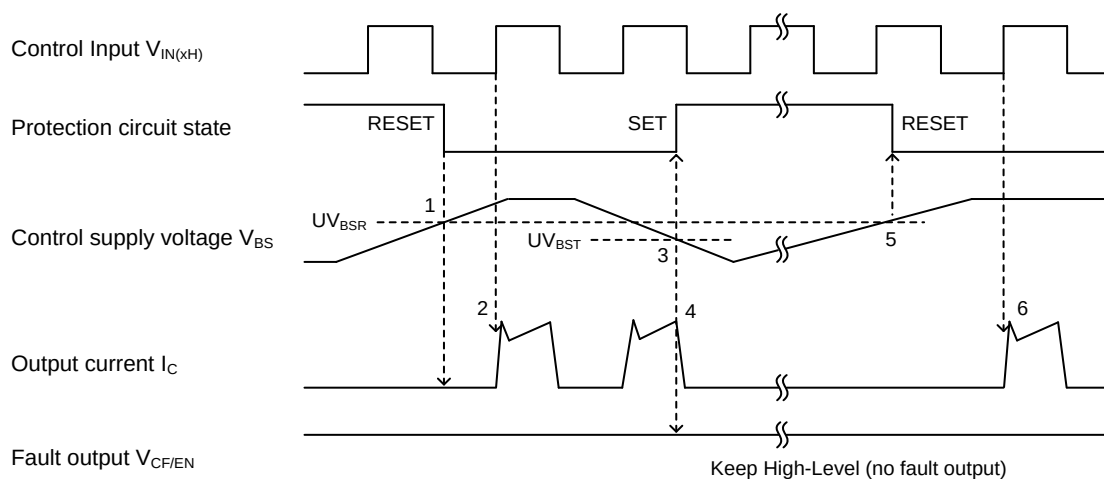


Figure 5. Under-Voltage Protection (High-side, V_{BS})

- (1) Control supply voltage V_{BS} rises. After the voltage reaches under-voltage reset level (UV_{BSR}), IGBTs are turned on by the next ON signal.
- (2) Normal operation: IGBTs turn on and output current.
- (3) V_{BS} level drops to under-voltage trip level (UV_{BST}).
- (4) All high-side IGBTs are turned off regardless of control input condition.
- (5) V_{BS} level reaches UV_{BSR} .
- (6) Normal operation starts according to the input signal.

Over Temperature (OT) Protection and Time Chart

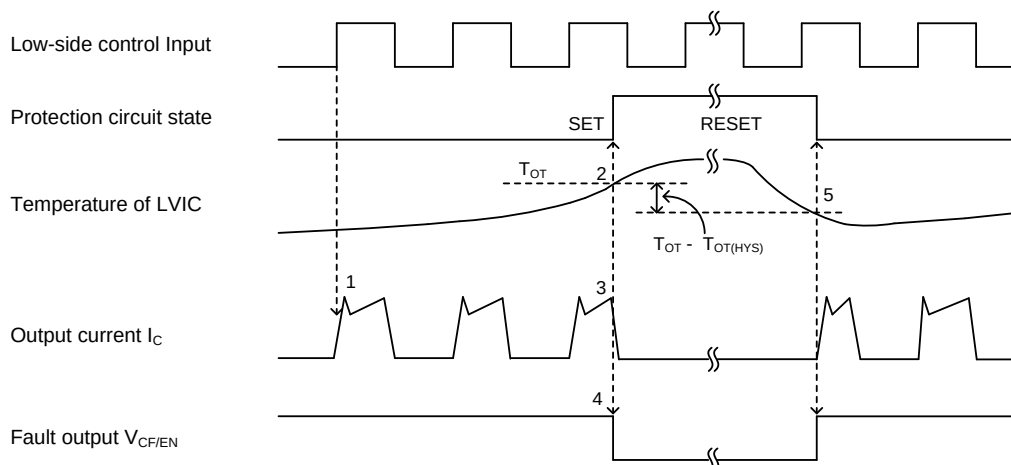


Figure 6. Over-Temperature Protection (Detecting LVIC Temperature)

- (1) Normal operation: IGBTs turn on and output current.
- (2) LVIC temperature exceeds over-temperature trip level (T_{OT}).
- (3) All low-side IGBTs are turned off regardless of control input condition.
- (4) CF/EN output is generated, and $V_{CF/EN}$ stays low as long as LVIC temperature is over T_{OT} .
- (5) LVIC temperature drops to over-temperature reset level ($T_{OT} - T_{OT(HYS)}$). Normal operation starts according to the input signal.

Switching Time Definitions

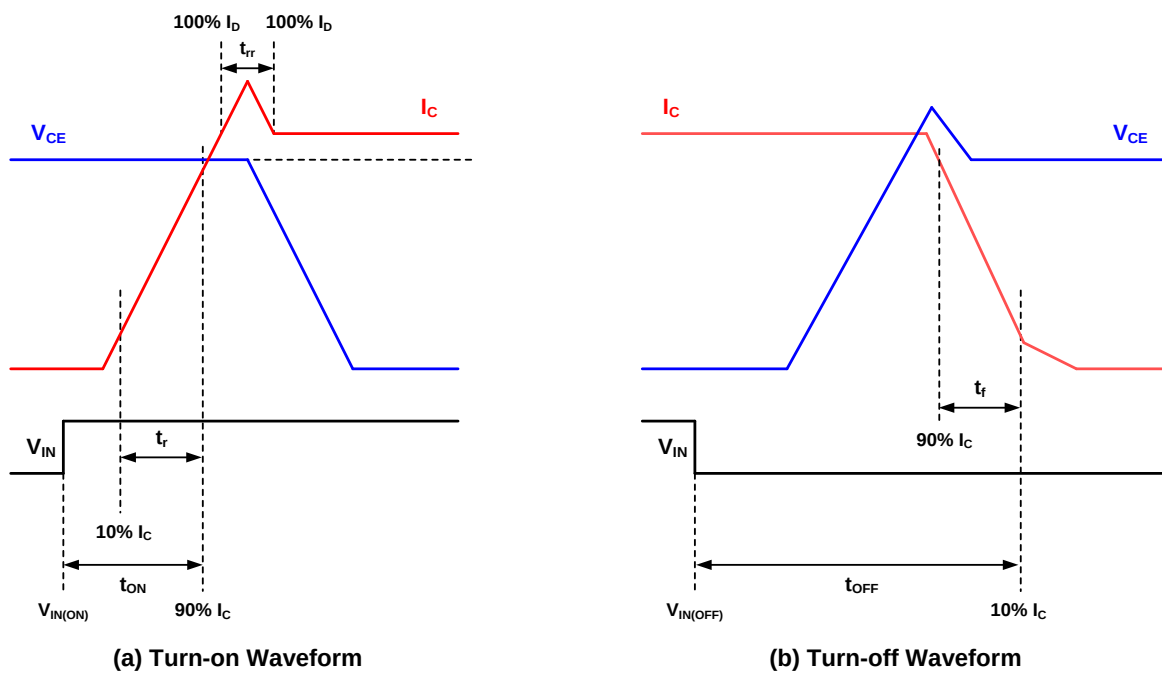
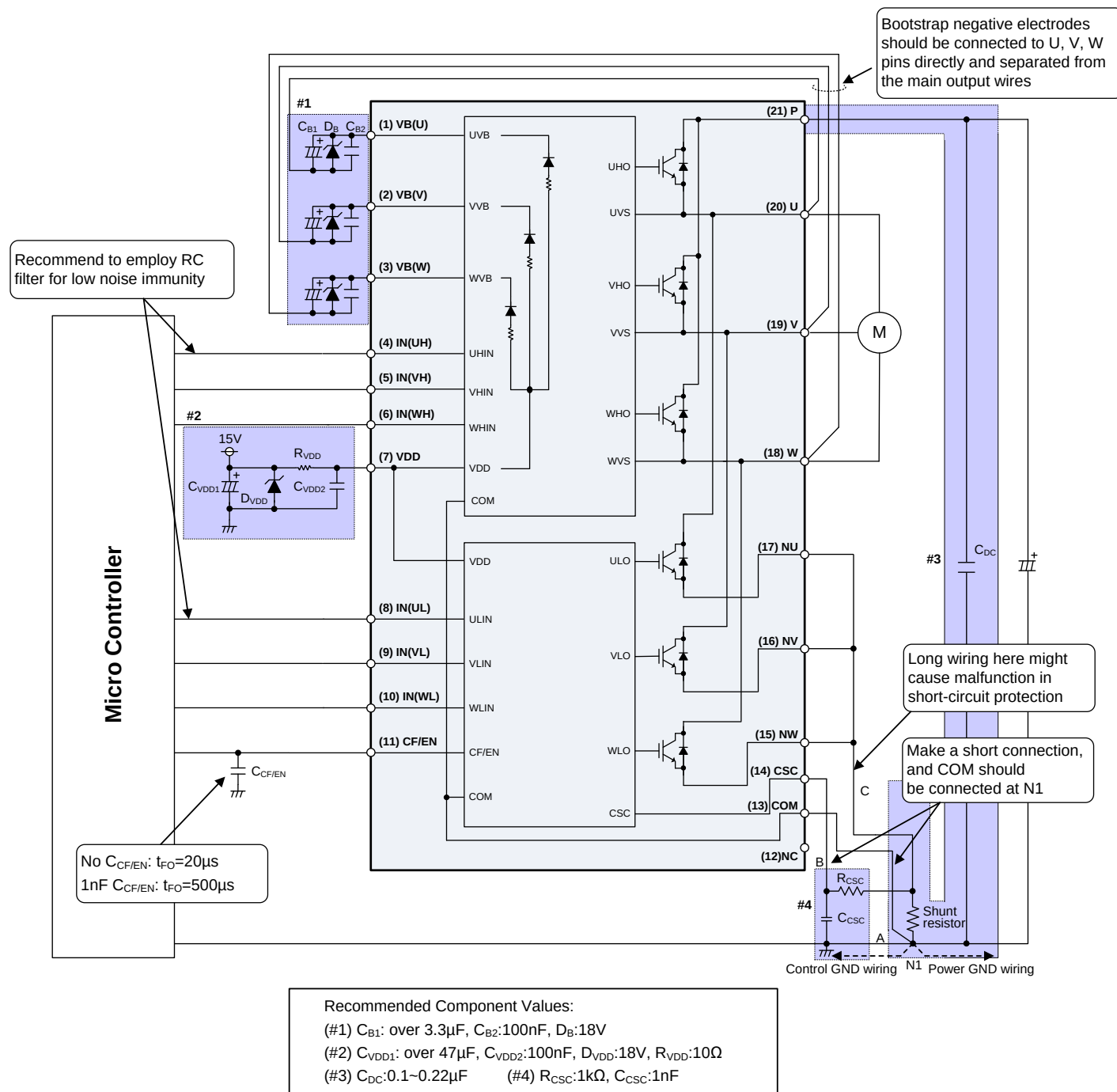


Figure 7. Switching Time Definitions

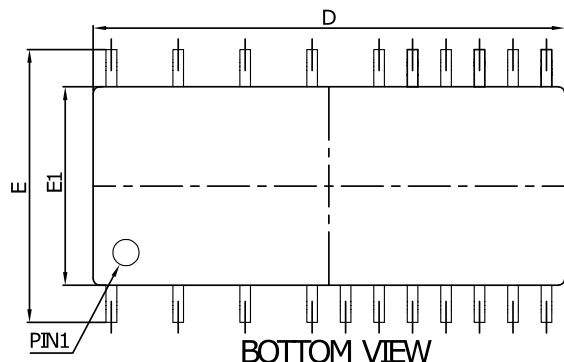
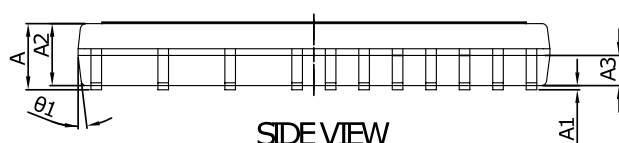
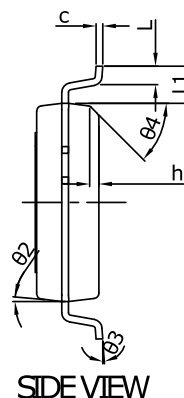
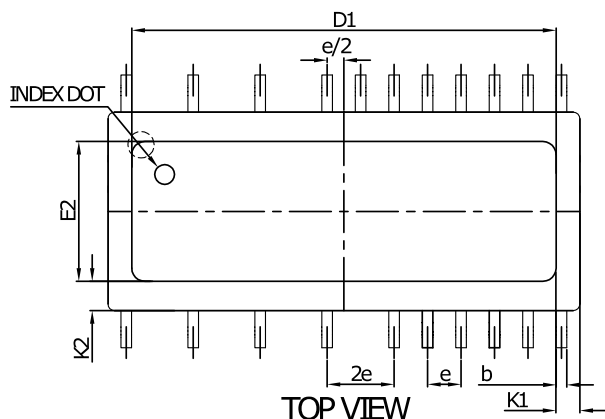
Example of Application Circuit



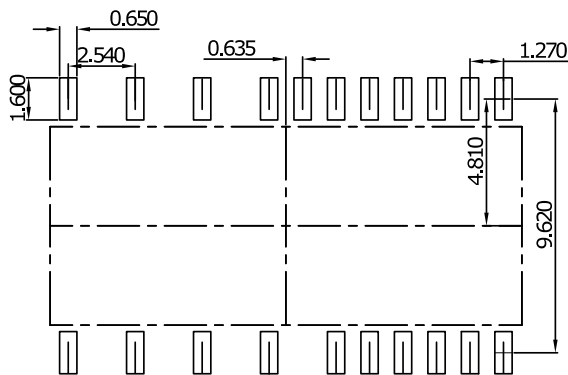
- (1) GND pattern: The star ground design is recommended. GND pattern should be separated from the one point of the shunt resistors. PCB patterns of A, B and C needs to be as short as possible to prevent the noise-caused malfunction.
- (2) Bootstrap and VDD supply capacitors: It is recommended that all capacitors are mounted as close to VB(x) and VDD of the IPM as possible. In addition, it is recommended to use C_{B1} , C_{B2} , C_{VDD1} and C_{VDD2} with good temperature and frequency characteristics.
- (3) A zener diode D_B and D_{VDD} (18V/1W) are recommended between each pair of control supply pins to avoid damage by external surges. Additionally, it is recommended to add the resistance R_{VDD} (10 Ω) to the VDD in series to prevent damage cause by external surges.
- (4) Snubber capacitor: Prevention of surge destruction can further be improved by placing the bus capacitor C_{DC} as close to pin P and N1 as possible.

- (5) CSC circuit: Switching noise filter of R_{CSC} and C_{CSC} should be placed as close to CSC pin and COM(13) pin as possible to prevent protection function errors. It is recommended to use R_{CSC} and C_{CSC} with low tolerance and temperature-compensated type. Time constant of the filter can be determined considering switching frequency, which is selected within typically $1\mu s$ in general motor drives.
- (6) Input circuit: The R_{IN} and C_{IN} filter circuit is recommended to place as close to IPM as possible to reduce input signal noise by switching operation. Typically, they are recommended 100Ω and $1nF$, respectively.
- (7) CF/EN circuit: $C_{CF/EN}$ can adjust fault output pulse duration time t_{FO} . Without $C_{CF/EN}$, t_{FO} has fixed $20\mu s$ (min.) pulse width. For the design guide, please refer to the Figure 2.

Package Dimensions, IPM-7DA



LAND PATTERN RECOMMENDATIONS



SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.304	2.504	2.704	0.091	0.099	0.106
A1	0.050	0.150	0.250	0.002	0.006	0.010
A2	2.254	2.354	2.454	0.089	0.093	0.097
A3	1.050	1.150	1.250	0.041	0.045	0.049
D	17.800	17.900	18.000	0.701	0.705	0.709
D1	15.800	16.100	16.200	0.622	0.634	0.638
E	10.140	10.340	10.540	0.399	0.407	0.415
E1	7.420	7.520	7.620	0.292	0.296	0.300
E2	5.000	5.300	5.400	0.197	0.209	0.213
L	0.505	0.705	0.905	0.020	0.028	0.036
L1	1.210	1.410	1.610	0.048	0.056	0.063
K1	0.700	0.900	1.100	0.028	0.035	0.043
K2	0.910	1.110	1.310	0.036	0.044	0.052
e	1.270TYP.			0.050TYP.		
b	0.410TYP.			0.016TYP.		
c	0.254TYP.			0.010TYP.		
θ1	7°TYP.			7°TYP.		
θ2	7°TYP.			7°TYP.		
θ3	0°	—	8°	0°	—	8°
θ4	45°TYP.			45°TYP.		
h	0.381TYP.			0.015TYP.		

UNIT: mm

NOTES

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.