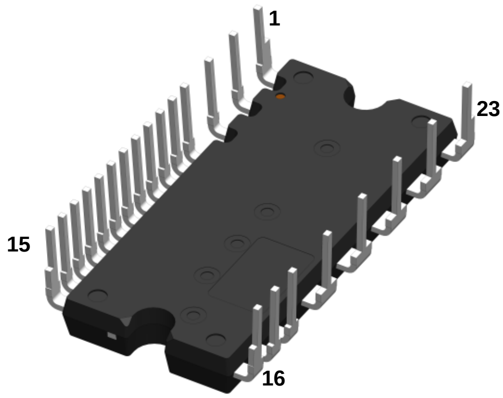
AIP5N10K060Q4(S/U)

External View



Size: 33.4 x 15 x 3.6 mm

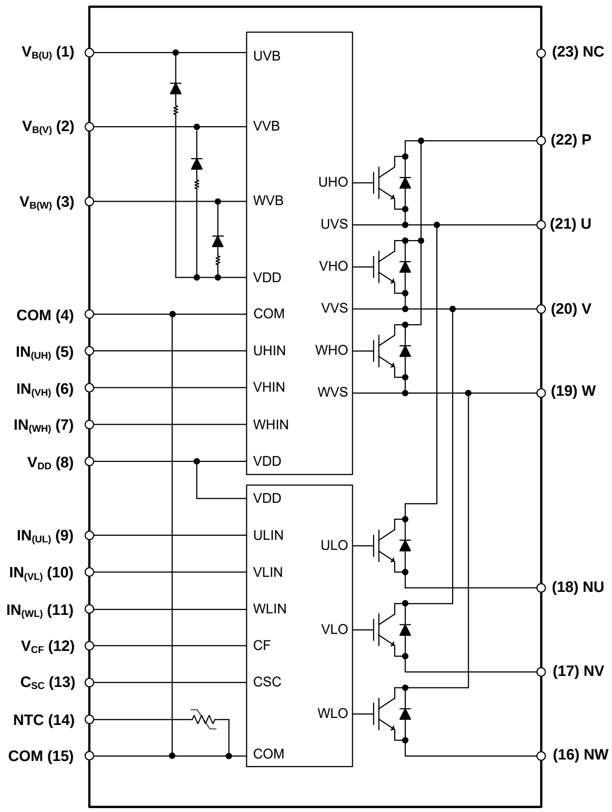
Features

- UL Recognized: UL1557 File E345245
- 600V-10A (Trench Shielded Planar Gate IGBT)
- 3 phase Inverter module including HVIC drivers
- Built-in bootstrap diodes with integrated current-limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Over-temperature (OT) protection
- Temperature monitoring (NTC)
- Short-circuit current protection (C_{SC})
- Controllable fault out signal (V_{CF}) corresponding to SC, UV and OT fault
- Wide input interface (3-18V), Schmitt trigger receiver circuit (Active High)
- Isolation ratings of 2000Vrms/min

Applications

- AC 100-240Vrms class low power motor drives
- Washing machines, Compressors, Fan Motors, Refrigerators, Dishwashers and Air-conditioners

Internal Equivalent Circuit / Pin Configuration



Ordering Information

Part Number	Temperature Range	Package	Pin Length Description
AIP5N10K060Q4	-40°C to 150°C	IPM-5	Normal
AIP5N10K060Q4S	-40°C to 150°C	IPM-5A	Short
AIP5N10K060Q4U	-40°C to 150°C	IPM-5C	Ultra Short

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Description

Pin Number	Pin Name	Pin Function
1	$V_{B(U)}$	High-Side Bias Voltage for U-Phase IGBT Driving
2	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
3	$V_{B(W)}$	High-Side Bias Voltage for W-Phase IGBT Driving
4	COM	Common Supply Ground
5	$IN_{(UH)}$	Signal Input for High-Side U-Phase
6	$IN_{(VH)}$	Signal Input for High-Side V-Phase
7	$IN_{(WH)}$	Signal Input for High-Side W-Phase
8	V_{DD}	Common Bias Voltage for IC and IGBTs Driving
9	$IN_{(UL)}$	Signal Input for Low-Side U-Phase
10	$IN_{(VL)}$	Signal Input for Low-Side V-Phase
11	$IN_{(WL)}$	Signal Input for Low-Side W-Phase
12	V_{CF}	Controllable Fault Output
13	C_{SC}	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
14	NTC	Thermistor (Temperature Monitoring)
15	COM	Common Supply Ground
16	NW	Negative DC-Link Input for W-Phase
17	NV	Negative DC-Link Input for V-Phase
18	NU	Negative DC-Link Input for U-Phase
19	W	Output for W-Phase
20	V	Output for V-Phase
21	U	Output for U-Phase
22	P	Positive DC-Link Input
23	NC	No Connection

Absolute Maximum Ratings

T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Ratings	Units
Inverter				
V_{PN}	Supply Voltage	Applied between P - NU,NV,NW	450	V
$V_{PN(surge)}$	Supply Voltage (surge)	Applied between P - NU,NV,NW	500	V
V_{CES}	Collector-Emitter Voltage		600	V
I_C	Output Phase Current	T_C=25°C, T_J<150°C	10	A
		T_C=100°C, T_J<150°C	5	A
$\pm I_{PK}$	Output Peak Phase Current	T_C=25°C, less than 1ms pulse width	15	A
t_{SC}	Short Circuit Withstand Time (오류! 참조 원본을 찾을 수 없습니다.)		5	μs
P_C	Collector Dissipation	T_C=25°C, per chip	23	W
T_J	Operating Junction Temperature		-40 to 150	℃
Control (Protection)				
V_{DD}	Control Supply Voltage	Applied between V_{DD}-COM	25	V
V_{DB}	High-Side Control Bias Voltage	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	25	V
V_{IN}	Input Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ – COM	-0.5 ~ V_{DD}+0.5	V
V_{CF}	Fault Output Supply Voltage	Applied between V_{CF}-COM	-0.5 ~ 5.5	V
I_{CF}	Fault Output Current	Sink current at V_{CF} terminal	1	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC}-COM	-0.5 ~ 5.5	V
Total System				
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	V_{DD}=13.5-16.5V, Inverter part T_J=150°C, Non-repetitive, less than 2μs	400	V
T_C	Module Case Operation Temperature	Measurement point of T_C is provided in Figure 1	-30 to 125	℃
T_{STG}	Storage Temperature		-40 to 150	℃
V_{ISO}	Isolation Voltage	60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate	2000	V_{rms}

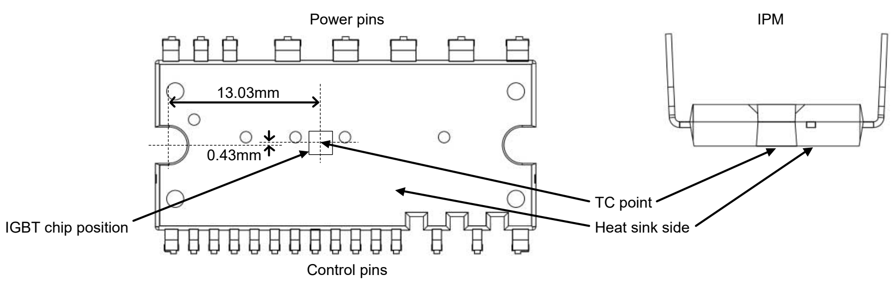


Figure 1. T_C Measurement Point

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (1)	Inverter IGBT (per 1/6 module)	-	-	5.4	K/W
$R_{th(j-c)F}$		Inverter FWD (per 1/6 module)	-	-	6.9	K/W

Note:

1. For the measurement point of case temperature (T_C), please refer to Figure 1.

Electrical Characteristics

T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Inverter							
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	$V_{DD}=V_{DB}$=15V, V_{IN}=5V	I_C=5A, T_J=25°C	-	1.60	2.00	V
			I_C=5A, T_J=125°C	-	1.90	-	V
V_F	FWD Forward Voltage	V_{IN}=0	I_F=5A, T_J=25°C	-	1.35	1.80	V
t_{ON}	Switching Times	V_{PN}=300V, $V_{DD}=V_{DB}$=15V I_C=5A, T_J=25°C, V_{IN}=0V ↔ 5V Inductive load (high-side)		0.30	0.60	1.10	μs
$t_{C(ON)}$				-	0.10	0.40	μs
t_{OFF}				-	1.00	1.50	μs
$t_{C(OFF)}$				-	0.10	0.30	μs
t_{rr}				-	0.10	-	μs
I_{CES}	Collector-Emitter Leakage Current	$V_{CE}=V_{CES}$	T_J=25°C	-	-	1	mA
			T_J=125°C	-	-	10	mA
Control (Protection)							
I_{QDD}	Quiescent V_{DD} Supply Current	V_{DD}=15V, $IN_{(UH,VH,WH,UL,VL,WL)}$=0V	V_{DD}-COM	-	-	2.1	mA
I_{QDB}	Quiescent V_{DB} Supply Current	V_{DB}=15V, $IN_{(UH, VH, WH)}$=0V	$V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	-	-	0.3	mA
$V_{SC(ref)}$	Short-Circuit Trip Level	V_{DD}=15V (2)		0.45	0.48	0.51	V
UV_{DT}	Supply Circuit Under-Voltage Protection	Trip Level		10.3	11.4	12.5	V
UV_{DR}		Reset Level		10.8	11.9	13.0	V
UV_{DBT}		Trip Level		8.5	9.5	10.5	V
UV_{DBR}		Reset Level		9.5	10.5	11.5	V
OT_T	Over-Temperature Protection (3)	V_{DD}=15V, Detect LVIC Temperature	Trip Level	110	130	150	℃
OT_{HYS}			Hysteresis of Trip Reset	-	30	-	℃
V_{CFH}	Fault Output Voltage	V_{SC}=0V, V_{CF} Circuit: 10kΩ to 5V pull-up		4.9	-	-	V
V_{CFL}		V_{SC}=1V, V_{CF} Circuit: 10kΩ to 5V pull-up		-	-	0.5	V
V_{CF+}	CF positive going threshold			-	1.9	2.2	V
V_{CF-}	CF negative going threshold			0.8	1.1	-	V
t_{FO}	Fault Output Pulse Width (4)			20	-	-	μs
I_{IN}	Input Current	V_{IN}=5V		-	1.0	-	mA
$V_{th(on)}$	ON Threshold Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM			2.3	2.6	V
$V_{th(off)}$	OFF Threshold Voltage			0.8	1.2		V
$V_{th(hys)}$	ON/OFF Threshold Hysteresis Voltage			-	1.1	-	V
$V_{F(BSD)}$	Bootstrap Diode Forward Voltage	I_F=10mA Including Voltage Drop by Limiting Resistor (5)		0.5	1.0	1.5	V
R_{BSD}	Built-in Limiting Resistance	Included in Bootstrap Diode		80	100	120	Ω

Notes:

2. Short-circuit protection works only for low sides.
3. When the LVIC temperature exceeds OT Trip temperature level (OT_T), OT protection is triggered and fault outputs.
4. Fault signal (F_O) outputs when SC, UV or OT protection is triggered. F_O pulse width is different for each protection mode. At SC failure, F_O pulse width is a fixed width (minimum 20μs), but at UV or OT failure, F_O outputs continuously until recovering from UV or OT state. (But minimum F_O pulse width is 20μs).
5. The characteristics of bootstrap diodes are described in Figure 2.

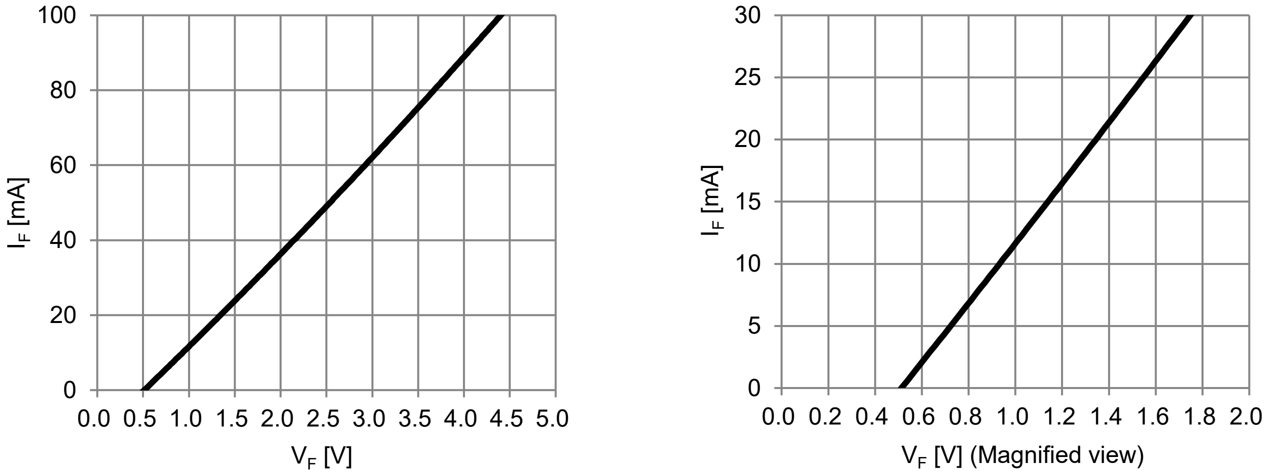


Figure 2. Built-in Bootstrap Diode V_F-I_F Characteristic (@T_A=25°C)

NTC Thermistor

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{25}	Resistance	T_{NTC}=25°C	-	84.83	-	kΩ
B(25/100)	C-constant		-	4092	-	K

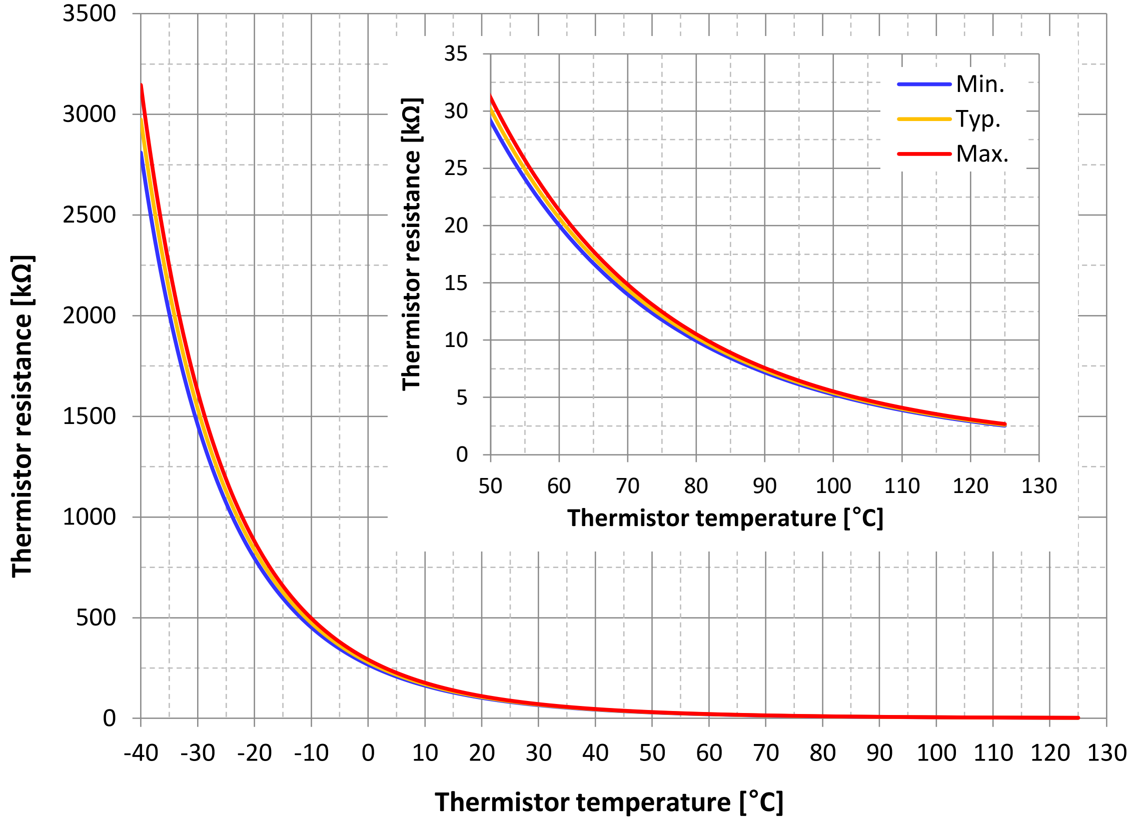


Figure 3. Thermistor Resistance vs. Temperature Curve

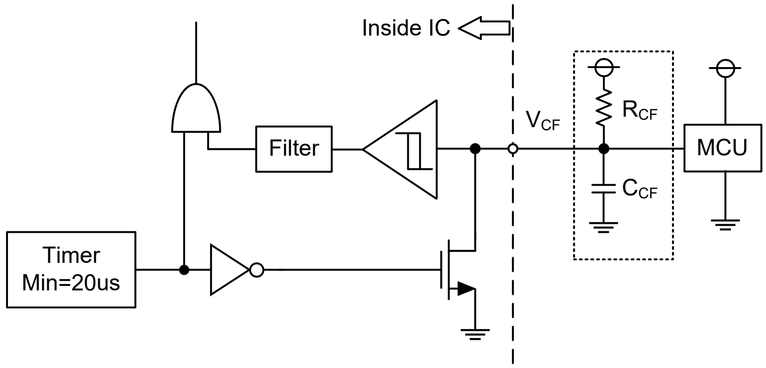


Figure 4. V_{CF} Output Circuit

(1) The V_{CF} pin provides an enable functionality that allows it to shut down the all low-side IGBTs. When the V_{CF} pin is in the high state the IPM is able to operate normally. If the V_{CF} pin is in a low state, the low-side IGBTs are turned off until the enable condition is restored. In addition, the V_{CF} pin can provide the fault output signal with the fixed or controlled fault out pulse width.

(2) If only a pull-up resistor of 10kΩ connected to the V_{CF} pin, the fault output pulse width is fixed at minimum 20us.

(3) If a capacitor is connected with a pull-up resistor together, the fault output pulse width can be controlled according to the resistor and the capacitor values. The length of fault output pulse width is determined by the following formula ;

- t_{FO} = -(R_{CF}*C_{CF})*ln(1-V_{CF+}/V_{DD}) + 20us(min.)
- ex) V_{DD}=5V, R_{CF}=2.2MΩ, C_{CF}=1nF, t_{FO}≈1.07ms. Recommended parameters in the design are C_{CF} of ≤ 1nF and R_{CF} of 0.1M to 2.2MΩ.

Mechanical Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Mounting Torque	Mounting Screw: M3 [6]		0.59	0.69	0.78	N m
Weight			-	5.25	-	g
Flatness	Refer to Figure 5		-50	-	100	μm

Note:

6. Plain washers (ISO 7089-7094) are recommended.

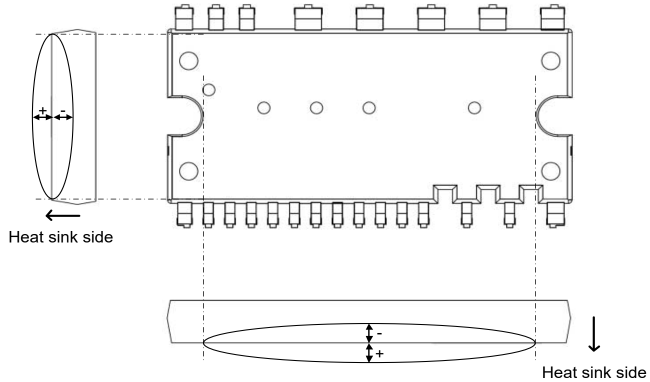


Figure 5. Flatness Measurement Positions

Recommended Operation Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PN}	Supply Voltage	Applied between P-NU, NV, NW	0	300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DD}-COM	13.5	15.0	16.5	V
V_{DB}	High-Side Bias Voltage	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	13.5	15.0	18.5	V
dV_{DD}/dt, dV_{DB}/dt	Control Supply Variation		-1	-	1	V/μs
t_{dead}	Arm Shoot-Through Blocking Time	For each input signal	1.0	-	-	μs
f_{PWM}	PWM Input Frequency	-40°C < T_J < 150°C	-	-	20	kHz
$PW_{IN(ON)}$	Minimum Input Pulse Width [7]		0.5	-	-	μs
$PW_{IN(OFF)}$			0.5	-	-	μs
COM	COM Variation	Between COM-NU, NV, NW (including surge)	-5.0	-	5.0	V

Note:

7. IPM may not respond if the input pulse width is less than $PW_{IN(ON)}$, $PW_{IN(OFF)}$.

Time Charts of the IPM Protective Function

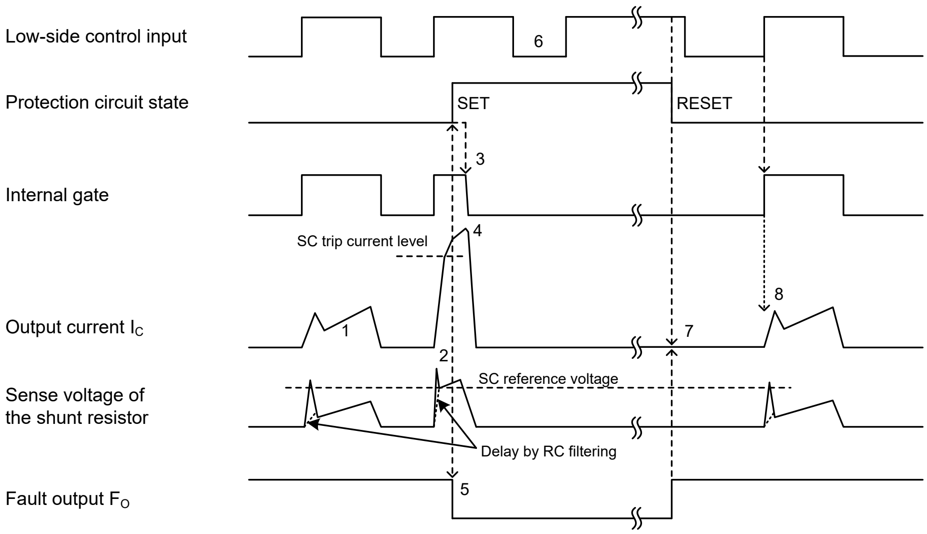


Figure 6. Short-Circuit Protection
(Low-side Operation Only with the External Shunt Resistor and RC Filter)

(1) Normal operation: IGBT turns on and outputs current.
(2) Short-circuit current detection (SC triggered).
(3) All low-side IGBTs' gates are hard interrupted.
(4) All low-side IGBTs turn OFF.
(5) F_O output time (t_{FO})=minimum 20μs.
(6) Input = "L" : IGBT OFF.
(7) Fault output finishes, but output current will not turn on until next ON signal (L→H).
(8) Normal operation: IGBT turns on and outputs current.

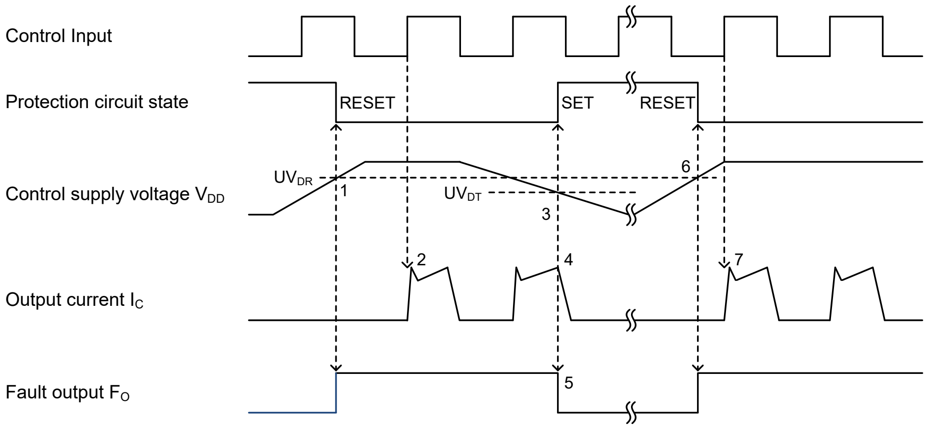


Figure 7. Under-Voltage Protection (Low-side, UV_D)

(1) Control supply voltage V_{DD} exceeds under voltage reset level (UV_{DR}), but IGBT turns on by next ON signal (L→H).
(2) Normal operation: IGBT turns on and outputs current.
(3) V_{DD} level drops to under voltage trip level (UV_{DT}).
(4) All low-side IGBTs turn OFF regardless of control input condition.
(5) F_O output time (t_{FO})=minimum 20μs, and F_O stays low as long as V_{DD} is below UV_{DR}.
(6) V_{DD} level reaches UV_{DR}.
(7) Normal operation: IGBT turns on and outputs current.

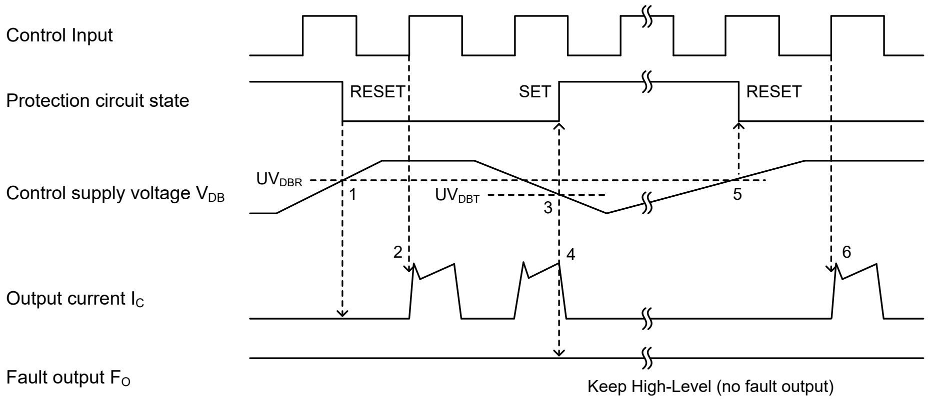


Figure 8. Under-Voltage Protection (High-side, UV_{DB})

(1) Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBR}, IGBT turns on by next ON signal (L→H).
(2) Normal operation: IGBT turns on and outputs current.
(3) V_{DB} level drops to under voltage trip level (UV_{DBT}).
(4) All high-side IGBTs turn OFF regardless of control input condition, but there is no F_O signal output.
(5) V_{DB} level reaches UV_{DBR}.
(6) Normal operation: IGBT turns on and outputs current.

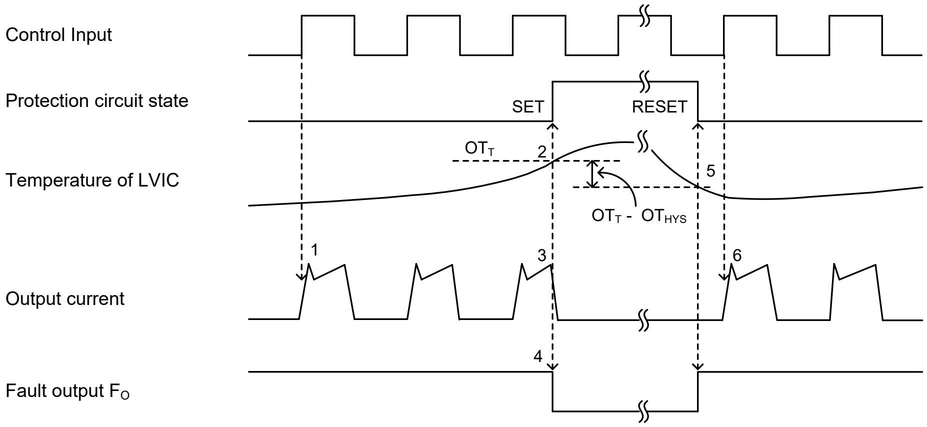
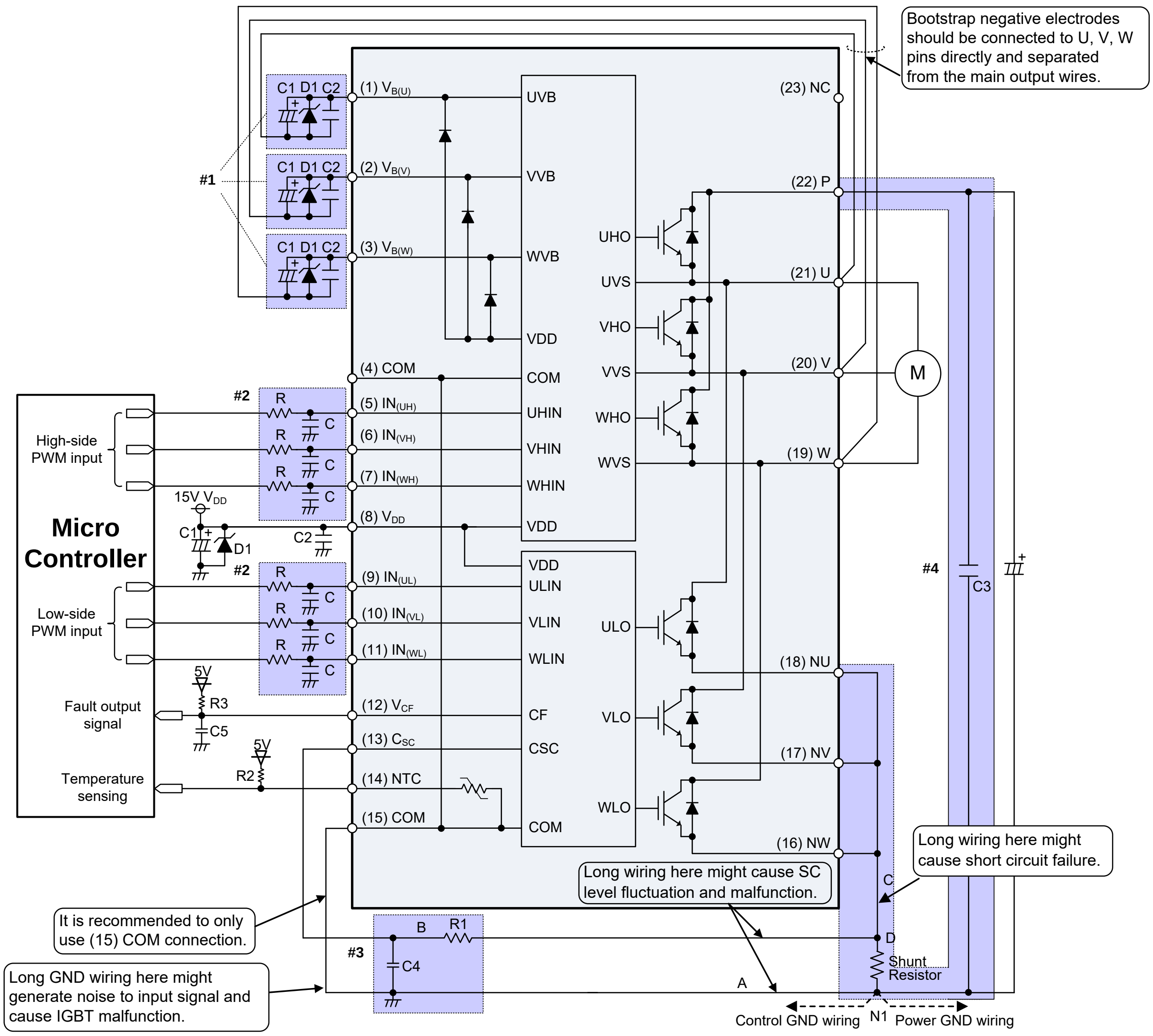


Figure 9. Over-Temperature Protection (Low-side, Detecting LVIC Temperature)

(1) Normal operation: IGBT turns on and outputs current.
(2) LVIC temperature exceeds over-temperature trip level (OT_T).
(3) All low-side IGBTs turn off regardless of control input condition.
(4) F_O output time (t_{FO})=minimum 20μs, and F_O stays low as long as LVIC temperature is over OT_T.
(5) LVIC temperature drops to over-temperature reset level (OT_T-OT_{HYS}).
(6) Normal operation: IGBT turns on by the next ON signal (L→H).

Example of Application Circuit



Recommended Component Values:

(#1) C1:over 10µF, C2:100nF, D1:24V	(#2) R:100Ω, C:1nF
(#3) R1:1kΩ, C4:2nF	(#4) C3:0.1~0.22µF

(1) If the control GND is connected with the power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect the control GND and power GND at a single point (N1), near the terminal of the shunt resistor.

(2) There are two COM pins in the IPM but it is recommended to only use the (15) COM pin to minimize SC detection noise.

(3) A zener diode D1 (24V/1W) is recommended between each pair of control supply pins to prevent surge destruction.

(4) Prevention of surge destruction can further be improved by placing the bus capacitor as close to pin P and N1 as possible. Generally a 0.1-0.22µF snubber capacitor C3 between the P-N1 terminals is recommended.

(5) Selection of the R1*C4 filter components for short-circuit protection is recommended to have tight tolerance, and is temperature-compensated type. The R1*C4 time constant should be set such that SC current is shut down within 2µs; (typically 1.5-2µs). R1 and C4 should be placed as close as possible to the C_{SC} pin. SC interrupting time may vary with layout patterns and components selection, therefore thorough evaluation in the system is necessary.

(6) NTC signal line should be pull up to the positive side of the 5V/3.3V logic power supply with a proper resistor R2.

(7) To prevent malfunction, traces A, B, and C should be as short as possible.

(8) It is recommended that all capacitors are mounted as close to the IPM as possible. (C1: electrolytic type with good temperature and frequency characteristics. C2: ceramic type with 0.1-2µF, good temperature, frequency and DC bias characteristics.)

(9) Input drives are active-high. There is a minimum 3.5kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the layout to each input should be as short as possible. When using RC coupling circuit, make sure the input signal levels meet the required turn-on and turn-off threshold voltages.

(10) V_{CF} output is open drain type. It should be pulled up to MCU or control power supply (max= 5±0.5V), limiting the current (I_{CF}) to no more than 1mA. I_{CF} is estimated roughly by the formula of control power supply voltage divided by the pull-up resistor R3. For example, if control supply is 5V, a 10kΩ (over 5kΩ) pull-up resistor R3 is recommended.

(11) If only a pull-up resistor R3 of 10kΩ connected to V_{CF} pin, the fault output pulse width is fixed at minimum 20us. If a capacitor C6 is connected with a pull-up resistor R3, the fault output pulse width can be controlled according to the resistor value and capacitor value. For the design guide, please refer to the Figure 4.

(12) Direct drive of the IPM from the MCU is possible without having to use opto-coupler or isolation transformer.

(13) The IPM may malfunction and erroneous operations may occur if high frequency noise is superimposed to the supply line. To avoid such problems, line ripple voltage is recommended to have dV/dt ≤ ±1V/µs, and Vripple ≤ 2Vp-p.

(14) It is not recommended to use the IPM to drive the same load in parallel with another IPM or inverter types.

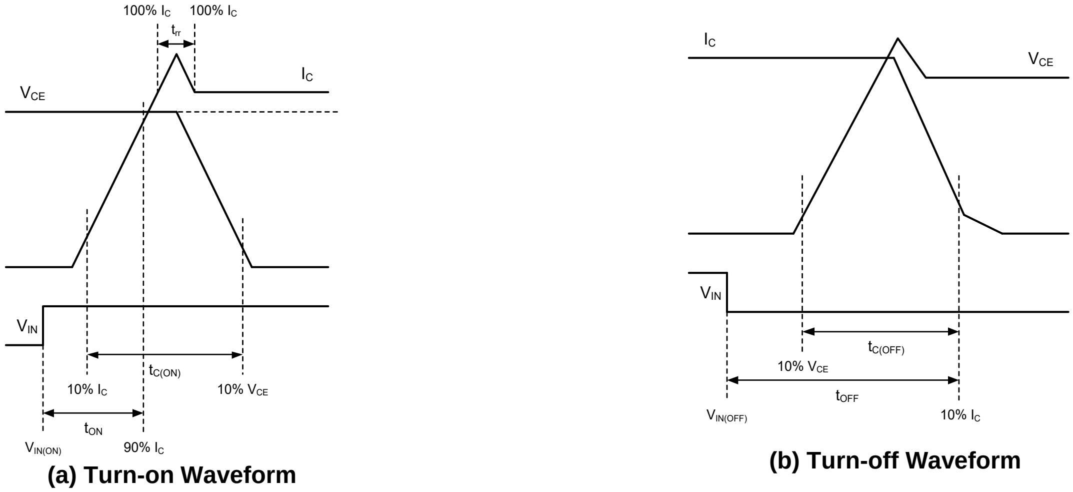
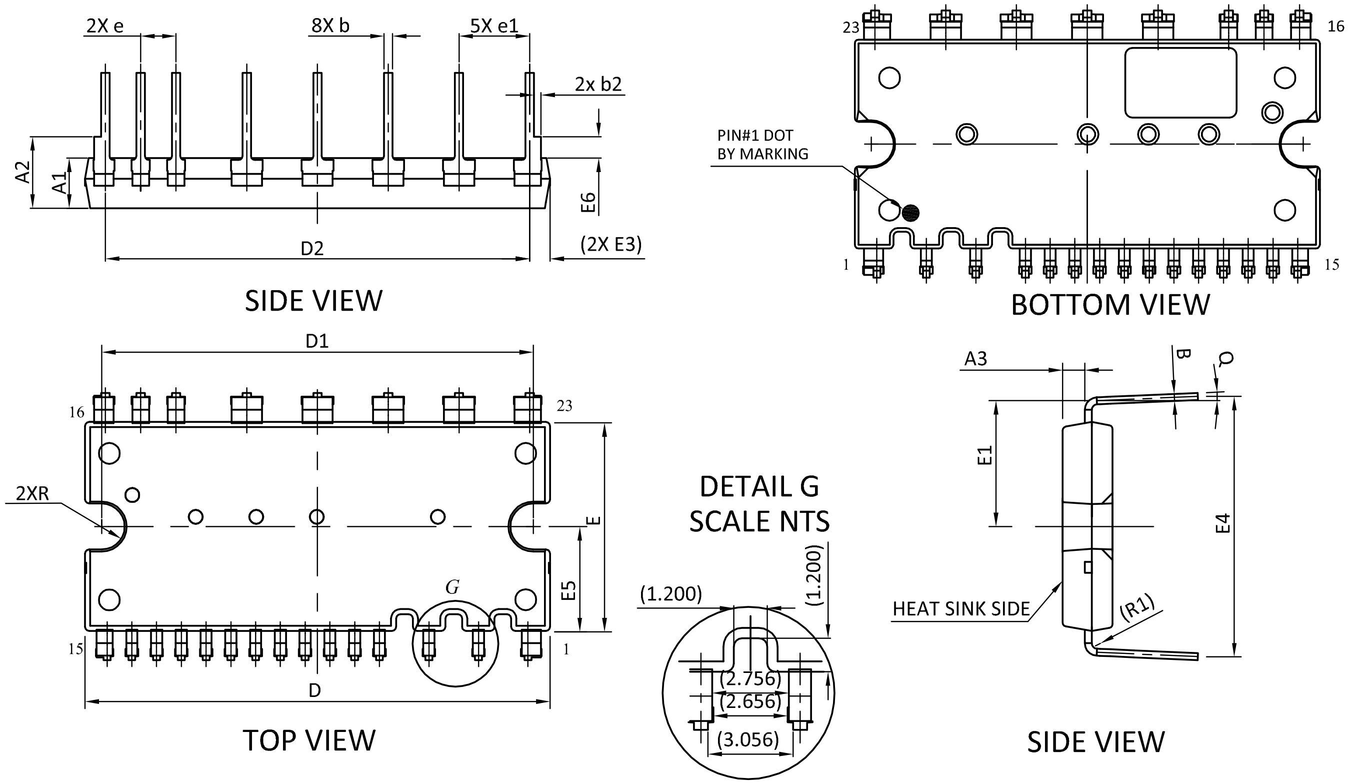
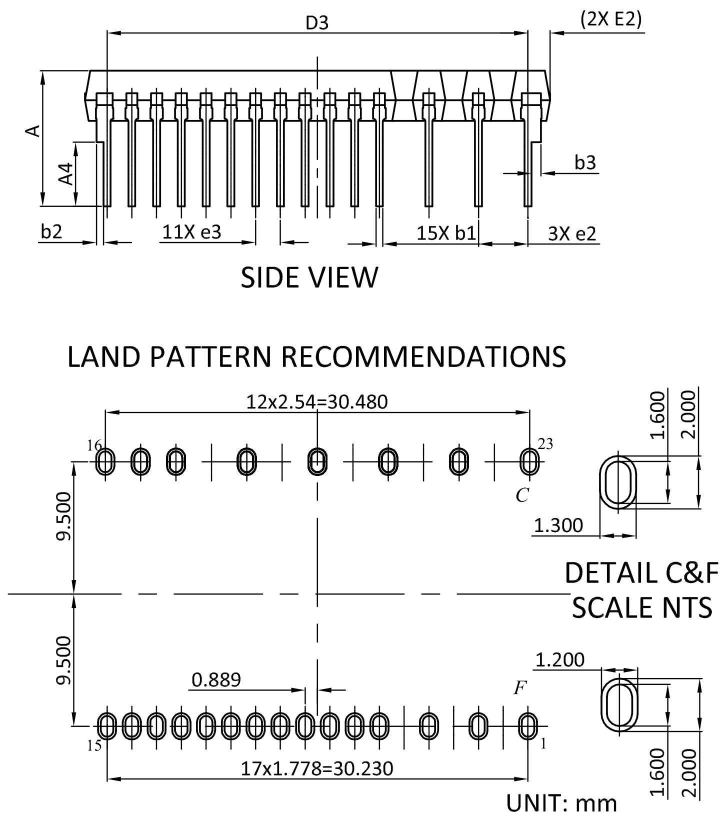


Figure 10. Switching Times Definition

Package Dimensions, IPM-5

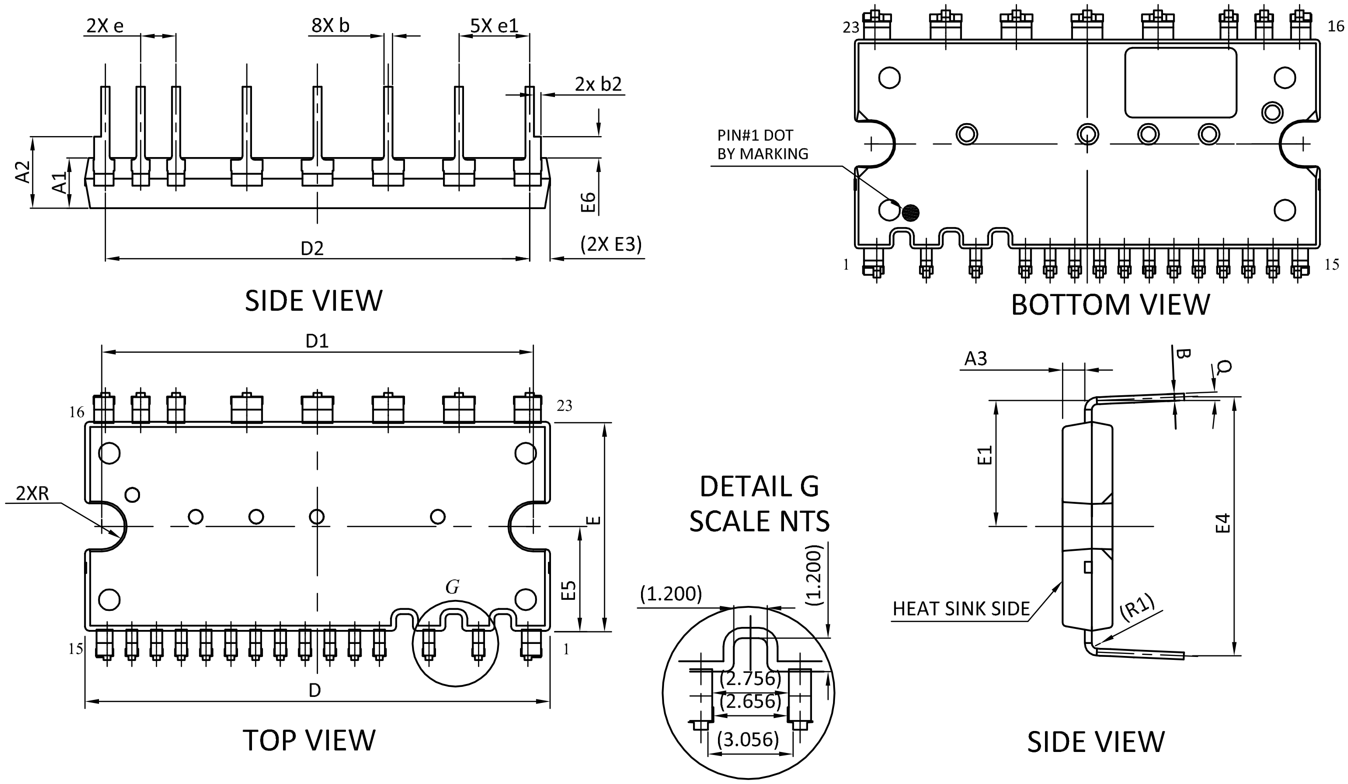


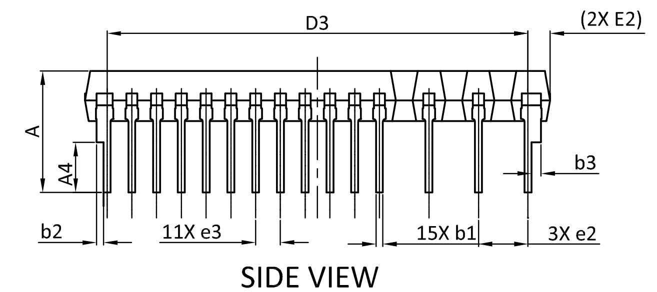


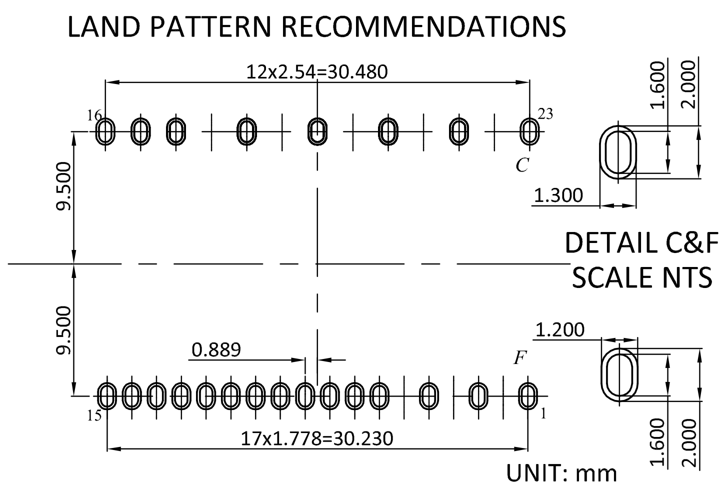
SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	9.300	9.700	10.100	0.366	0.382	0.398
A1	3.300	3.600	3.900	0.130	0.142	0.154
A2	4.700	5.100	5.500	0.185	0.201	0.217
A3	1.500	1.600	1.700	0.059	0.063	0.067
A4	4.200	4.600	5.000	0.165	0.181	0.197
B	0.400	0.500	0.600	0.016	0.020	0.024
b	0.500	0.600	0.700	0.020	0.024	0.028
b1	0.400	0.500	0.600	0.016	0.020	0.024
b2	0.400	0.500	0.600	0.016	0.020	0.024
b3	0.600	0.700	0.800	0.024	0.028	0.031
D	33.100	33.400	33.700	1.303	1.315	1.327
D1	30.800	31.000	31.200	1.213	1.220	1.228
D2	30.180	30.480	30.780	1.188	1.200	1.212
D3	29.930	30.230	30.530	1.178	1.190	1.202
E	14.700	15.000	15.300	0.579	0.591	0.602
E1	8.600	9.000	9.400	0.339	0.354	0.370
E2		1.600REF			0.063REF	
E3		1.500REF			0.059REF	
E4	18.300	18.700	19.100	0.720	0.736	0.752
E5	7.300	7.500	7.700	0.287	0.295	0.303
E6	1.100	1.500	1.900	0.043	0.059	0.075
e	2.340	2.540	2.740	0.092	0.100	0.108
e1	4.880	5.080	5.280	0.192	0.200	0.208
e2	3.356	3.556	3.756	0.132	0.140	0.148
e3	1.578	1.778	1.978	0.062	0.070	0.078
R	1.500	1.600	1.700	0.059	0.063	0.067
R1		0.400REF			0.016REF	
Q		2° - 6°			2° - 6°	

NOTES
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
4. ( ) IS REFERENCE.

Package Dimensions, IPM-5A



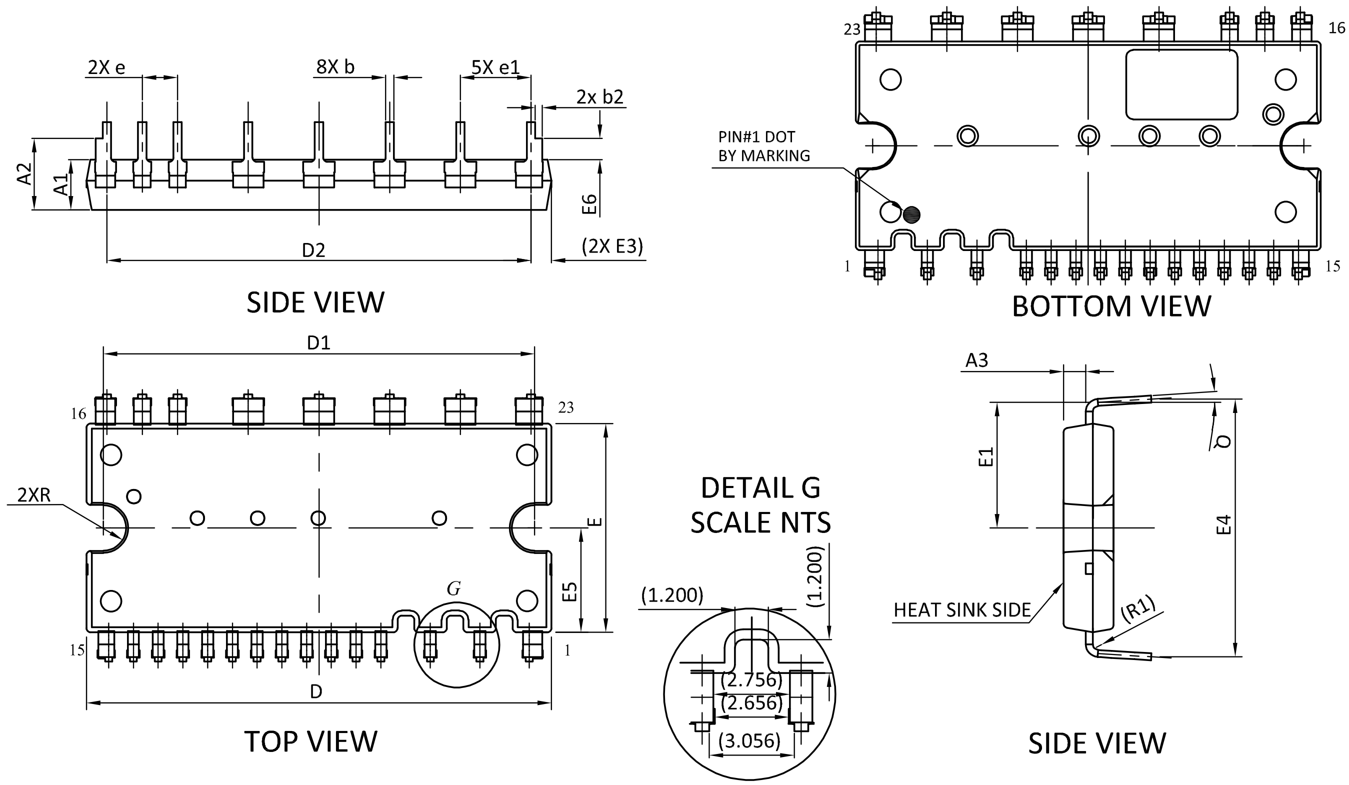


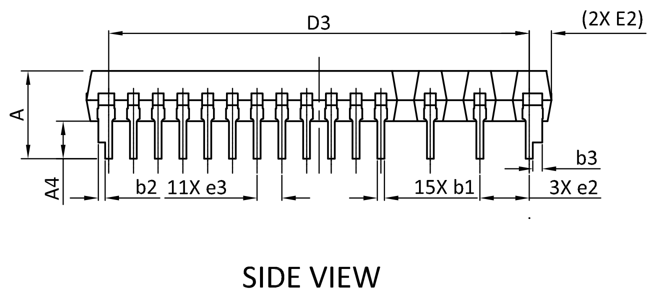


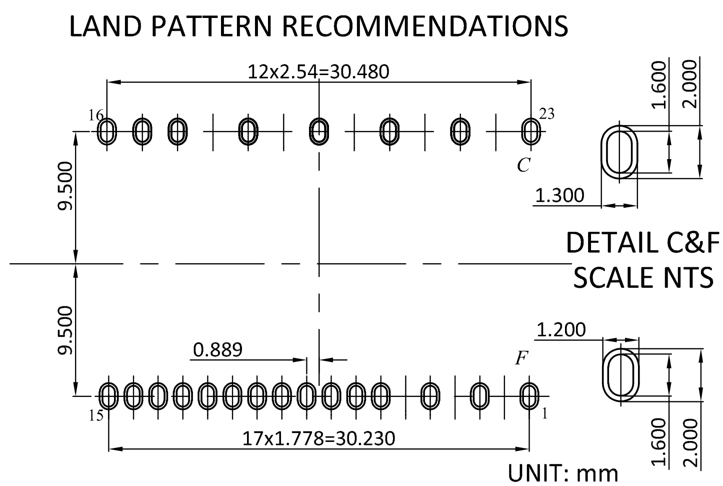
SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	8.300	8.700	9.100	0.327	0.343	0.358
A1	3.300	3.600	3.900	0.130	0.142	0.154
A2	4.700	5.100	5.500	0.185	0.201	0.217
A3	1.500	1.600	1.700	0.059	0.063	0.067
A4	3.200	3.600	4.000	0.126	0.142	0.157
B	0.400	0.500	0.600	0.016	0.020	0.024
b	0.500	0.600	0.700	0.020	0.024	0.028
b1	0.400	0.500	0.600	0.016	0.020	0.024
b2	0.400	0.500	0.600	0.016	0.020	0.024
b3	0.600	0.700	0.800	0.024	0.028	0.031
D	33.100	33.400	33.700	1.303	1.315	1.327
D1	30.800	31.000	31.200	1.213	1.220	1.228
D2	30.180	30.480	30.780	1.188	1.200	1.212
D3	29.930	30.230	30.530	1.178	1.190	1.202
E	14.700	15.000	15.300	0.579	0.591	0.602
E1	8.600	9.000	9.400	0.339	0.354	0.370
E2		1.600REF			0.063REF	
E3		1.500REF			0.059REF	
E4	18.200	18.600	19.000	0.717	0.732	0.748
E5	7.300	7.500	7.700	0.287	0.295	0.303
E6	1.100	1.500	1.900	0.043	0.059	0.075
e	2.340	2.540	2.740	0.092	0.100	0.108
e1	4.880	5.080	5.280	0.192	0.200	0.208
e2	3.356	3.556	3.756	0.132	0.140	0.148
e3	1.578	1.778	1.978	0.062	0.070	0.078
R	1.500	1.600	1.700	0.059	0.063	0.067
R1		0.400REF			0.016REF	
Q		2° - 6°			2° - 6°	

NOTES
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
4. ( ) IS REFERENCE.

Package Dimensions, IPM-5C







SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	5.900	6.300	6.700	0.232	0.248	0.264
A1	3.400	3.600	3.800	0.134	0.142	0.150
A2	4.700	5.100	5.500	0.185	0.201	0.217
A3	1.500	1.600	1.700	0.059	0.063	0.067
A4	2.500	2.700	2.900	0.098	0.106	0.114
B	0.400	0.500	0.600	0.016	0.020	0.024
b	0.500	0.600	0.700	0.020	0.024	0.028
b1	0.400	0.500	0.600	0.016	0.020	0.024
b2	0.400	0.500	0.600	0.016	0.020	0.024
b3	0.600	0.700	0.800	0.024	0.028	0.031
D	33.100	33.400	33.700	1.303	1.315	1.327
D1	30.800	31.000	31.200	1.213	1.220	1.228
D2	30.180	30.480	30.780	1.188	1.200	1.212
D3	29.930	30.230	30.530	1.178	1.190	1.202
E	14.700	15.000	15.300	0.579	0.591	0.602
E1	8.600	9.000	9.400	0.339	0.354	0.370
E2		1.600REF			0.063REF	
E3		1.500REF			0.059REF	
E4	18.120	18.520	18.920	0.713	0.729	0.745
E5	7.300	7.500	7.700	0.287	0.295	0.303
E6	1.100	1.500	1.900	0.043	0.059	0.075
e	2.340	2.540	2.740	0.092	0.100	0.108
e1	4.880	5.080	5.280	0.192	0.200	0.208
e2	3.356	3.556	3.756	0.132	0.140	0.148
e3	1.578	1.778	1.978	0.062	0.070	0.078
R	1.500	1.600	1.700	0.059	0.063	0.067
R1		0.400REF			0.016REF	
Q		2° - 6°			2° - 6°	

NOTES
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
4. ( ) IS REFERENCE.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.