ALPHA & OMEGA SEMICONDUCTOR

AOBB065V120X2Q

1200 V αSiC Silicon Carbide Power MOSFET

Features

- Proprietary αSiC MOSFET technology
- Low loss, with low $R_{DS,\ ON}$
- Fast switching with low R_G and low capacitance
- Optimized gate drive voltage (V_{GS} = 15 V)
- Low reverse recovery diode (Qrr)
- AEC-Q101 Automotive Qualified

Applications

- xEV Charger
- Electric Vehicle Supply Equipment (EVSE)
- Motor Drives
- Automotive Inverters

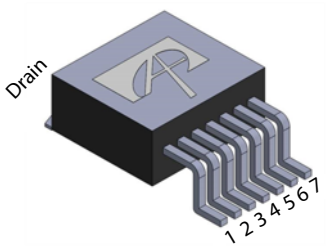
Product Summary

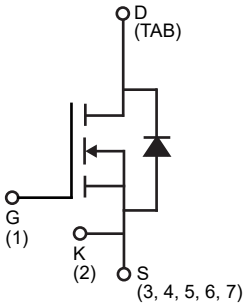
V_{DS} @ $T_{J,\ max}$	1200 V
I_{DM}	85 A
$R_{DS(ON),\ typ}$	65 mΩ
Q_{rr}	131 nC
E_{OSS} @ 800 V	30 µJ
100% UIS Tested	

AEC Qualified

GREEN Product

Pin Configuration





Ordering Part Number	Package Type	Form	Shipping Quantity
AOBB065V120X2Q	TO-263-7L	Tape and Reel	800/Reel

Absolute Maximum Ratings

(T_A = 25°C, unless otherwise noted)

Symbol	Parameter		AOBB065V120X2Q	Units
V_{DS}	Drain-Source Voltage		1200	V
$V_{GS,\ MAX}$	Gate-Source Voltage	Maximum	-8/+18	V
$V_{GS,OP,TRANS}$		Max Transient [A]	-8/+20	
$V_{GS,OP}$		Recommended Operating [B]	-5/+15	
I_D	Continuous Drain Current	T_C = 25°C	35	A
		T_C = 100°C	25	
I_{DM}	Pulsed Drain Current [C]		85	
E_{AS}	Single Pulsed Avalanche Energy [D]		250	mJ
P_D	Power Dissipation [C]		170	W
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 175	°C
T_L	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		260	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient (E,F)		40	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case (G)	0.73	0.88	°C/W

Electrical Characteristics

(T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V, T_J=25°C		1200			V
		I_D=250µA, V_{GS}=0V, T_J=150°C		1200			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=1200V, V_{GS}=0V				50	µA
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V, V_{GS}=+15/-5V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=10mA		1.8	2.8	3.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=15V, I_D=10A	T_J=25°C		65	85	mΩ
			T_J=150°C		90		mΩ
g_{fs}	Forward Transconductance	V_{DS}=20V, I_D=10A			8		S
V_{SD}	Diode Forward Voltage	I_S=10A,V_{GS}=-5V			4.1	5	V
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=800V, f=1MHz			1716		pF
C_{oss}	Output Capacitance				71		pF
C_{rss}	Reverse Transfer Capacitance				5		pF
E_{oss}	Coss Stored Energy				30		µJ
R_G	Gate Resistance	f=1MHz			1.7		Ω
SWITCHING							
Q_g	Total Gate Charge	V_{GS}=-5/+15V, V_{DS}=800V, I_D=20A			62		nC
Q_{gs}	Gate Source Charge				22		nC
Q_{gd}	Gate Drain Charge				22		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=0V/+15V, V_{DS}=800V, I_D=20A, R_G=5Ω, L=120µH, FWD: AOBB065V120X2Q			9.3		ns
t_r	Turn-On Rise Time				9.4		ns
$t_{d(off)}$	Turn-Off Delay Time				13		ns
t_f	Turn-Off Fall Time				8		ns
E_{on}	Turn-On Energy				192		µJ
E_{off}	Turn-Off Energy				25		µJ
E_{tot}	Total Switching Energy				217		µJ
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A,dI/dt=1560A/us, V_{DS}=800V			18		ns
I_{rm}	Peak Reverse Recovery Current				13		A
Q_{rr}	Body Diode Reverse Recovery Charge				131		nC

Notes:
A. < 1% duty cycle, f>1Hz
B. Device can be operated at V_{GS}=0/15V. Actual operating VGS will depend on application specifics such as parasitic inductance and dV/dt but should not exceed maximum ratings.
C. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
D. L=5mH, I_{AS}=10A, R_G=25Ω, Starting T_J=25°C.
E. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A=25°C.
F. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
G. The value of $R_{\theta JC}$ is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.
H. The static characteristics in Figures 1 to 8 are obtained using <300ms pulses, duty cycle 0.5% max.
I. These curves are based on $R_{\theta JC}$ which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

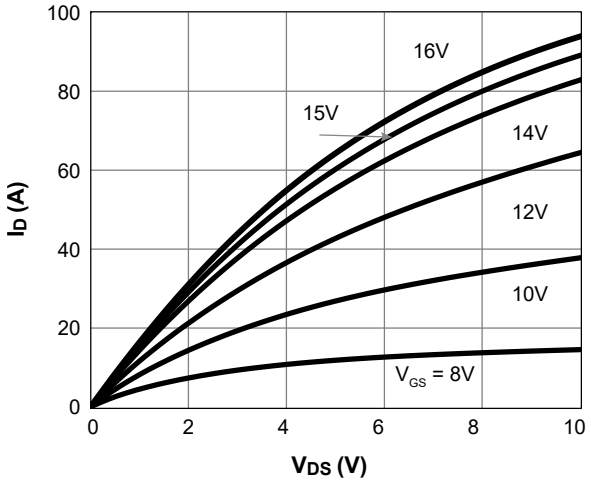


Figure 1. On-Region Characteristics T_J = 25°C

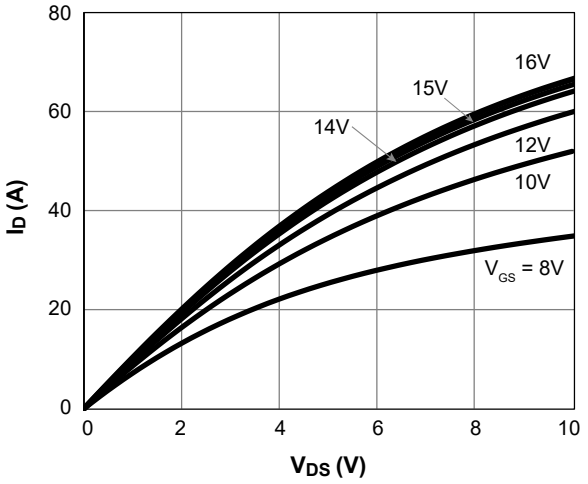


Figure 2. On-Region Characteristics T_J = 175°C

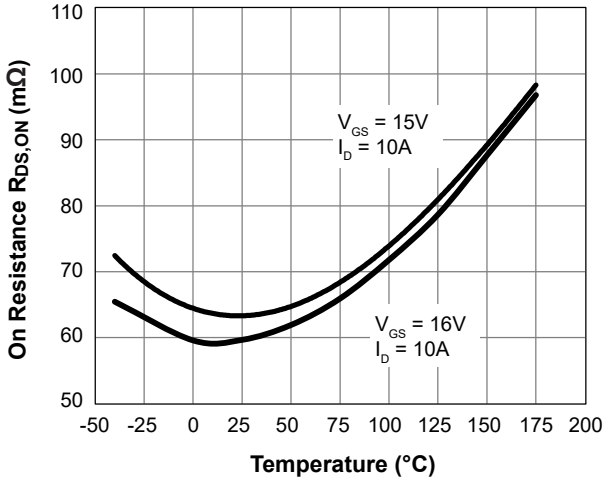


Figure 3. On Resistance vs. Junction Temperature

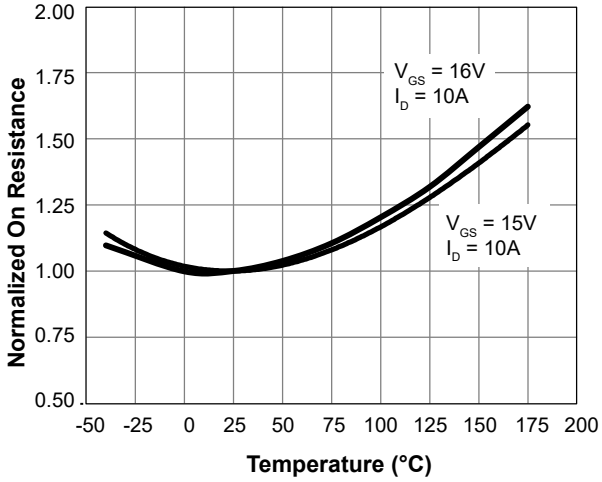


Figure 4. Normalized On-Resistance vs. Junction Temperature

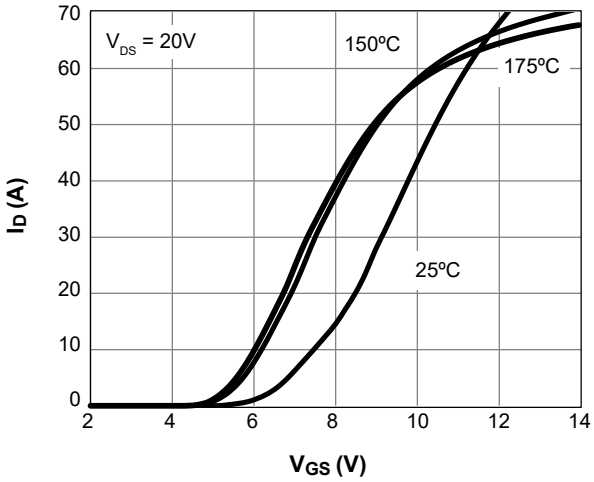


Figure 5. Transfer Characteristics

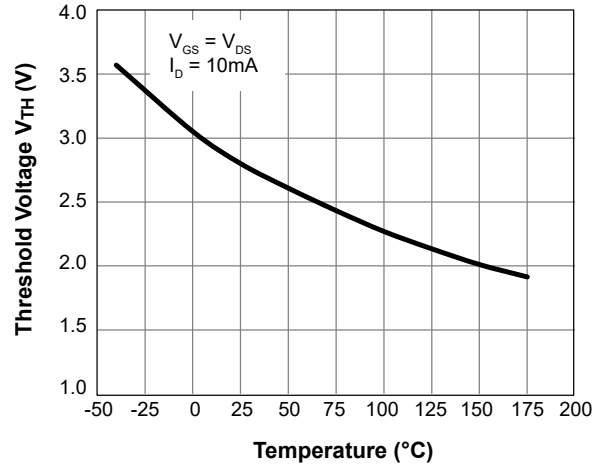


Figure 6. Threshold Voltage vs. Junction Temperature

Typical Electrical and Thermal Characteristics *(Continued)*

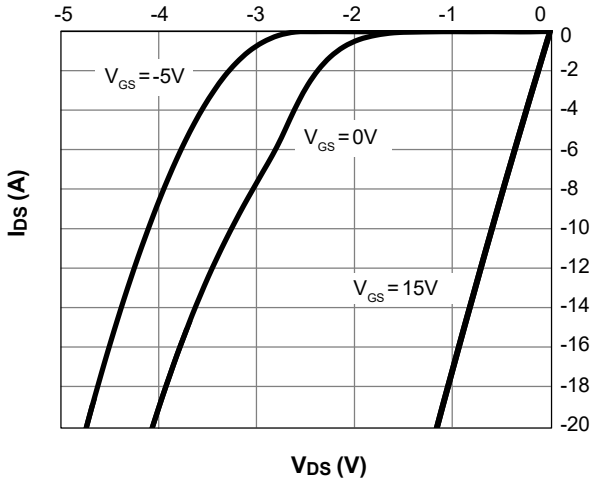


Figure 7. Body-diode Characteristics at 25°C

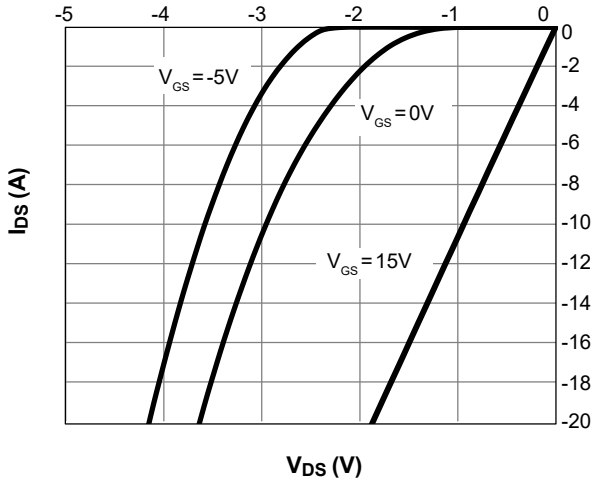


Figure 8. Body-diode Characteristics at 175°C

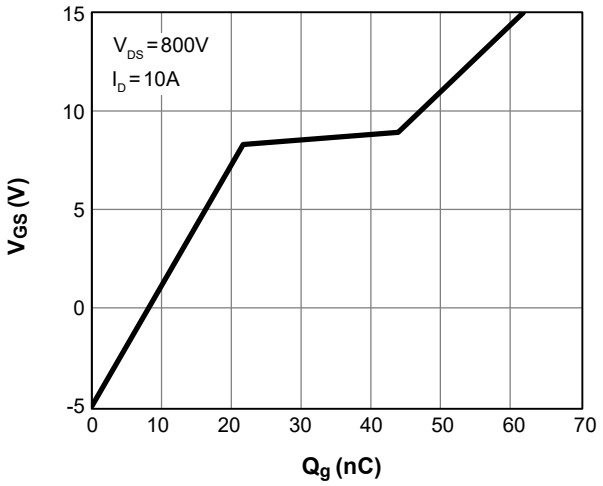


Figure 9. Gate-charge Characteristics

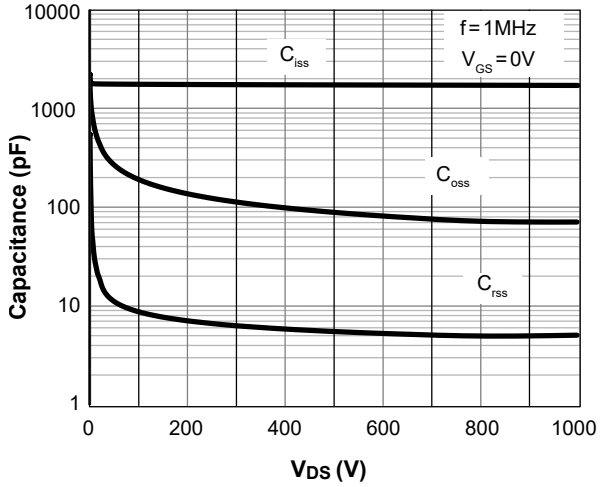


Figure 10. Capacitance Characteristics

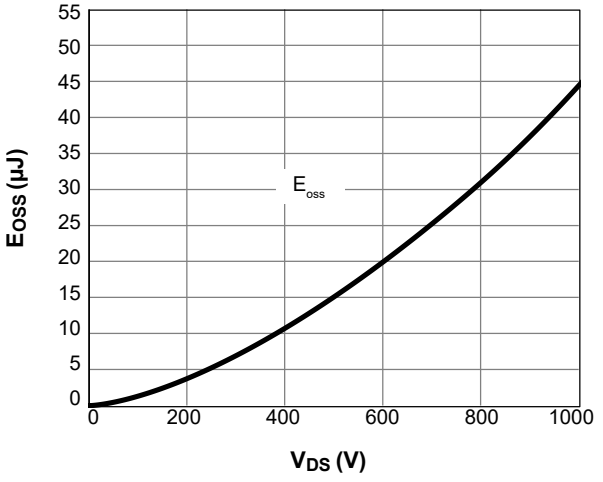


Figure 11. Coss Stored Energy

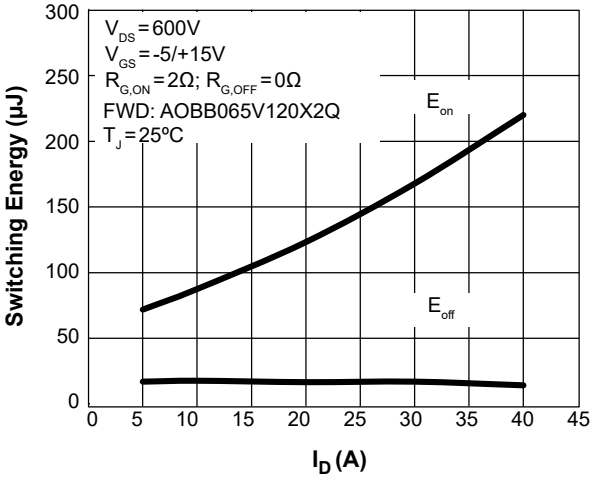


Figure 12. Switching Energy vs. Drain Current

Typical Electrical and Thermal Characteristics *(Continued)*

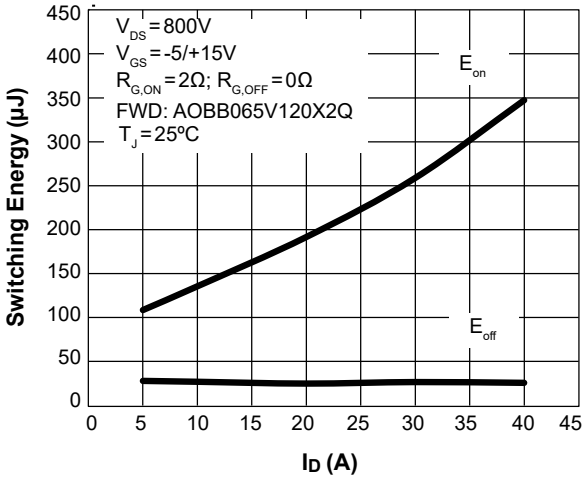


Figure 13. Switching Energy vs. Drain Current

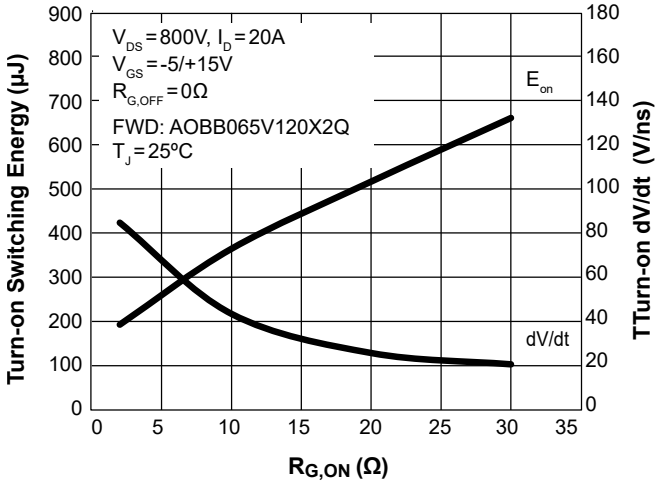


Figure 14. Turn-on Energy and dV/dt vs. External Gate Resistance

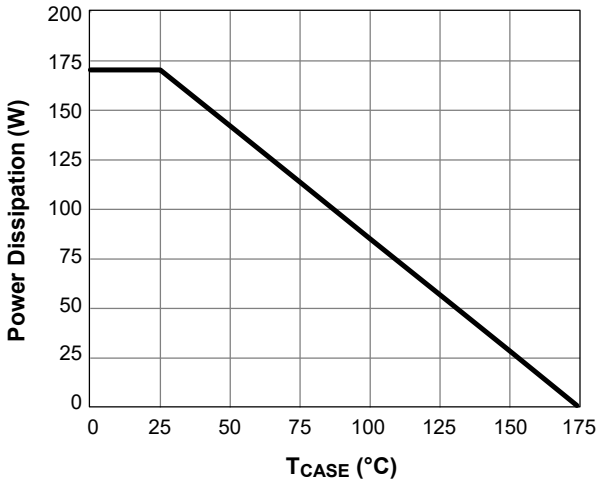


Figure 15. Power De-rating (Note I)

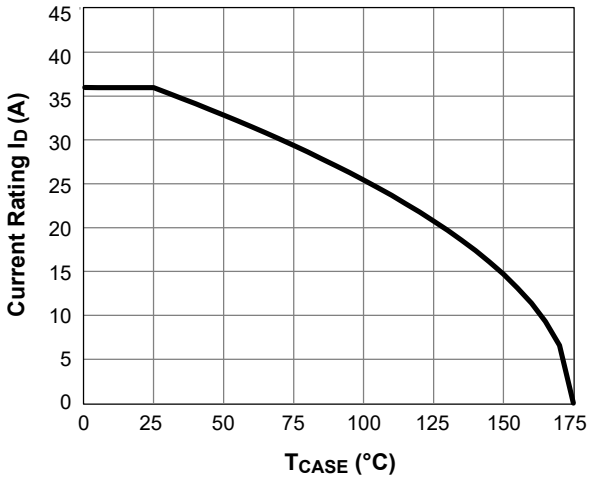


Figure 16. Current De-rating (Note I)

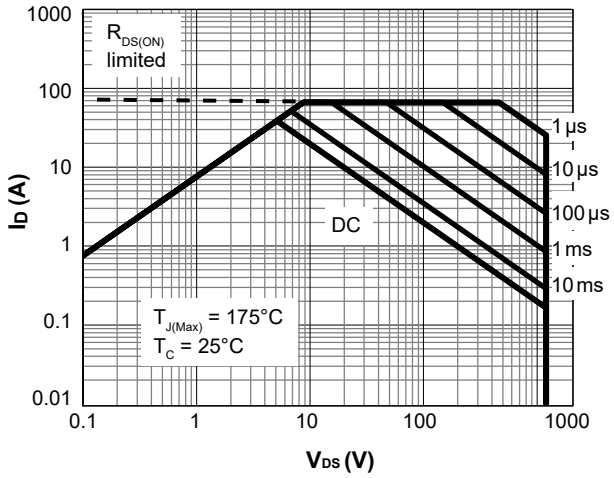


Figure 17. Maximum Forward Biased Safe Operating Area for AOBB150V120X2Q (Note I)

Typical Electrical and Thermal Characteristics *(Continued)*

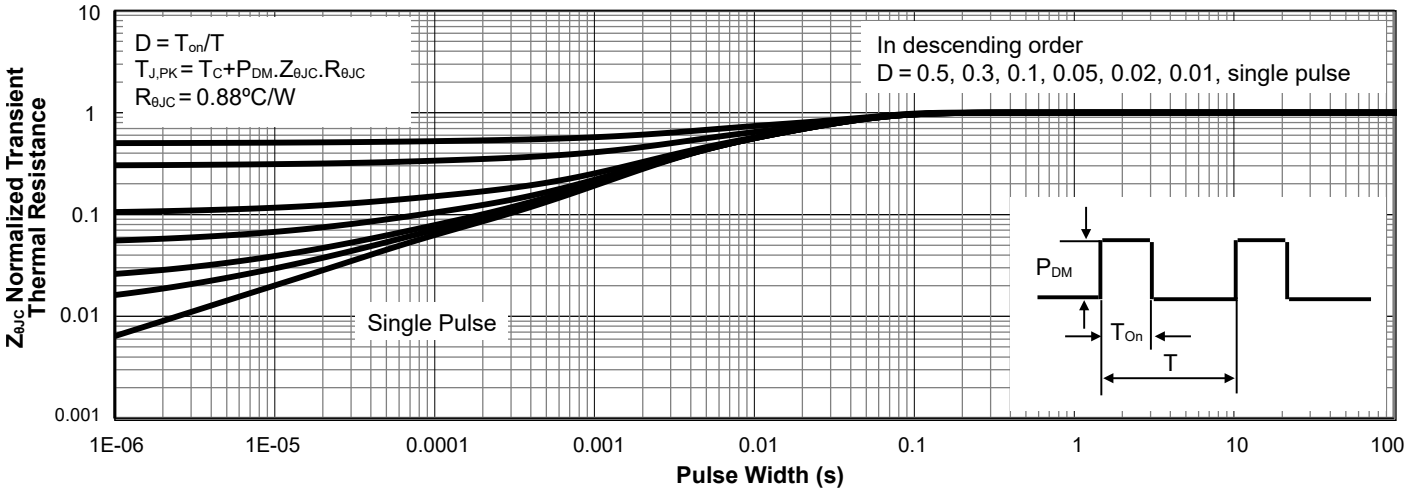


Figure 18. Normalized Maximum Transient Thermal Impedance for AOBB065V120X2Q (Note I)

Test Circuits and Waveforms

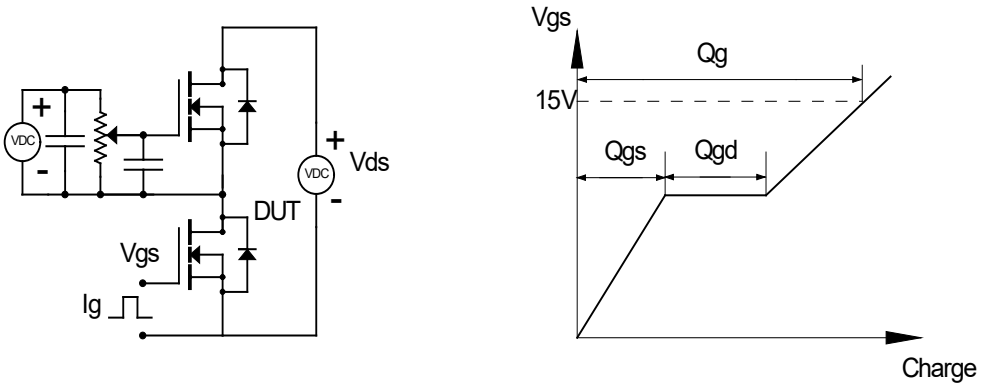


Figure 18. Gate Charge Test Circuits and Waveforms

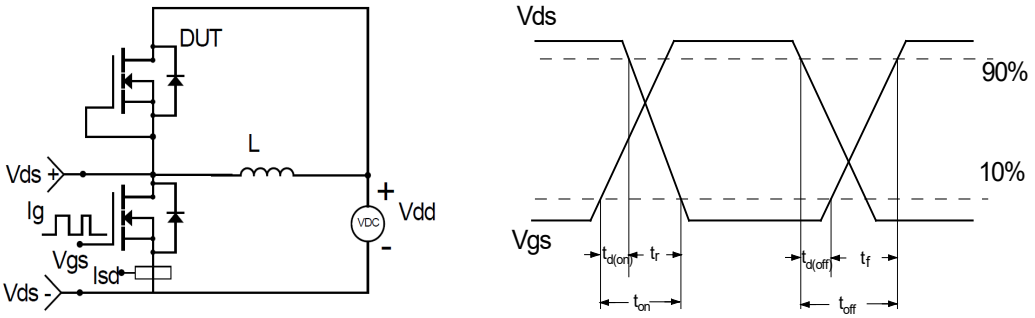


Figure 19. Inductive Switching Test Circuit and Waveforms

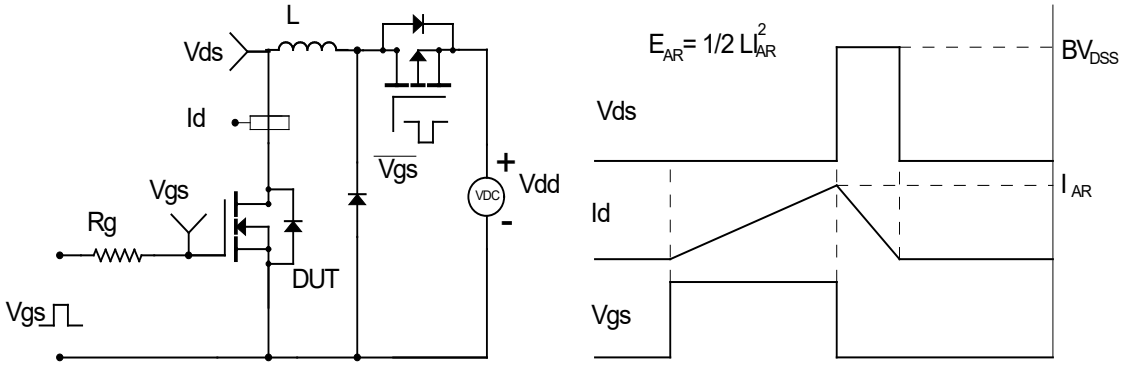


Figure 20. Unclamped Inductive Switching (UIS) Test Circuit and Waveforms

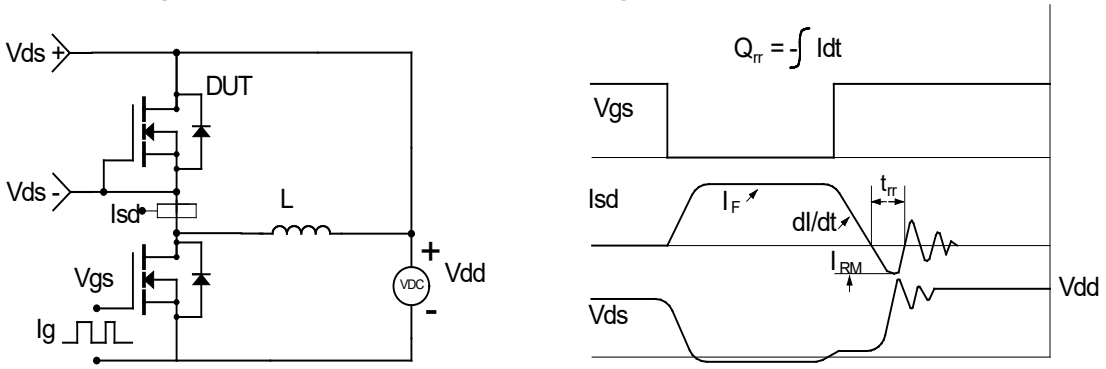
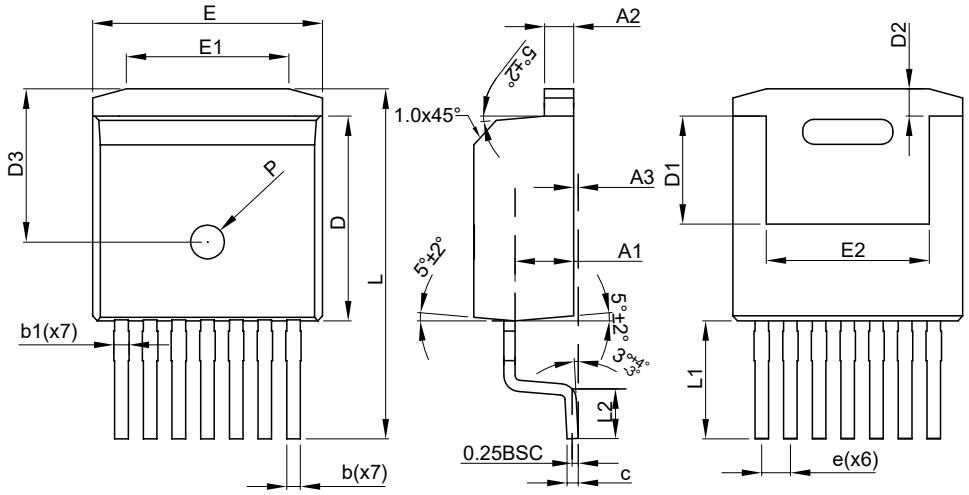
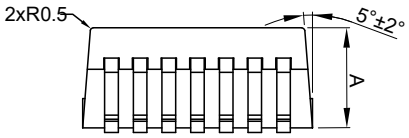


Figure 21. Diode Recovery Test Circuits and Waveforms

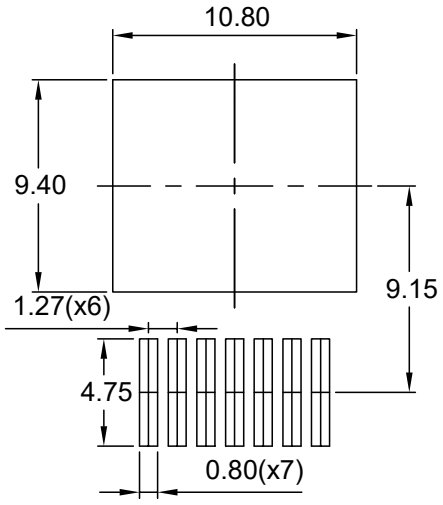
Package Dimensions, TO-263-7L



TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

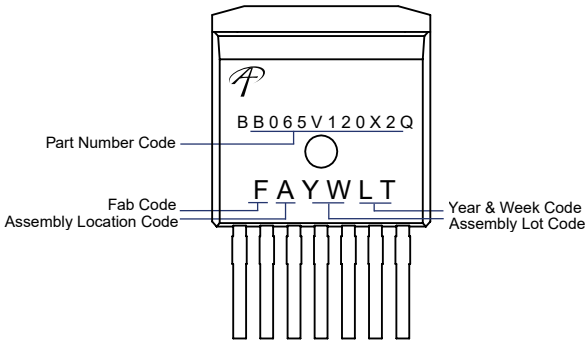
SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	4.30	4.43	4.56	0.169	0.174	0.180
A1	2.45	2.60	2.75	0.096	0.102	0.108
A2	1.20	1.30	1.40	0.047	0.051	0.055
A3	0.00	0.13	0.25	0.000	0.005	0.010
b	0.50	0.60	0.70	0.020	0.024	0.028
b1	0.60	0.70	0.90	0.024	0.028	0.035
c	0.45	0.50	0.60	0.018	0.020	0.024
D	8.93	9.08	9.23	0.352	0.357	0.363
D1	4.65	4.80	4.95	0.183	0.189	0.195
D2	0.98	1.20	1.42	0.039	0.047	0.056
D3	6.48	6.78	7.08	0.255	0.267	0.279
E	10.08	10.18	10.28	0.397	0.401	0.405
E1	6.50	7.00	7.50	0.256	0.276	0.295
E2	6.92	7.22	7.52	0.272	0.284	0.296
e	1.27BSC			0.05BSC		
L	15.00	15.50	16.00	0.591	0.610	0.630
L1	5.09	5.22	5.33	0.200	0.206	0.210
L2	1.90	2.20	2.50	0.075	0.087	0.098
P	1.40	1.50	1.60	0.055	0.059	0.063

NOTE:

1. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. DOTTED OUTLINE IS GUIDELINE TO BE COMPATIBLE WITH
INDUSTRY COMMON LAYOUT BUT NOT RECOMMENDED BY AOS.

Part Marking

AOBB065V120X2Q
TO-263-7L



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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.