AOCR35105E

12V Common-Drain Dual N-Channel MOSFET

MRigidCSP™

General Description

- Trench Power MOSFET technology
- Low $R_{SS(ON)}$
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS 2.0 and Halogen-Free Compliant

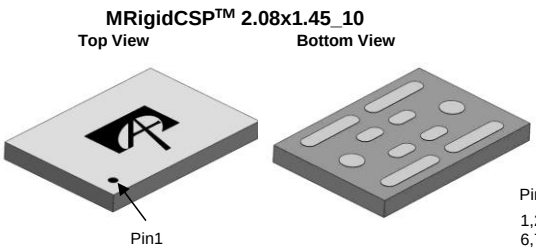
Applications

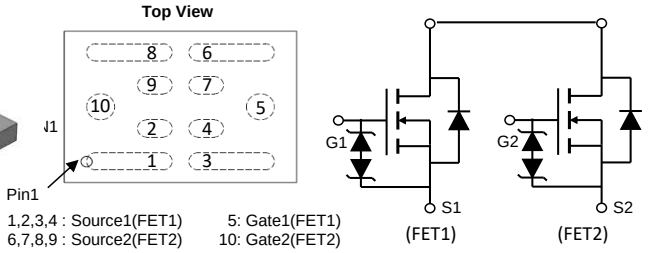
- Battery protection switch
- Mobile device battery charging and discharging

Product Summary

V_{SS}	12V
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 2.5mΩ
$R_{SS(ON)}$ (at V_{GS}=3.8V)	< 2.8mΩ
$R_{SS(ON)}$ (at V_{GS}=3.1V)	< 3.5mΩ
$R_{SS(ON)}$ (at V_{GS}=2.5V)	< 4.9mΩ
Typical ESD protection	**HBM Class 2**

MRigidCSP™ 2.08x1.45_10





1,2,3,4 : Source1(FET1)
6,7,8,9 : Source2(FET2)
5: Gate1(FET1)
10: Gate2(FET2)

Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOCR35105E	MRigidCSP™2.08x1.45_10	Tape & Reel	6000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Source-Source Voltage		V_{SS}	12	V
Gate-Source Voltage		V_{GS}	±8	V
Source Current(DC) Note1	T_A=25°C	I_S	25	A
Source Current(Pulse) Note2		I_{SM}	100	
Power Dissipation Note1	T_A=25°C	P_D	2.3	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	40	48	°C/W
Maximum Junction-to-Ambient	Steady-State		45	54	°C/W

Note 1. I_s rated value is based on bare silicon.Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 µs pulses, duty cycle 1% max.

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{SSS}	Source-Source Breakdown Voltage	I_S=250µA, V_{GS}=0V Test Circuit 6	12			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=12V, V_{GS}=0V Test Circuit 1			1	µA
		T_J=55°C			5	
I_{GSS}	Gate leakage current	V_{SS}=0V, V_{GS}=±8V Test Circuit 2			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS}, I_S=250µA Test Circuit 3	0.45	0.85	1.25	V
$R_{SS(ON)}$	Static Source to Source On-Resistance	V_{GS}=4.5V, I_S=5A Test Circuit 4	1.4	2	2.5	mΩ
		T_J=125°C	1.9	2.75	3.5	
		V_{GS}=3.8V, I_S=5A Test Circuit 4	1.5	2.2	2.8	mΩ
		V_{GS}=3.1V, I_S=5A Test Circuit 4	1.8	2.65	3.5	mΩ
		V_{GS}=2.5V, I_S=5A Test Circuit 4	2.6	3.65	4.9	mΩ
g_{FS}	Forward Transconductance	V_{SS}=5V, I_S=5A Test Circuit 3		60		S
V_{FSS}	Forward Source to Source Voltage	I_S=1A,V_{GS}=0V Test Circuit 5		0.6	1	V
DYNAMIC PARAMETERS						
R_g	Gate resistance	f=1MHz		2.6		KΩ
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{G1S1}=4.5V, V_{SS}=6V, I_S=5A		24		nC
$t_{D(on)}$	Turn-On DelayTime	V_{G1S1}=4.5V, V_{SS}=6V, R_L=1.2Ω, R_{GEN}=3Ω Test Circuit8		3.6		µs
t_r	Turn-On Rise Time			9.7		µs
$t_{D(off)}$	Turn-Off DelayTime			3.4		µs
t_f	Turn-Off Fall Time			18		µs

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

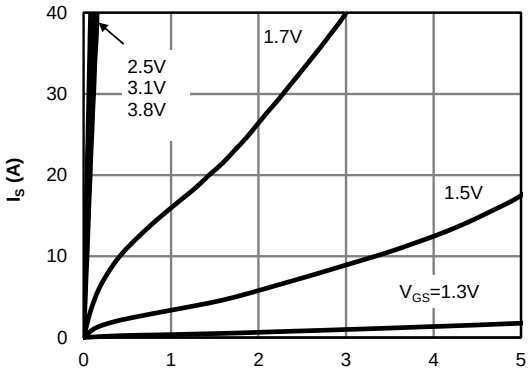


Figure 1: On-Region Characteristics

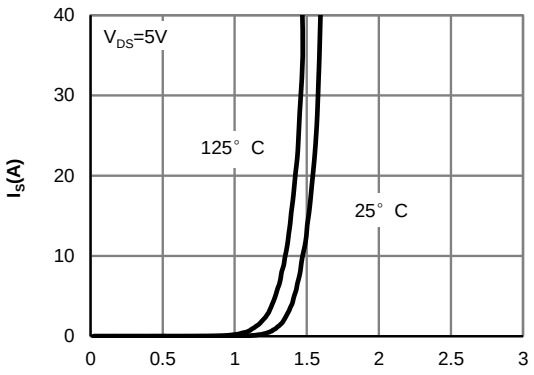


Figure 2: Transfer Characteristics

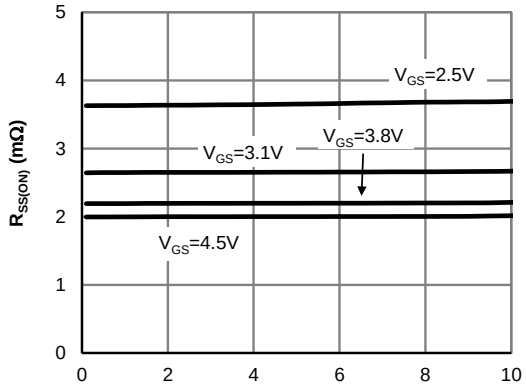


Figure 3: On-Resistance vs. Source Current and Gate Voltage

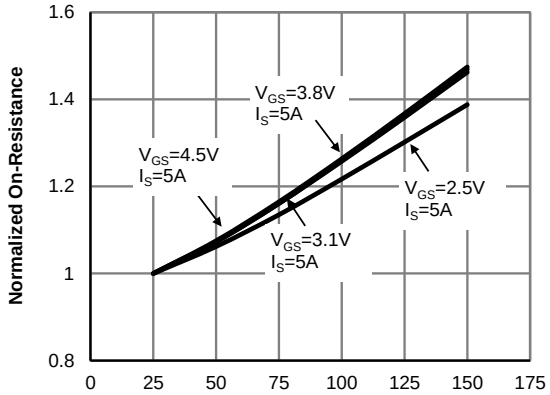


Figure 4: On-Resistance vs. Junction Temperature

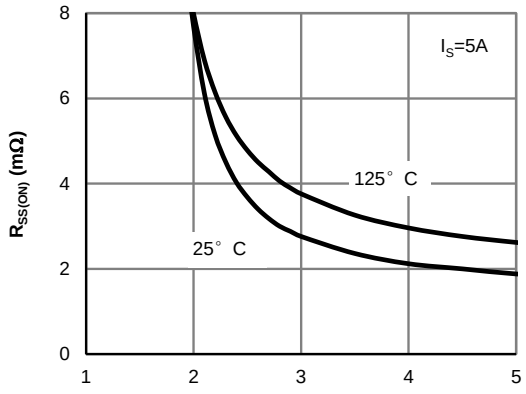


Figure 5: On-Resistance vs. Gate-Source Voltage

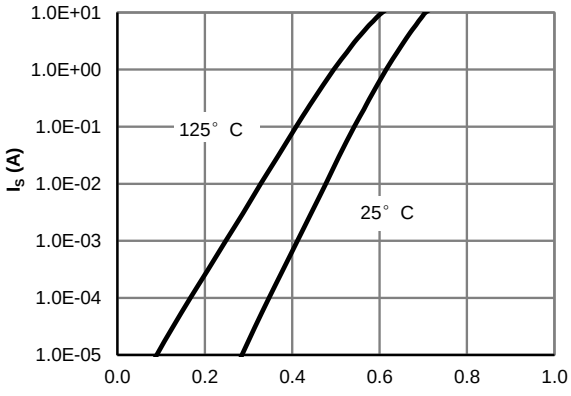


Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

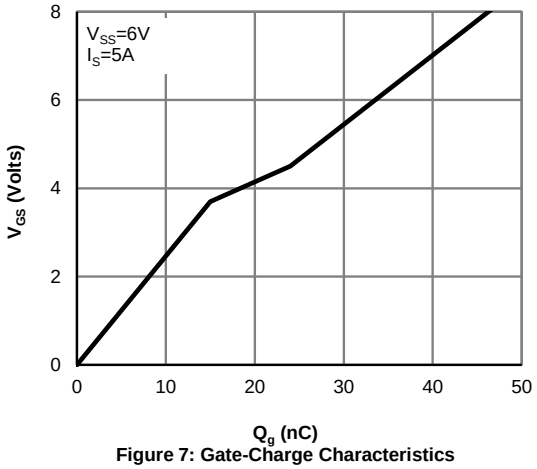


Figure 7: Gate-Charge Characteristics

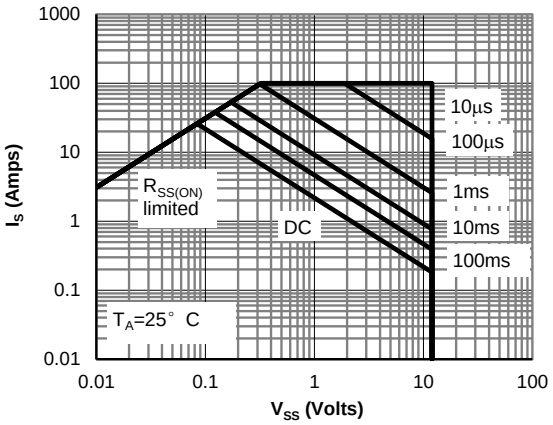


Figure 8: Maximum Forward Biased Safe Operating Area (Note1)

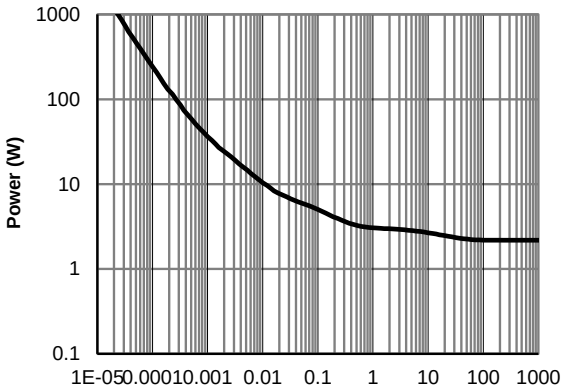


Figure 9: Single Pulse Power Rating Junction-to-Ambient (Note1)

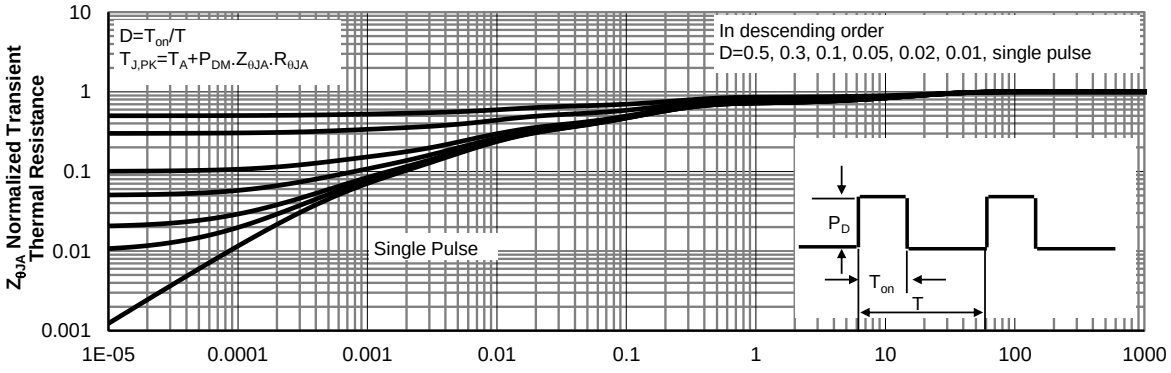
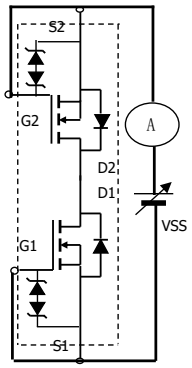


Figure 10: Normalized Maximum Transient Thermal Impedance (Note1)

TEST CIRCUIT 1 Isss

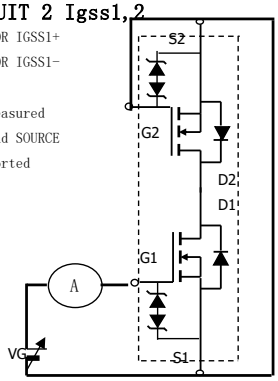
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 2 Igss1,2

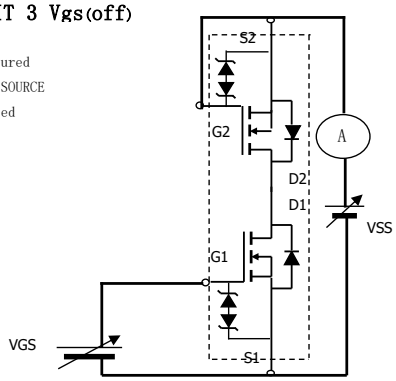
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



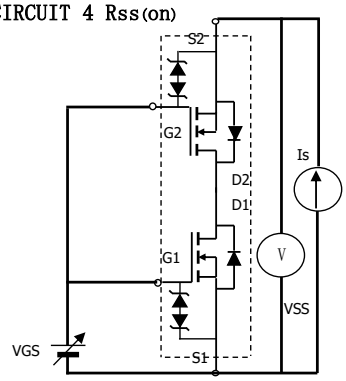
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted

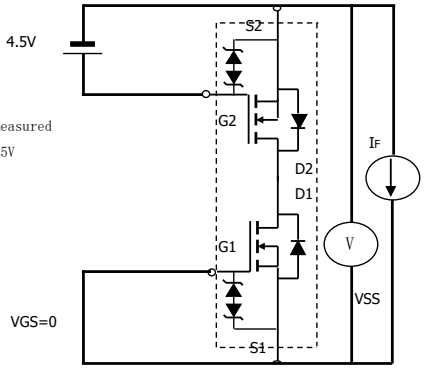


TEST CIRCUIT 4 Rss(on)

Vss/Is



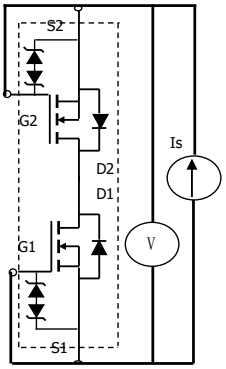
TEST CIRCUIT 5 $V_{F(SS)1,2}$



When FET1 measured
FET2 VGS=4.5V

TEST CIRCUIT 6 BV_{DSS}

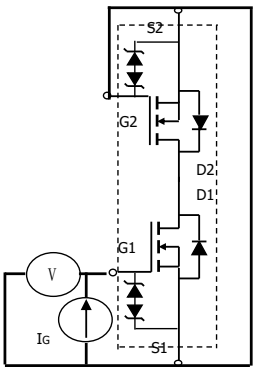
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 $BV_{GS01,2}$

POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-

When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 8
Switching time