
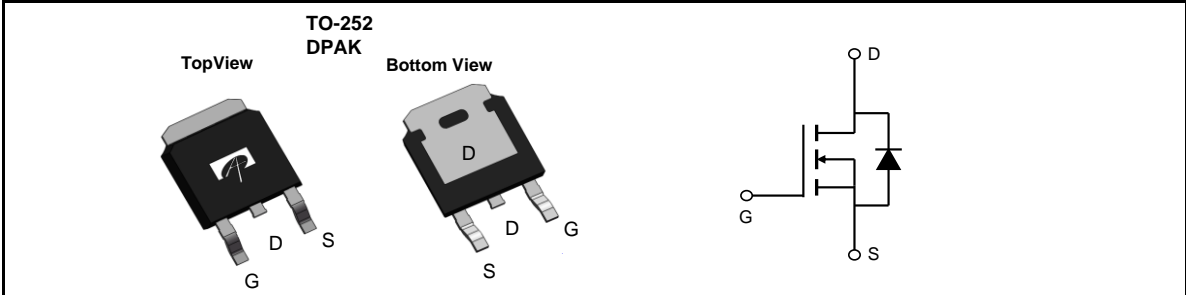


<p>General Description</p> <ul style="list-style-type: none"> Trench Power AlphaSGT™ technology Low $R_{DS(ON)}$ Wave solderable Excellent $Q_g \times R_{DS(ON)}$ Product (FOM) RoHS 2.0 and Halogen-Free Compliant <p>Applications</p> <ul style="list-style-type: none"> High Frequency Switching and Synchronous Rectification 	<p>Product Summary</p> <table style="width: 100%; border: none;"> <tr> <td style="padding: 2px;">V_{DS}</td> <td style="padding: 2px;">60V</td> </tr> <tr> <td style="padding: 2px;">I_D (at $V_{GS}=10V$)</td> <td style="padding: 2px;">70A</td> </tr> <tr> <td style="padding: 2px;">$R_{DS(ON)}$ (at $V_{GS}=10V$)</td> <td style="padding: 2px;">< 2.5mΩ</td> </tr> </table> <p style="margin-top: 10px;">100% UIS Tested 100% Rg Tested</p> 	V_{DS}	60V	I_D (at $V_{GS}=10V$)	70A	$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 2.5mΩ
V_{DS}	60V						
I_D (at $V_{GS}=10V$)	70A						
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 2.5mΩ						



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD66643	TO-252	Tape & Reel	2500

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ C$	70
		$T_C=100^\circ C$	70
Pulsed Drain Current ^C	I_{DM}	280	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ C$	37
		$T_A=70^\circ C$	30
Avalanche Current ^C	I_{AS}	39	A
Avalanche energy $L=0.3mH$ ^C	E_{AS}	228	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	156
		$T_C=100^\circ C$	63
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	6.2
		$T_A=70^\circ C$	4
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient ^{A D}				
Maximum Junction-to-Case	$R_{\theta JC}$	0.6	0.8	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.2	2.8	3.4	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		2.1 3.5	2.5 4.2	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		70		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				70	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		4800		pF
C _{OSS}	Output Capacitance			1300		pF
C _{ISS}	Reverse Transfer Capacitance			36		pF
R _g	Gate resistance	f=1MHz	0.4	0.9	1.4	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =20A		68	95	nC
Q _{gs}	Gate Source Charge			17		nC
Q _{gd}	Gate Drain Charge			15		nC
Q _{OSS}	Output Charge	V _{GS} =0V, V _{DS} =30V		84		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =30V, R _L =1.5Ω, R _{GEN} =3Ω		16.5		ns
t _r	Turn-On Rise Time			11.5		ns
t _{D(off)}	Turn-Off DelayTime			45.5		ns
t _f	Turn-Off Fall Time			13		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		32		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		132		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

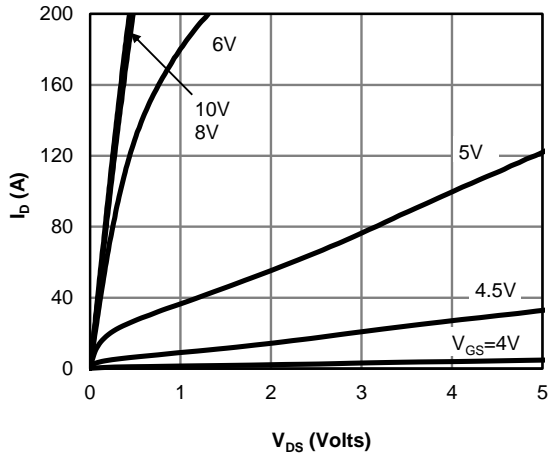


Figure 1: On-Region Characteristics (Note E)

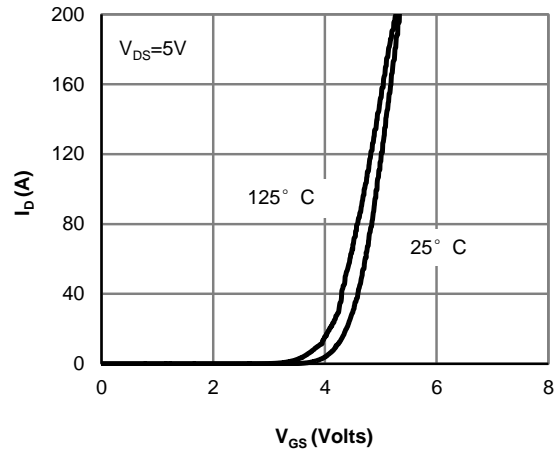


Figure 2: Transfer Characteristics (Note E)

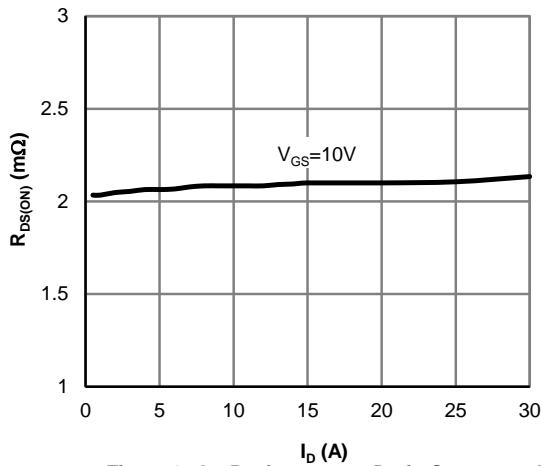


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

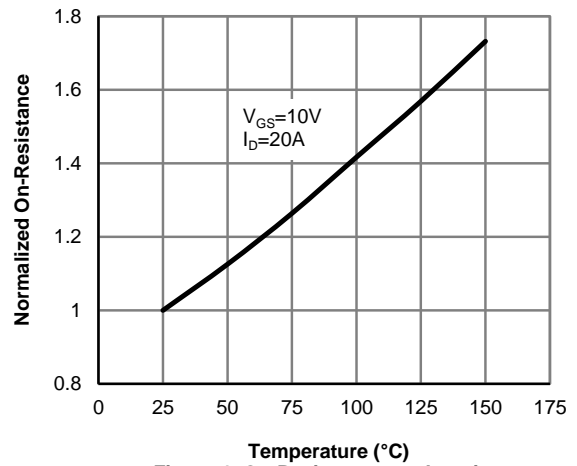


Figure 4: On-Resistance vs. Junction Temperature (Note E)

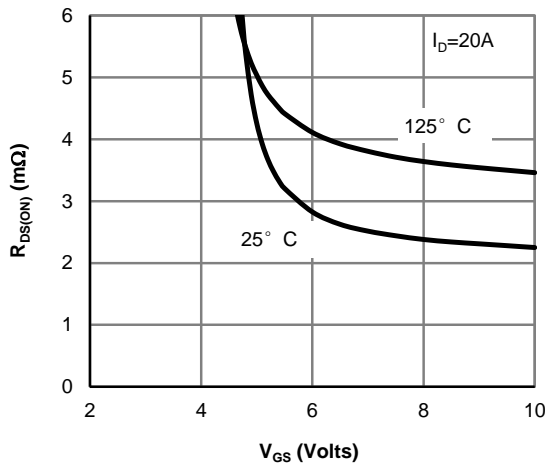


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

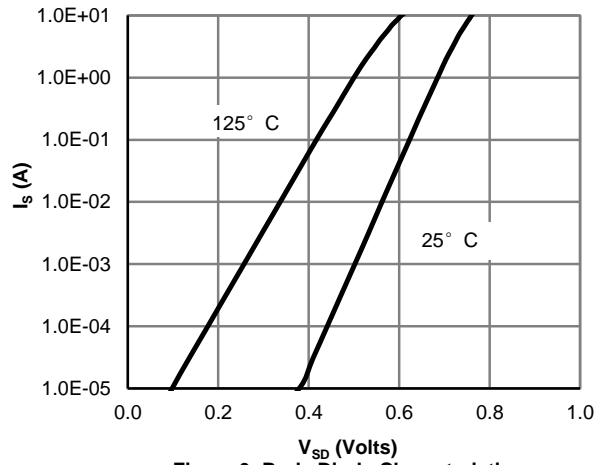


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

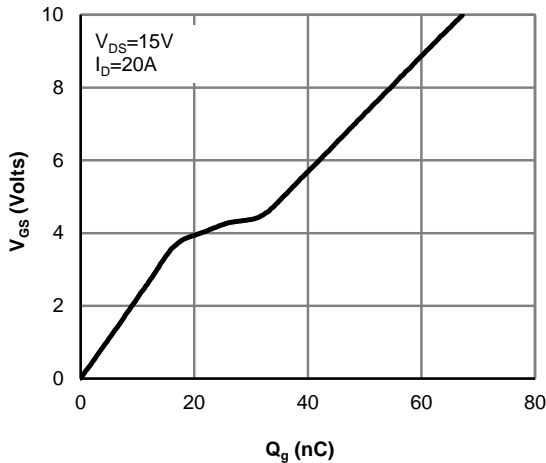


Figure 7: Gate-Charge Characteristics

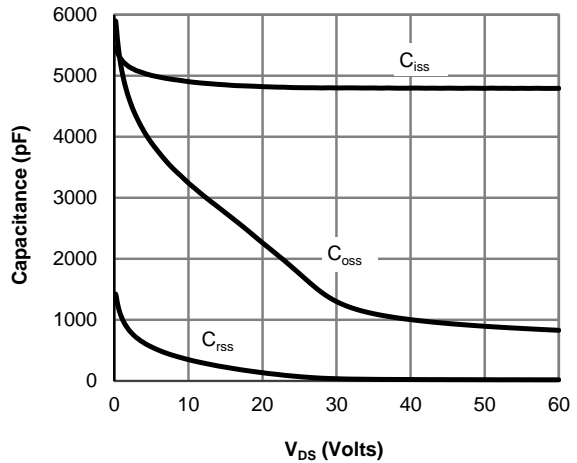


Figure 8: Capacitance Characteristics

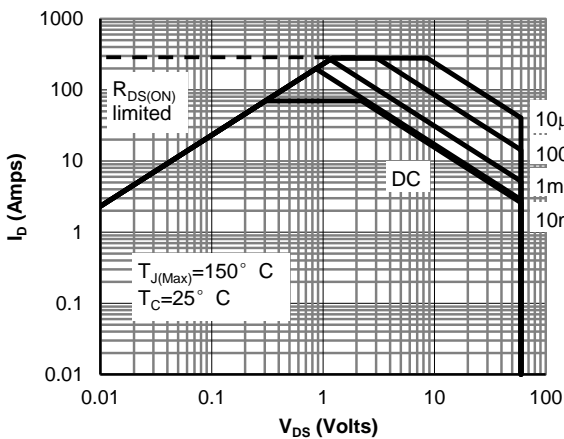


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

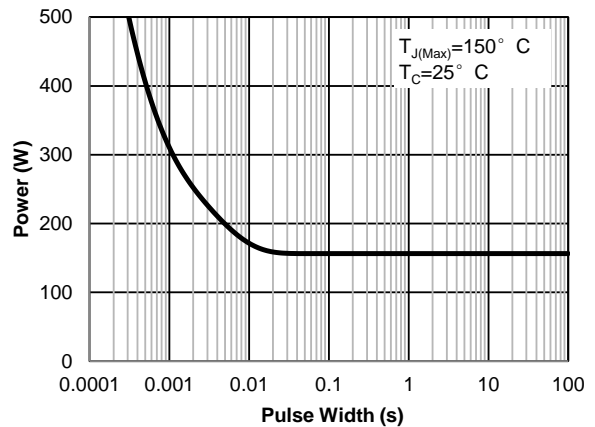


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

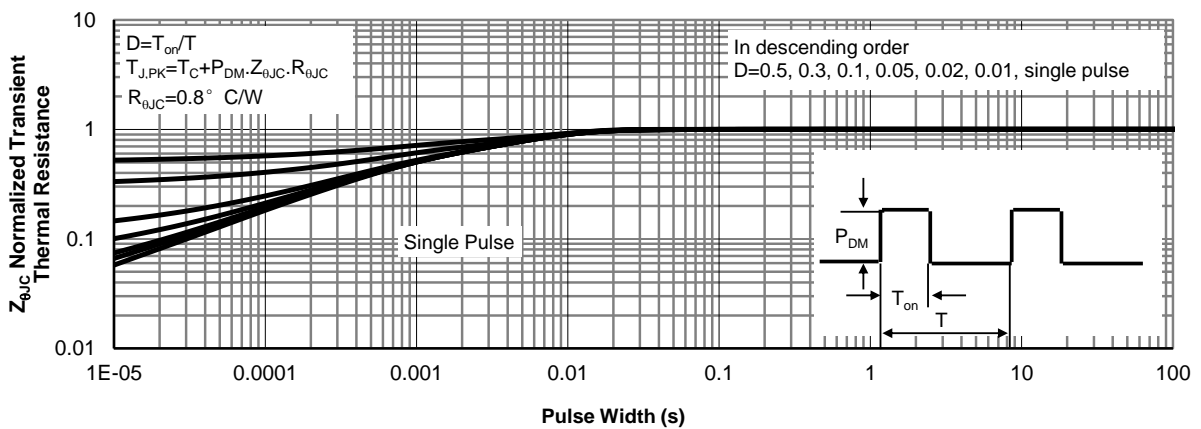


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

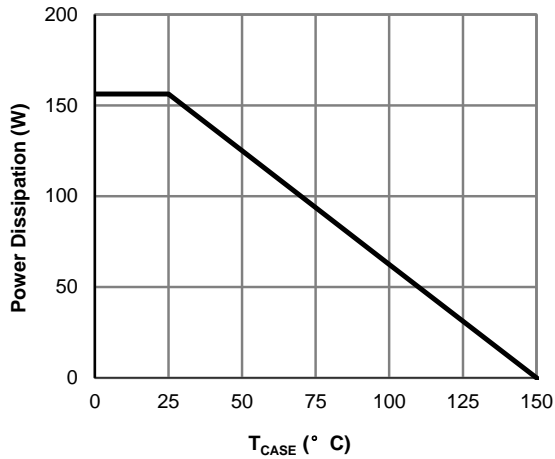


Figure 12: Power De-rating (Note F)

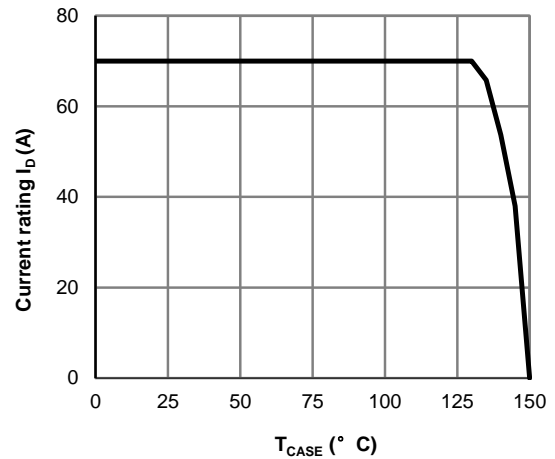


Figure 13: Current De-rating (Note F)

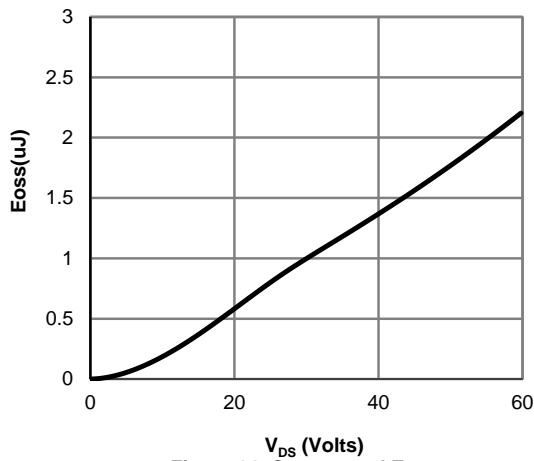


Figure 14: Coss stored Energy

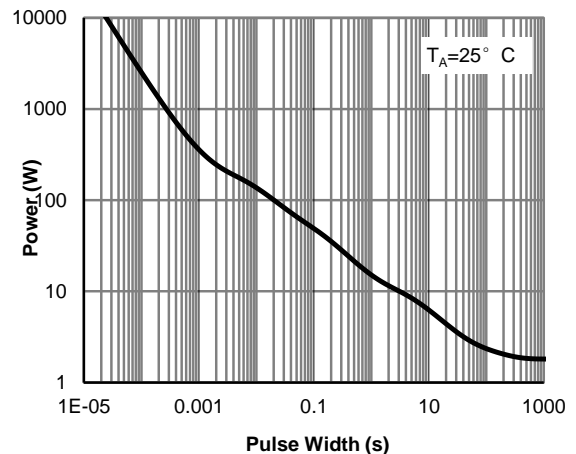


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

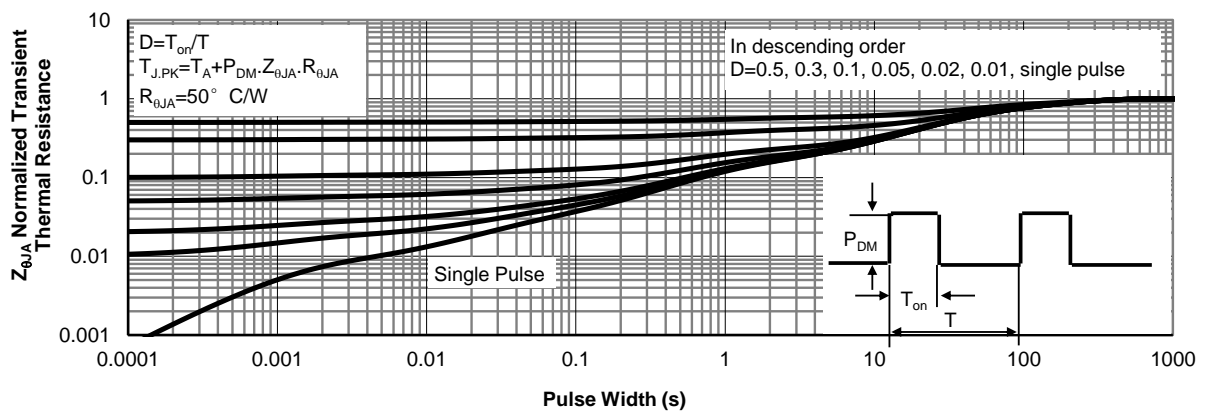


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

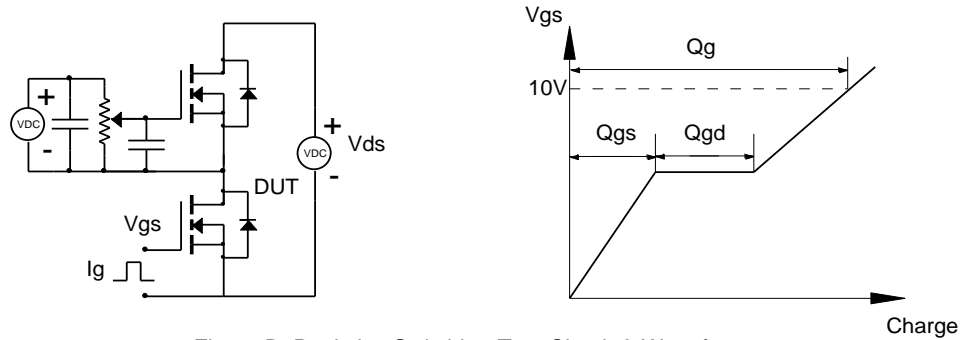


Figure B: Resistive Switching Test Circuit & Waveforms

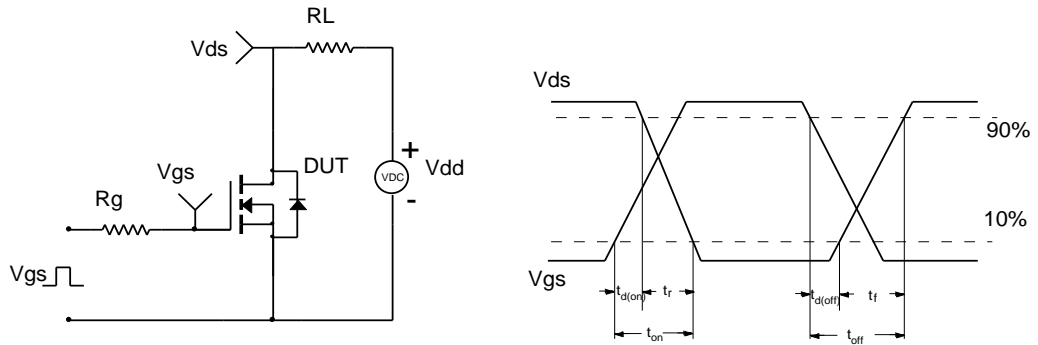


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

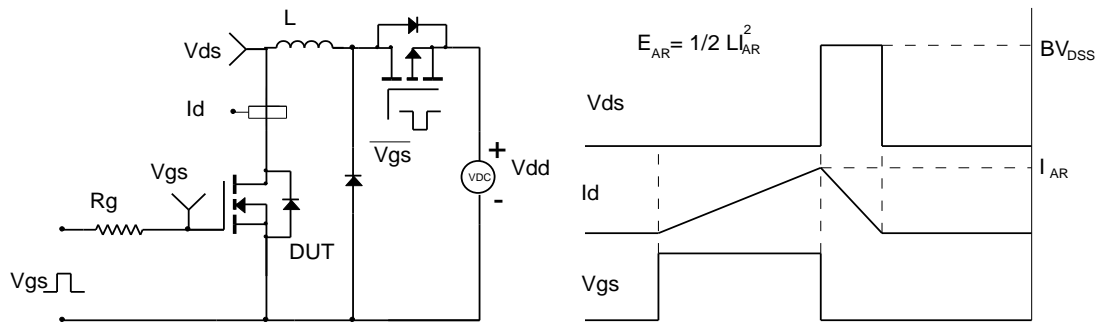


Figure D: Diode Recovery Test Circuit & Waveforms

