



General Description

- Trench Power AlphaSGT™ Technology
- Robust SOA for linear mode operation
- Low $R_{DS(ON)}$
- MSL1 up to 260°C peak reflow
- RoHS 2.0 and Halogen-Free Compliant

Applications

- Hot swap
- Load switch
- Soft start
- 48V systems

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	334A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 1.85mΩ

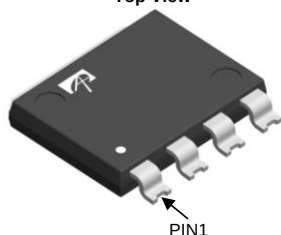
100% UIS Tested
100% Rg Tested

Max $T_j=175^{\circ}C$

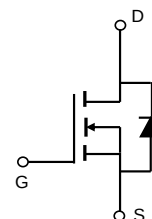
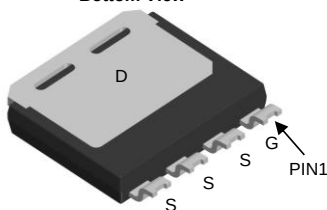


LFLPAK8x8

Top View



Bottom View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOLV66935	LFLPAK8x8	Tape & Reel	2000

Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	334	A
		236	
Pulsed Drain Current ^C	I_{DM}	1336	
Avalanche Current ^C	I_{AS}	100	A
Avalanche energy L=0.1mH ^C	E_{AS}	500	mJ
Power Dissipation ^B	P_D	428	W
		214	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Max	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	40	$^{\circ}C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	0.35	$^{\circ}C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.1	2.6	3.1	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		1.54 2.6	1.85 3.2	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		36		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				200	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance ^G	V _{GS} =0V, V _{DS} =50V, f=200KHz	11700	14700	17600	pF
C _{oss}	Output Capacitance ^G		2100	3000	3900	pF
C _{rss}	Reverse Transfer Capacitance ^G		10	36	62	pF
R _g	Gate resistance	f=1MHz	0.5	1	1.5	Ω
SWITCHING PARAMETERS^G						
Q _{g(10V)}	Total Gate Charge ^G	V _{GS} =10V, V _{DS} =50V, I _D =20A	95	165	235	nC
Q _{gs}	Gate Source Charge ^G		32	58	84	nC
Q _{gd}	Gate Drain Charge ^G		8	15	22	nC
Q _{oss}	Output Charge	V _{GS} =0V, V _{DS} =50V		240		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =2.5Ω, R _{GEN} =3Ω		37		ns
t _r	Turn-On Rise Time			26		ns
t _{D(off)}	Turn-Off DelayTime			76		ns
t _f	Turn-Off Fall Time			32		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		58		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		465		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=175° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. Guaranteed by design. Not production tested.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

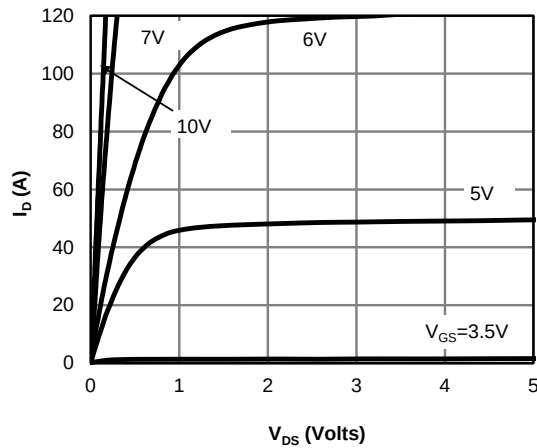


Figure 1: On-Region Characteristics (Note E)

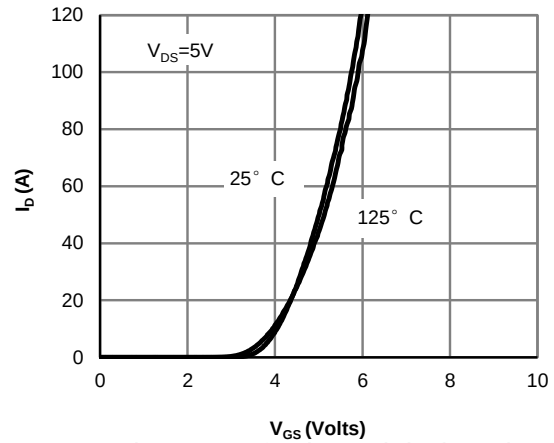


Figure 2: Transfer Characteristics (Note E)

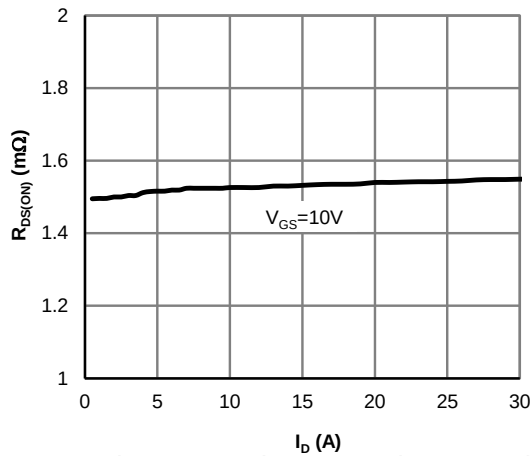


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

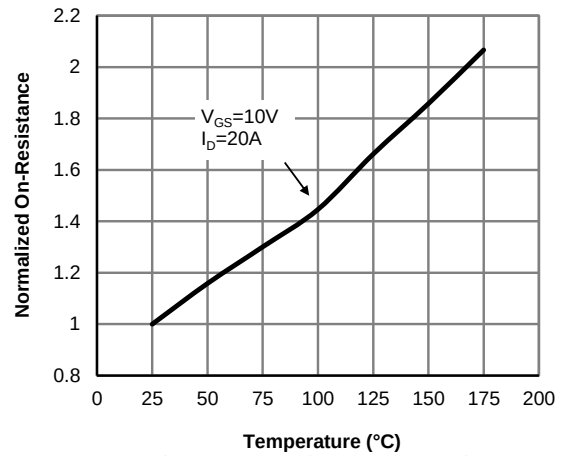


Figure 4: On-Resistance vs. Junction Temperature (Note E)

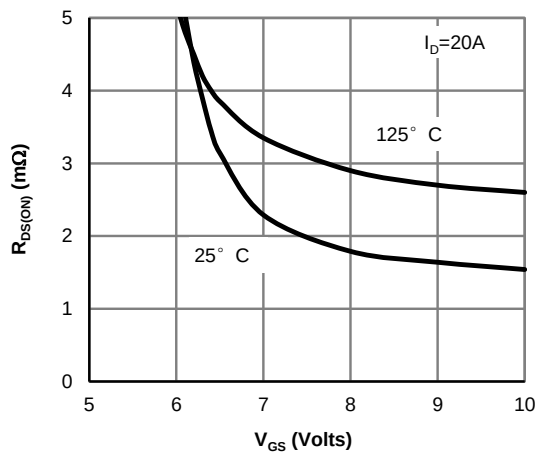


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

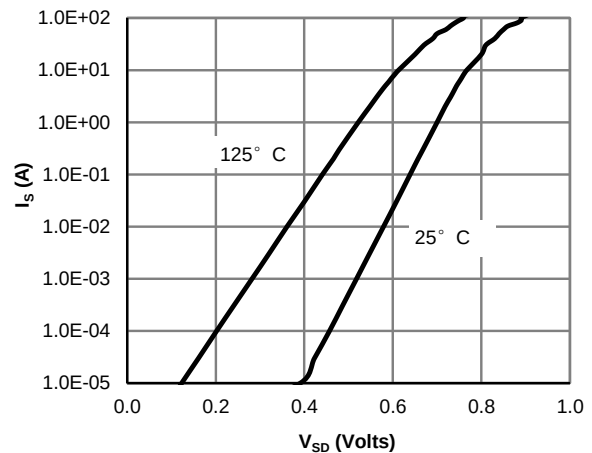
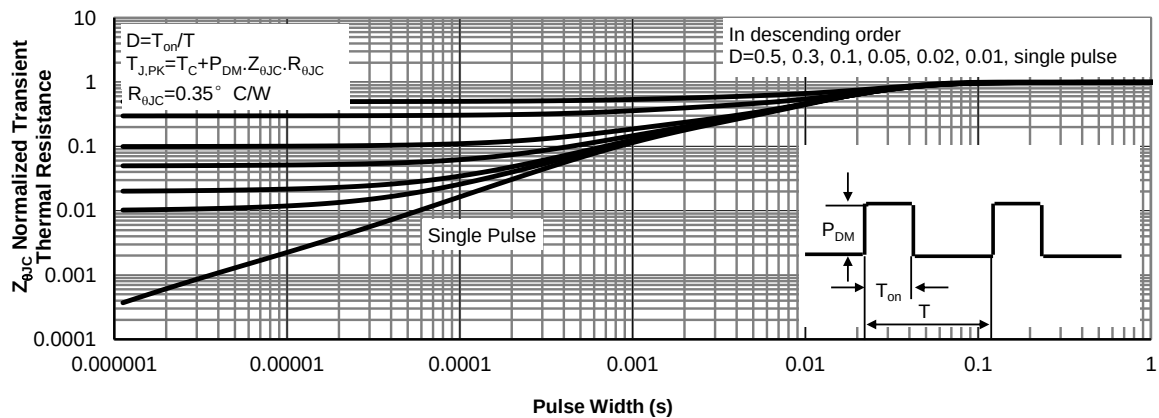
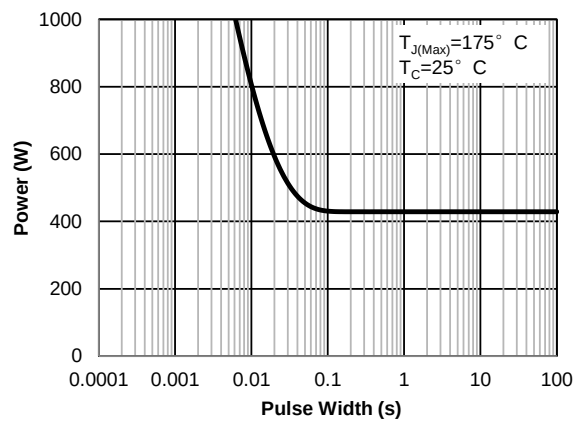
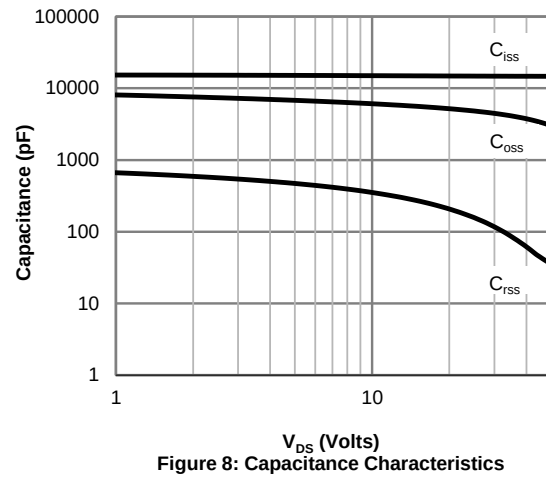
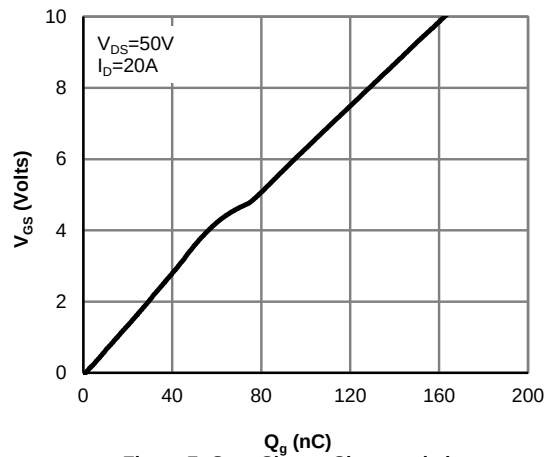


Figure 6: Body-Diode Characteristics (Note E)

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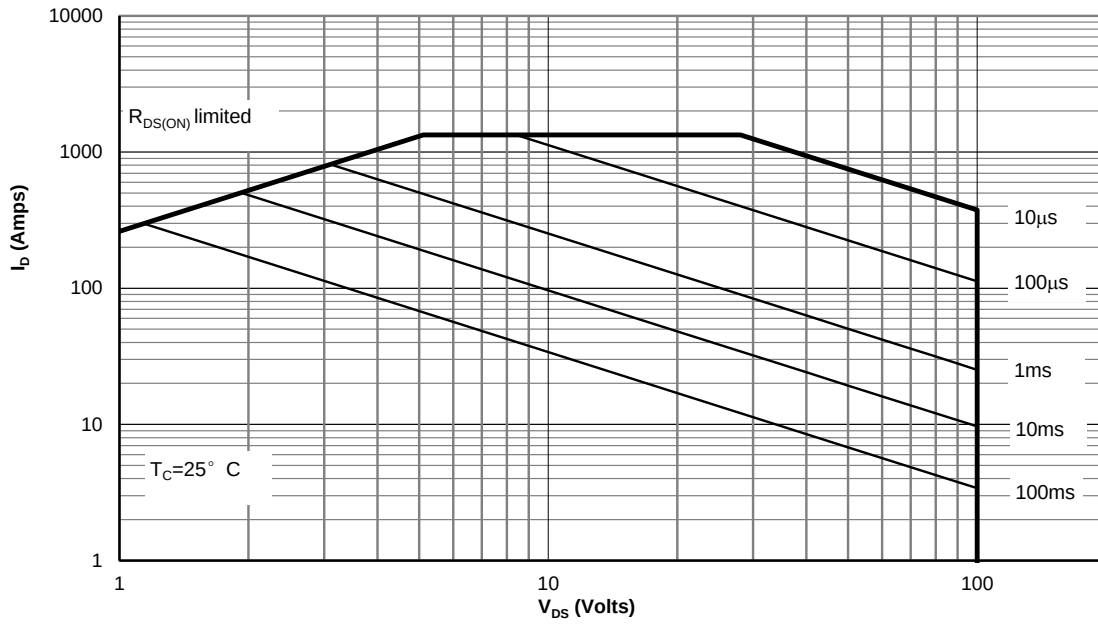


Figure 11: Safe Operating Area (Note F)

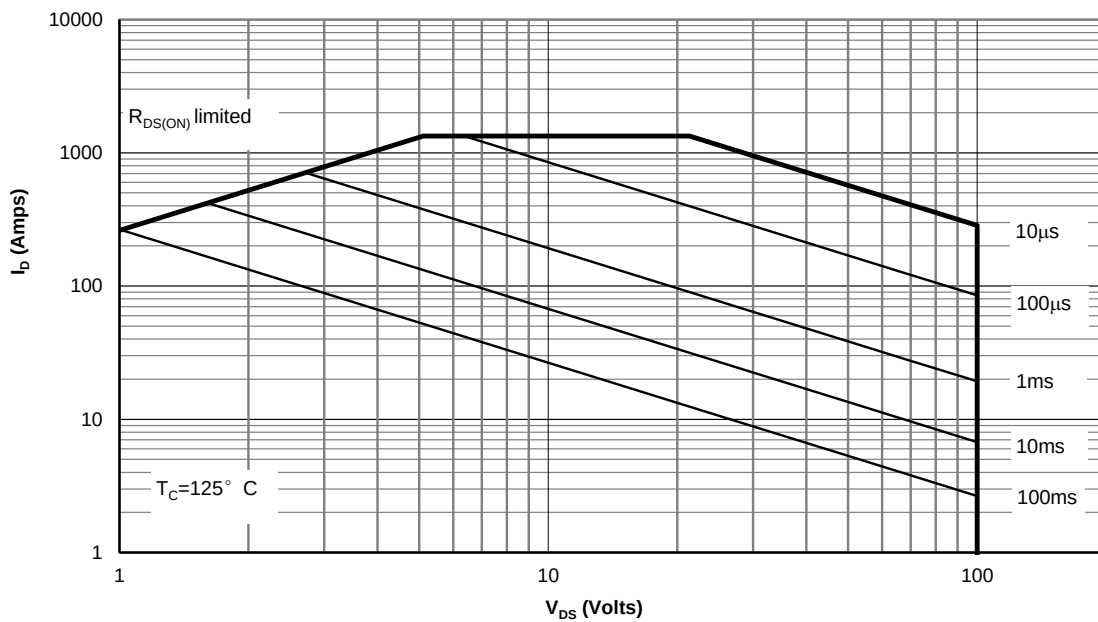


Figure 12: Safe Operating Area (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

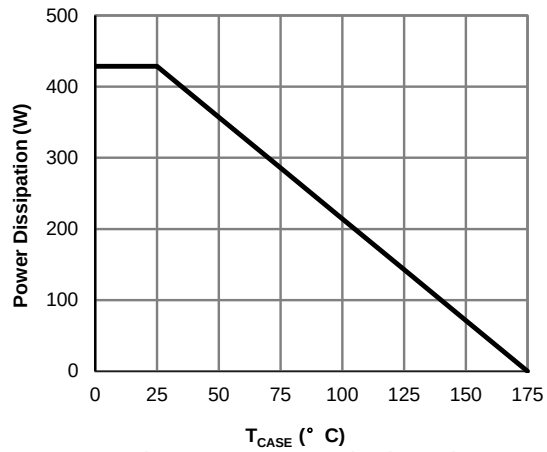


Figure 13: Power De-rating (Note F)

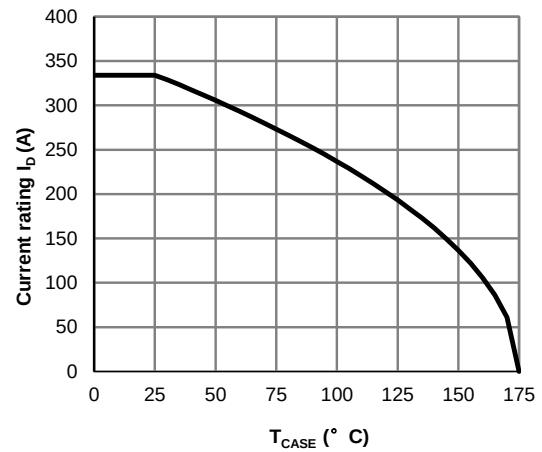


Figure 14: Current De-rating (Note F)

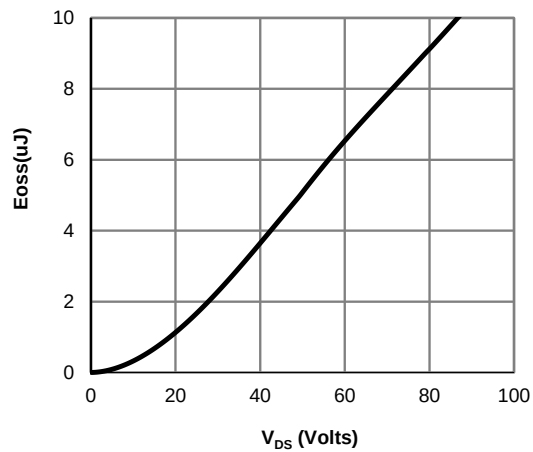


Figure 15: Coss stored Energy

Figure A: Gate Charge Test Circuit & Waveforms

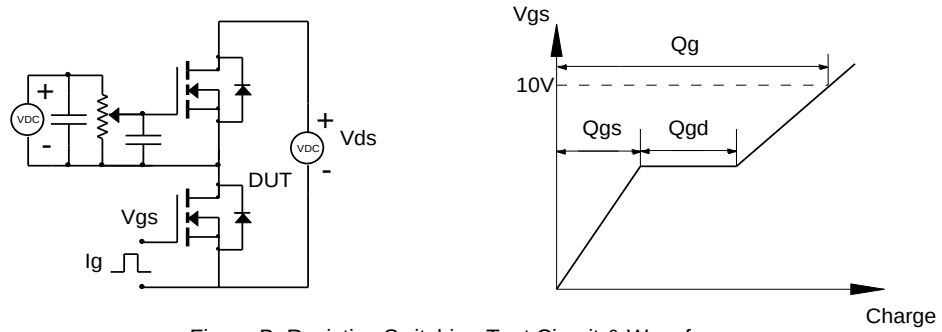


Figure B: Resistive Switching Test Circuit & Waveforms

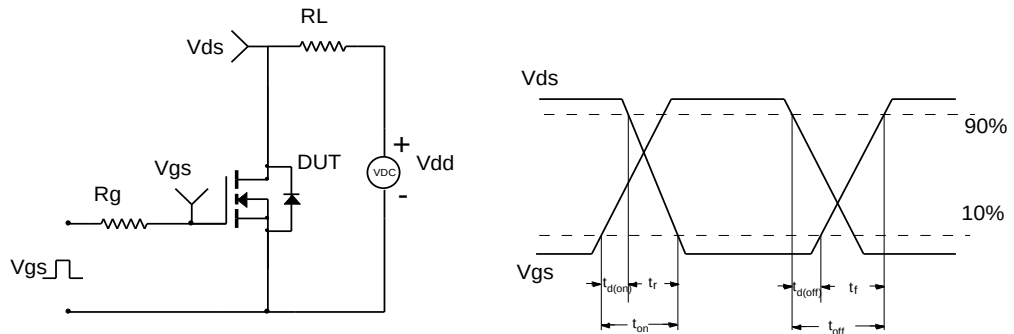


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

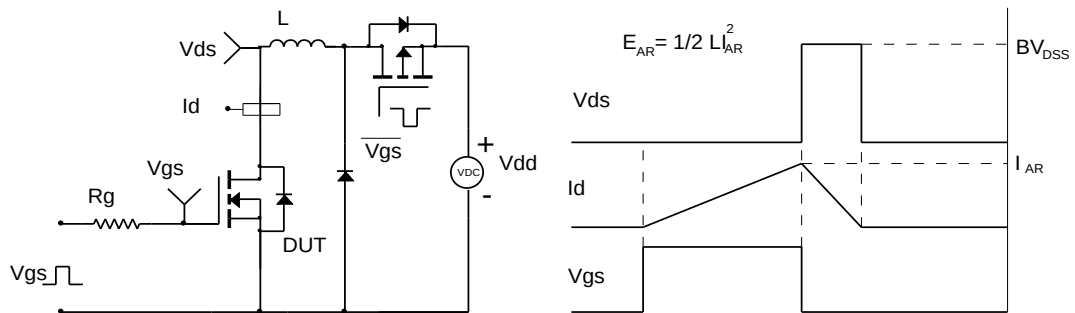


Figure D: Diode Recovery Test Circuit & Waveforms

