ALPHA & OMEGA SEMICONDUCTOR

AON6926

30V Dual Asymmetric N-Channel MOSFET

General Description

The AON6926 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6A package. The Q1 "High Side" MOSFET is desgined to minimze switching losses. The Q2 "Low Side" MOSFET is an SRFET™ that features low $R_{DS(ON)}$ to reduce conduction losses as well as an integrated Schottky diode with low Q_{RR} and V_f to reduce switching losses. The AON6926 is well suited for use in compact DC/DC converter applications.

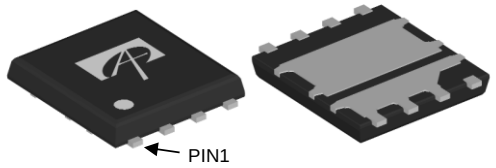
Product Summary

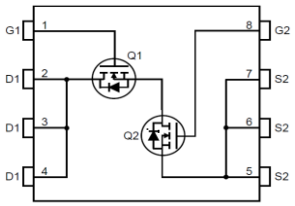
	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	44A	50A
$R_{DS(ON)}$ (at V_{GS}=10V)	<11mΩ	<8.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	<14mΩ	<12mΩ

100% UIS Tested
100% Rg Tested

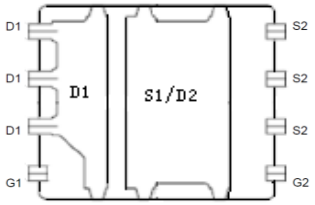
Green Product

DFN5X6





Top View



Bottom View

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C=25°C	I_D	44	50	A
	T_C=100°C		28	32	
Pulsed Drain Current [C]		I_{DM}	100	140	
Continuous Drain Current	T_A=25°C	I_{DSM}	11	12	A
	T_A=70°C		9	10	
Avalanche Current [C]		I_{AS}, I_{AR}	27	15	A
Avalanche Energy L=0.1mH [C]		E_{AS}, E_{AR}	36	11	mJ
Power Dissipation [B]	T_C=25°C	P_D	31	35	W
	T_C=100°C		12.5	14	
Power Dissipation [A]	T_A=25°C	P_{DSM}	1.9	2.1	W
	T_A=70°C		1.2	1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	29	24	35	29	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		56	50	67	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3.4	3	4	3.6	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=125°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.5	2	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		8.8	11	mΩ
		T_J=125°C		12	15	
		V_{GS}=4.5V, I_D=20A		11.2	14	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		55		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.74	1	V
I_S	Maximum Body-Diode Continuous Current				35	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	920	1150	1380	pF
C_{oss}	Output Capacitance		125	180	235	pF
C_{rss}	Reverse Transfer Capacitance		60	105	150	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.55	1.1	1.65	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A	16	20	24	nC
Q_g(4.5V)	Total Gate Charge		7	9.5	11.4	nC
Q_{gs}	Gate Source Charge			2.7		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		6.5		ns
t_r	Turn-On Rise Time			2		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs	7	8.7	10.5	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs	11	13.5	16	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with TA=25°C.

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.5	mA
		T_J=125°C			100	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.2	1.9	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	140			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		6.9	8.5	mΩ
		T_J=125°C		9.8	12	
		V_{GS}=4.5V, I_D=20A		9.3	12	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.5	0.7	V
I_S	Maximum Body-Diode Continuous Current				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	900	1130	1360	pF
C_{oss}	Output Capacitance		320	465	605	pF
C_{rss}	Reverse Transfer Capacitance		12	40	70	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.35	0.7	1.1	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A	12	16	20	nC
Q_g(4.5V)	Total Gate Charge		6	8	10	nC
Q_{gs}	Gate Source Charge			3		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		6		ns
t_r	Turn-On Rise Time			4		ns
$t_{D(off)}$	Turn-Off DelayTime			19		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs	9	12	15	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs	18	23	28	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

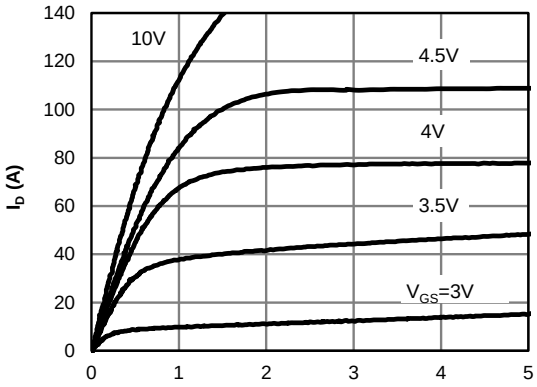


Fig 1: On-Region Characteristics (Note E)

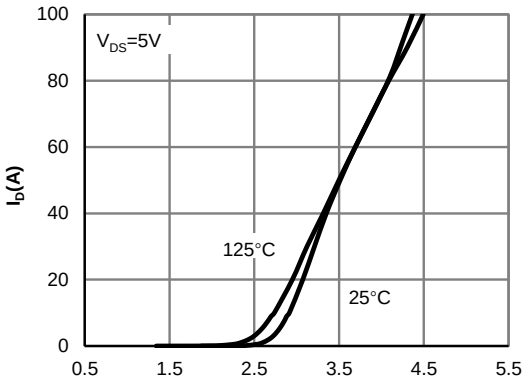


Figure 2: Transfer Characteristics (Note E)

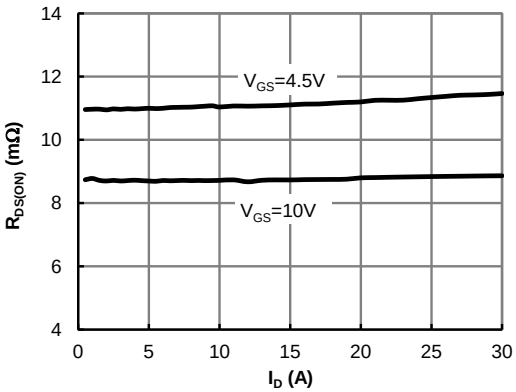


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

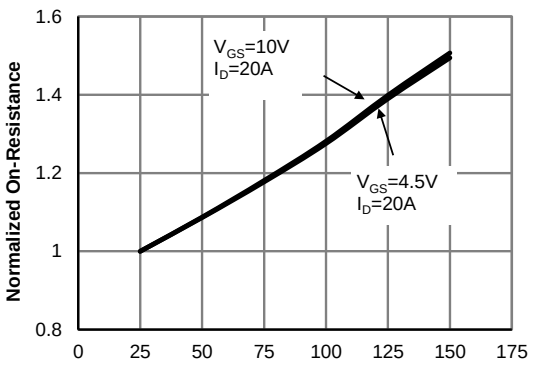


Figure 4: On-Resistance vs. Junction Temperature (Note E)

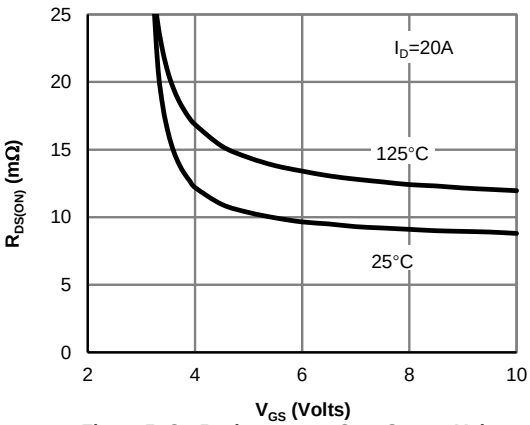


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

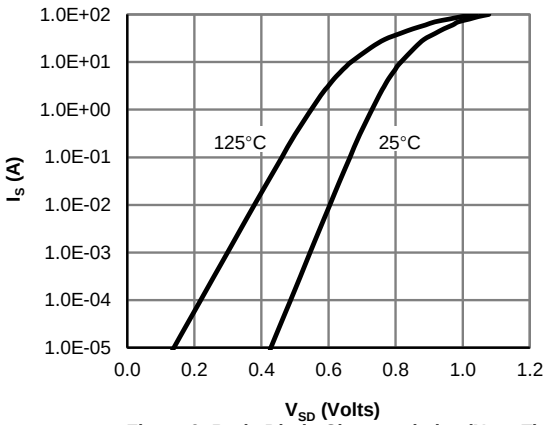


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

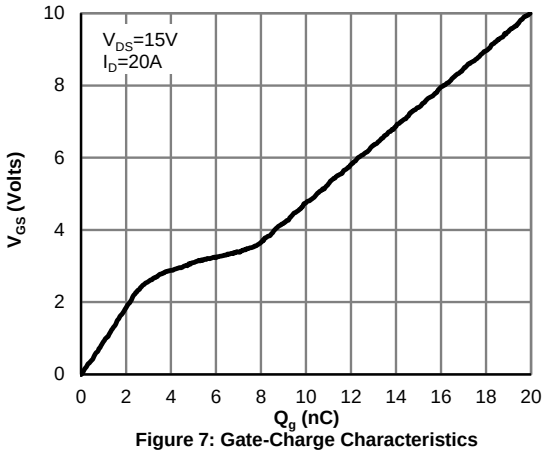


Figure 7: Gate-Charge Characteristics

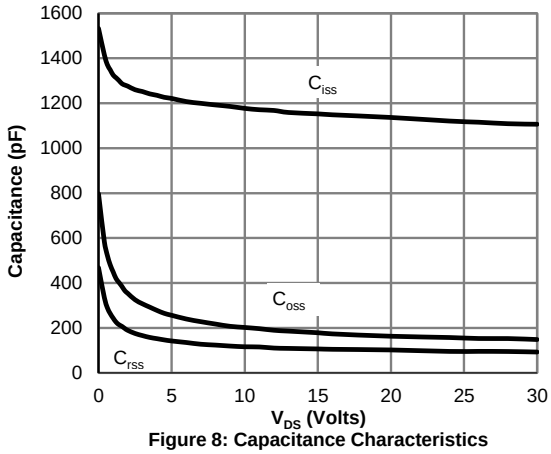


Figure 8: Capacitance Characteristics

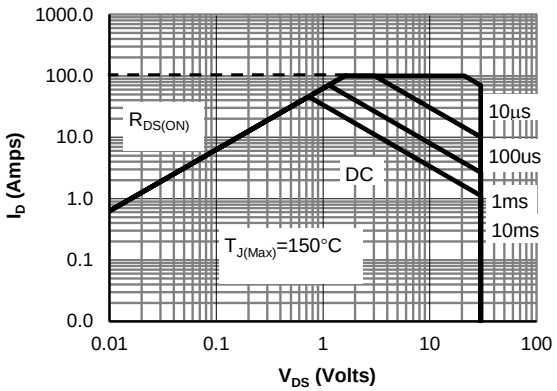


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

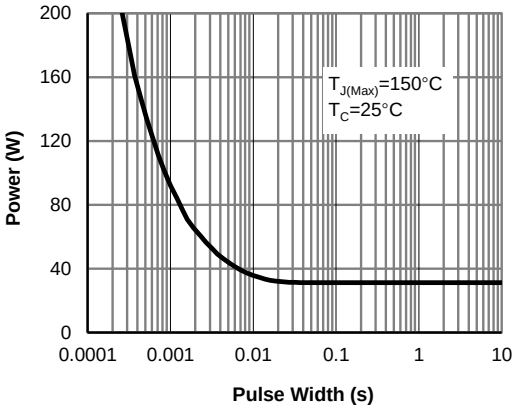


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

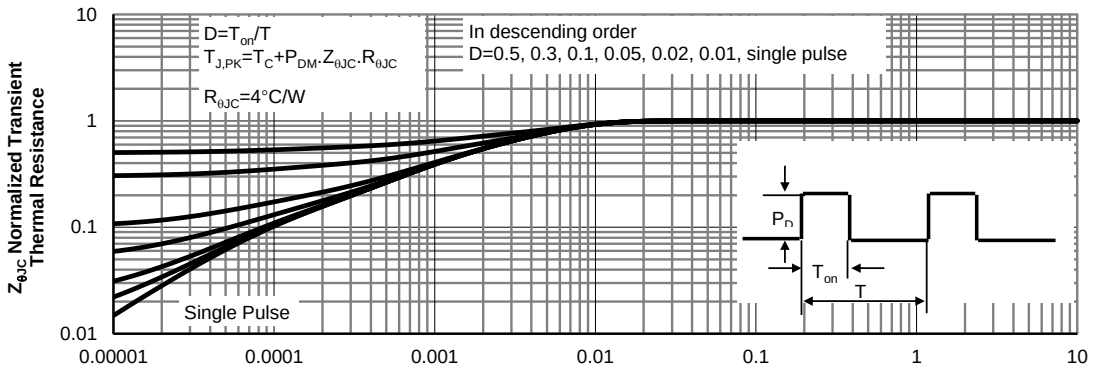


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

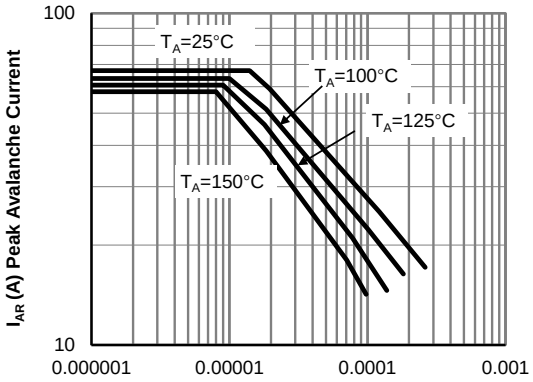


Figure 12: Single Pulse Avalanche capability (Note C)

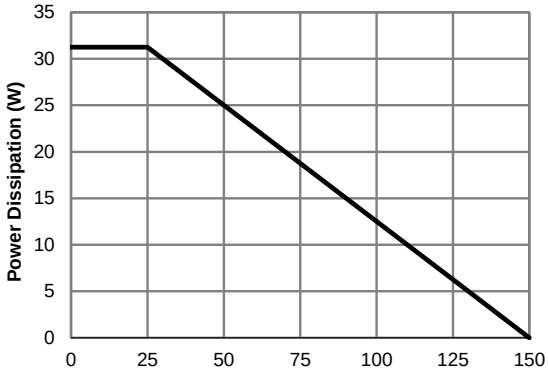


Figure 13: Power De-rating (Note F)

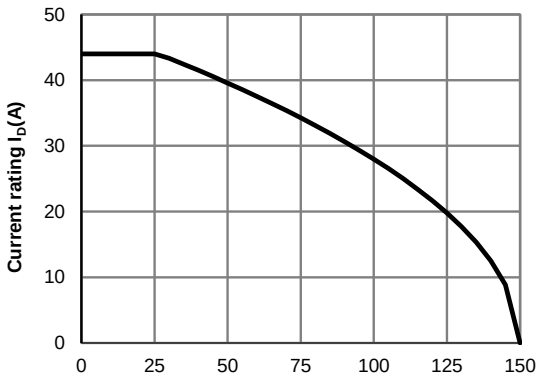


Figure 14: Current De-rating (Note F)

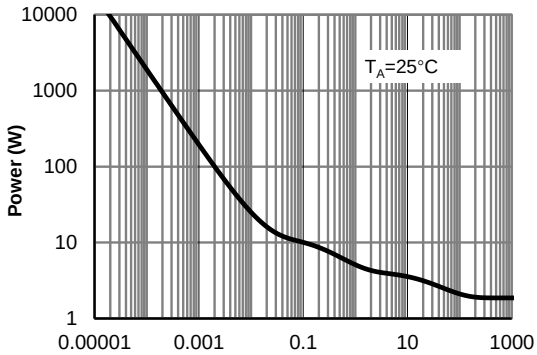


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

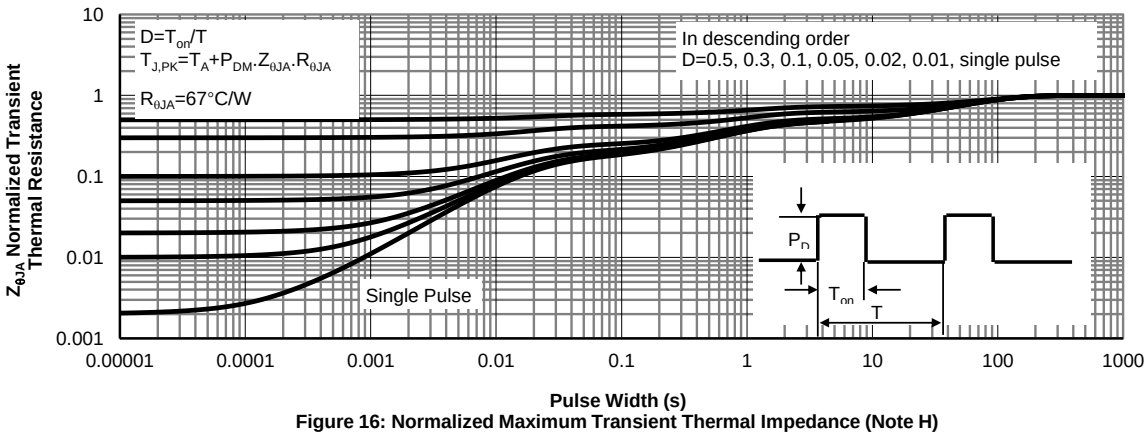


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

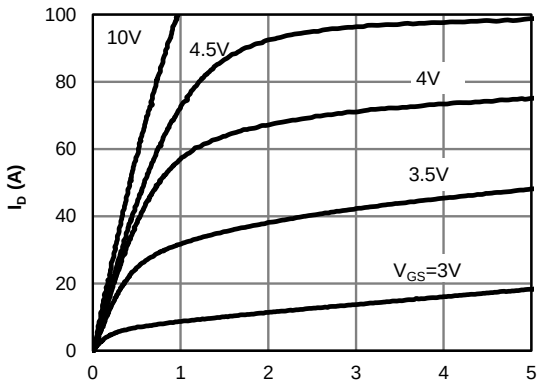


Fig 1: On-Region Characteristics (Note E)

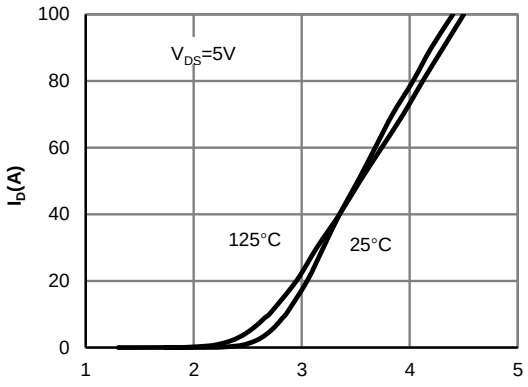


Figure 2: Transfer Characteristics (Note E)

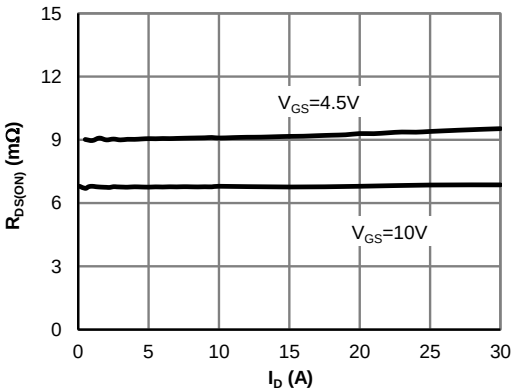


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

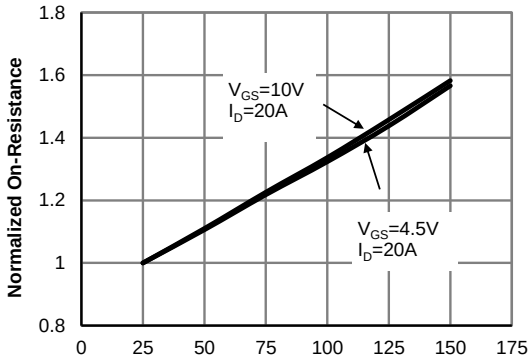


Figure 4: On-Resistance vs. Junction Temperature (Note E)

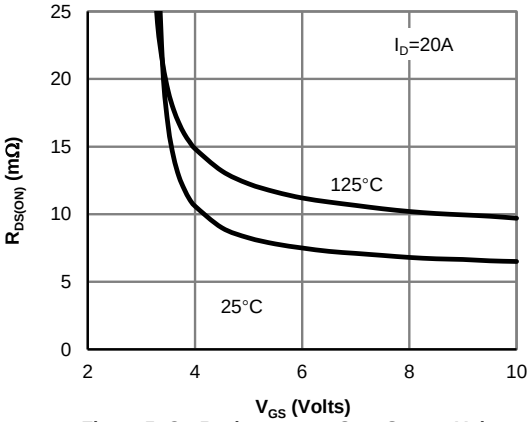


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

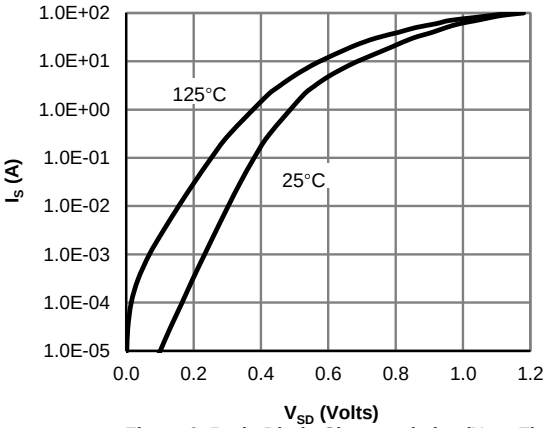


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

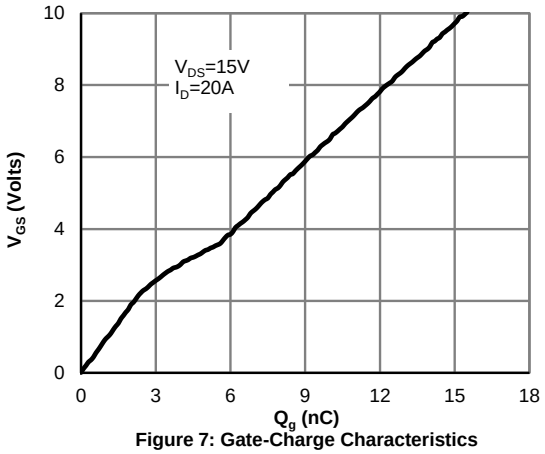


Figure 7: Gate-Charge Characteristics

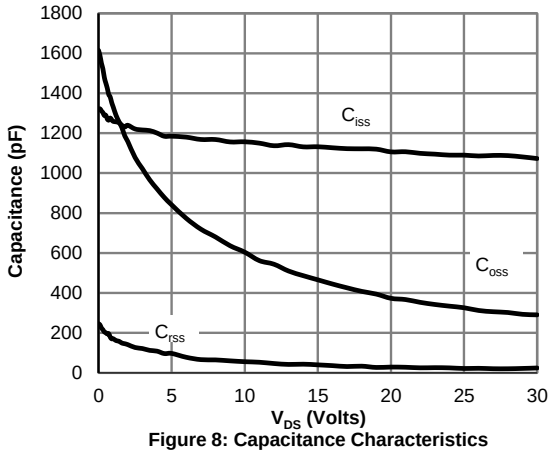


Figure 8: Capacitance Characteristics

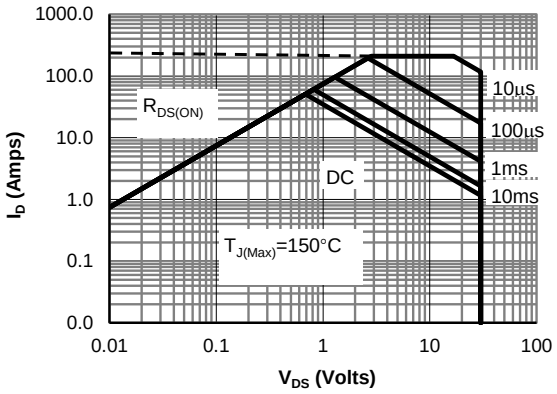


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

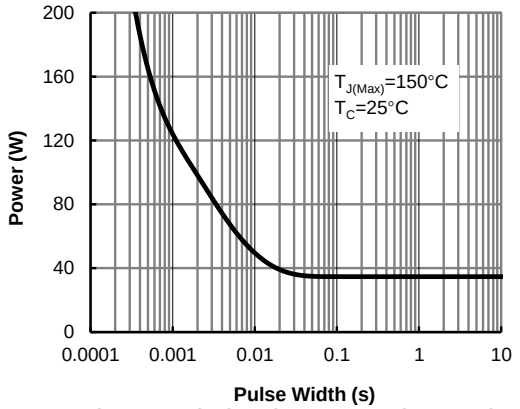


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

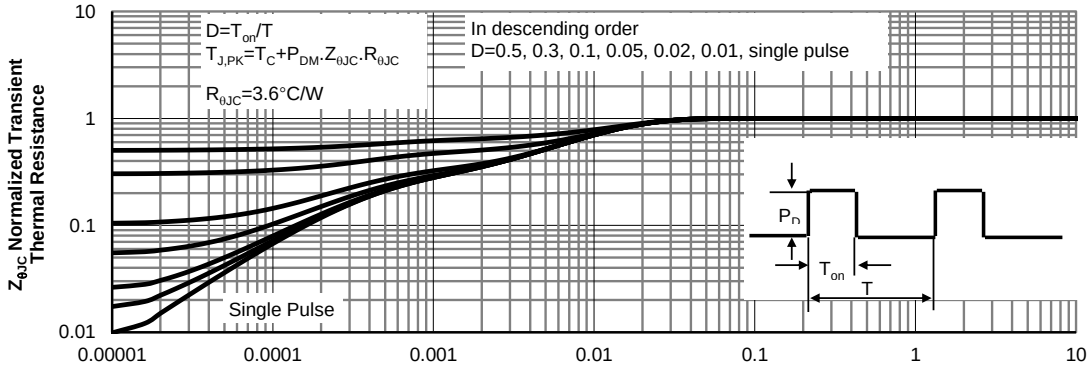


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

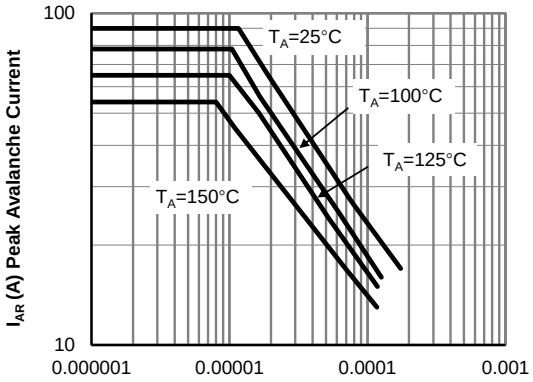


Figure 12: Single Pulse Avalanche capability (Note C)

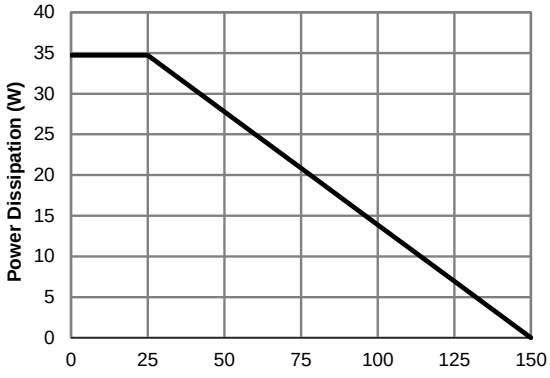


Figure 13: Power De-rating (Note F)

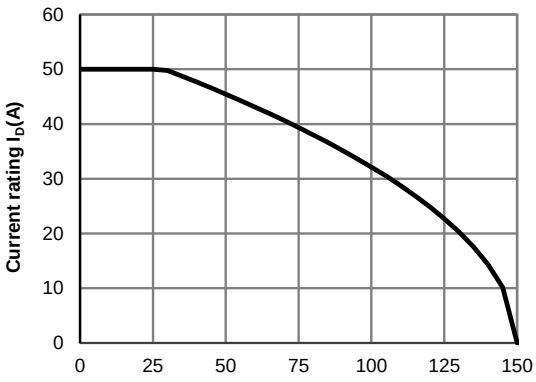


Figure 14: Current De-rating (Note F)

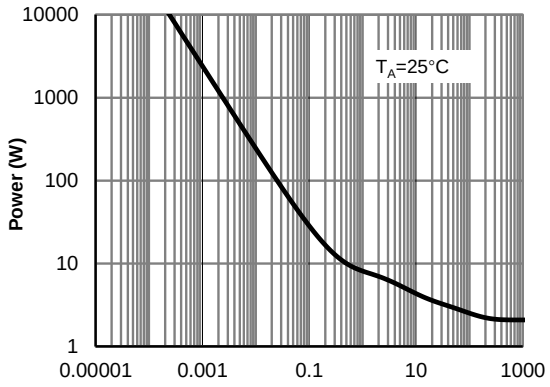


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

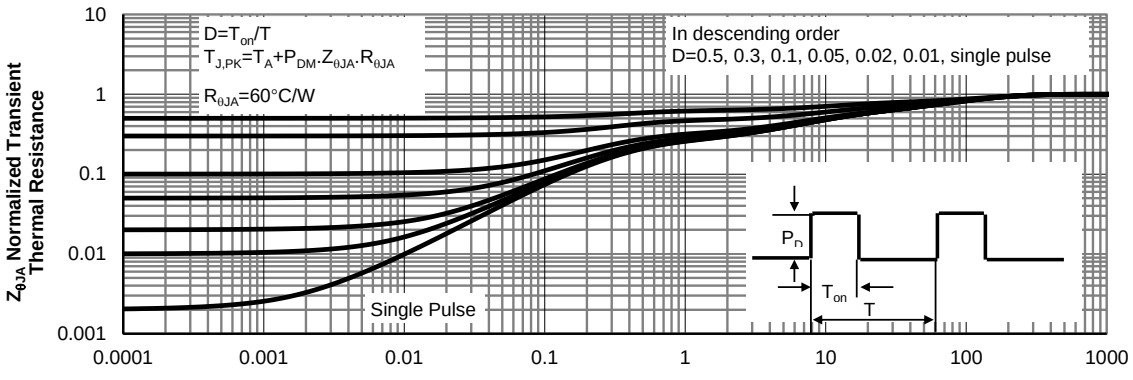
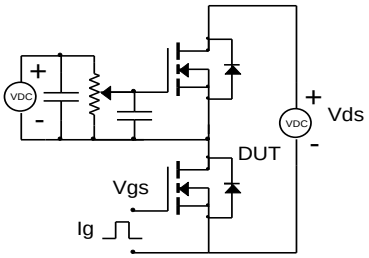
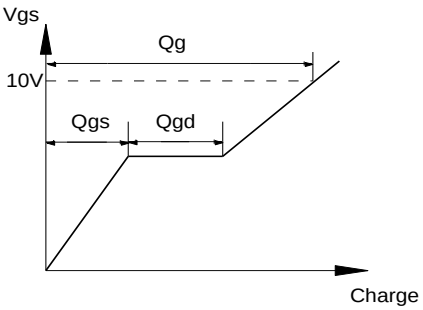


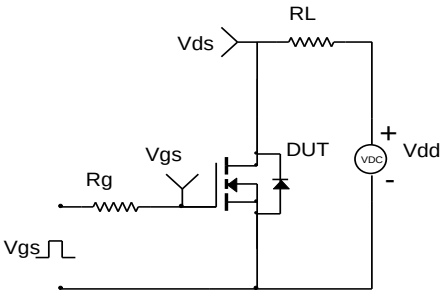
Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

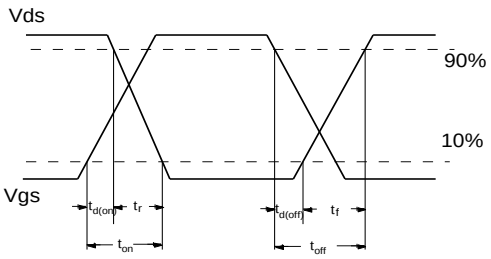
Gate Charge Test Circuit & Waveform



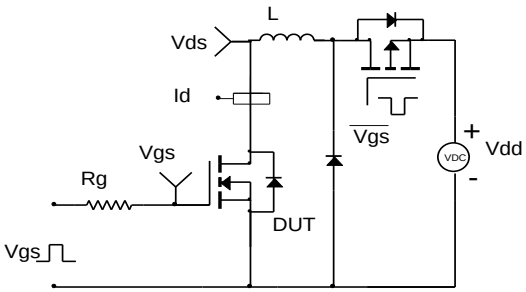


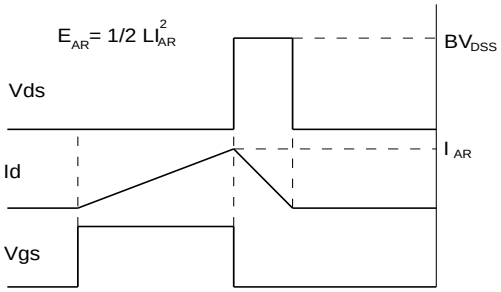
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms