ALPHA & OMEGA SEMICONDUCTOR

# AONC68817

## 80V N-Channel MOSFET

### General Description

- Trench Power AlphaSGT™ technology
- Source Down package with center gate
- Top side cooling
- Low $R_{DS(ON)}$
- Logic level
- Low Gate Charge
- MSL1
- RoHS 2.0 and Halogen-Free Compliant

### Applications

- High-frequency switching applications

### Product Summary

| | |
|---|---|
| $V_{DS}$ | 80V |
| $I_D$ (at $V_{GS}$=10V) | 135A |
| $R_{DS(ON)}$ (at $V_{GS}$=10V) | < 4.4mΩ |
| $R_{DS(ON)}$ (at $V_{GS}$=4.5V) | < 6mΩ |

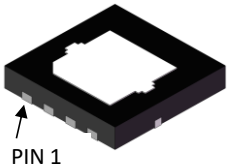
100% UIS Tested
100% Rg Tested

Max Tj=175°C

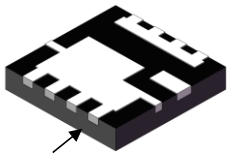
GREEN Product

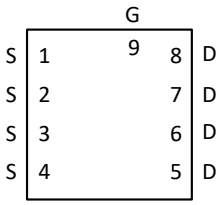
**DFN 3.3x3.3A**

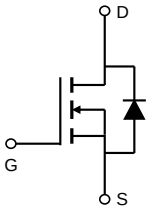
Top View




Bottom View




| Orderable Part Number | Package Type | Form | Minimum Order Quantity |
|---|---|---|---|
| AONC68817 | DFN3.3x3.3A | Tape & Reel | 3000 |

**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 80 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current | $T_C$=25°C | $I_D$ | 135 | A |
| | $T_C$=100°C | | 95 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 540 | |
| Avalanche Current [C] | | $I_{AS}$ | 37 | A |
| Avalanche energy | L=0.1mH [C] | $E_{AS}$ | 68 | mJ |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 170 | W |
| | $T_C$=100°C | | 85 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 175 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 20 | 25 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 35 | 45 | °C/W |
| Maximum Junction-to-Case,top | Steady-State | $R_{\theta JC}$ | 0.83 | 0.88 | °C/W |
| Maximum Junction-to-Case,bottom | Steady-State | $R_{\theta JC}$ | 0.67 | 0.75 | °C/W |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 80 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=80V, $V_{GS}$=0V | | | 1 | µA |
| | | $T_J$=55°C | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250µA | 1.6 | 2.1 | 2.6 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=20A | | 3.6 | 4.4 | mΩ |
| | | $T_J$=125°C | | 6.3 | 7.6 | |
| | | $V_{GS}$=4.5V, $I_D$=20A | | 4.8 | 6 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=20A | | 97 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A, $V_{GS}$=0V | | 0.7 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | 135 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=40V, f=1MHz | | 2360 | | pF |
| $C_{oss}$ | Output Capacitance | | | 680 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 15 | | pF |
| $R_g$ | Gate resistance | f=1MHz | 0.3 | 0.65 | 1.3 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=40V, $I_D$=20A | | 31 | 45 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 14 | 20 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 7 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 5 | | nC |
| $Q_{oss}$ | Output Charge | $V_{GS}$=0V, $V_{DS}$=40V | | 46 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=40V, $R_L$=2.0Ω, $R_{GEN}$=3Ω | | 9 | | ns |
| $t_r$ | Turn-On Rise Time | | | 3.6 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 27 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 4 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=20A, di/dt=100A/µs | | 28 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=20A, di/dt=100A/µs | | 20 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

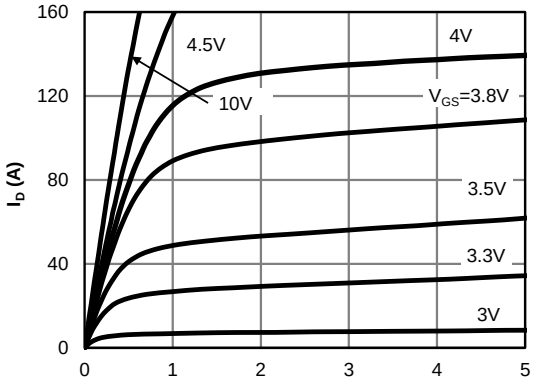



**Figure 1: On-Region Characteristics (Note E)**

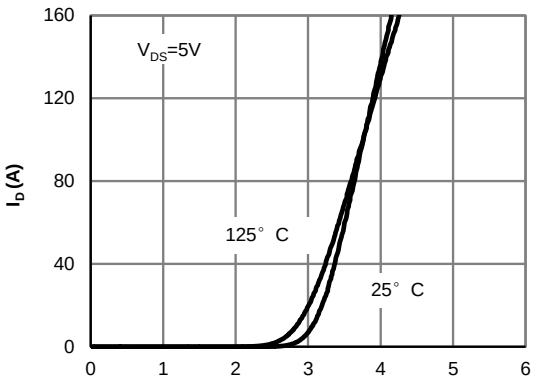



**Figure 2: Transfer Characteristics (Note E)**

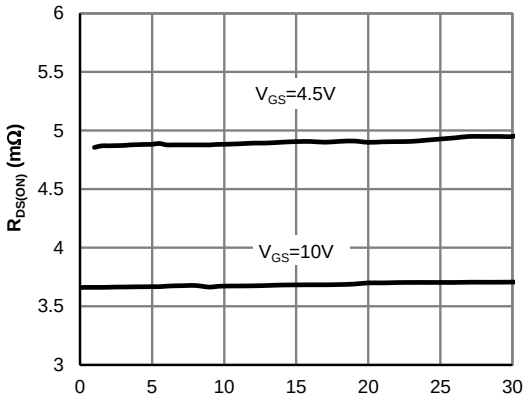



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

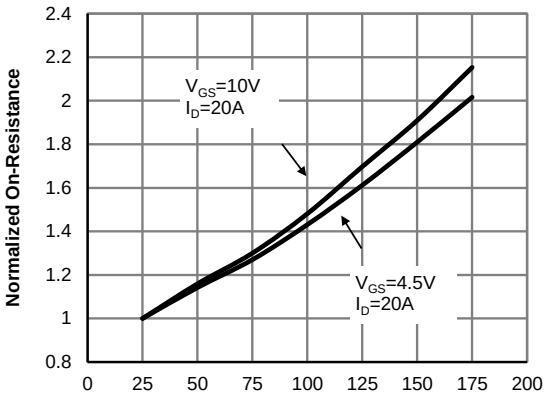



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

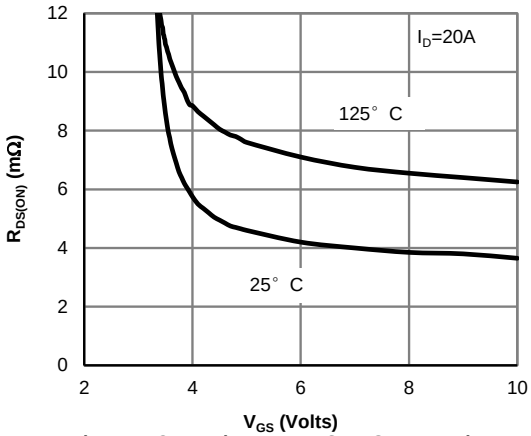



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

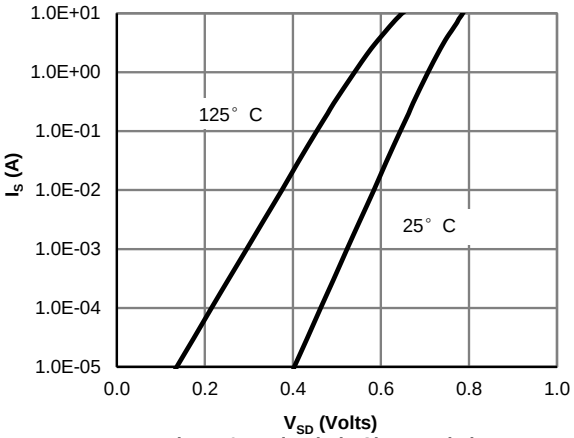



**Figure 6: Body-Diode Characteristics (Note E)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

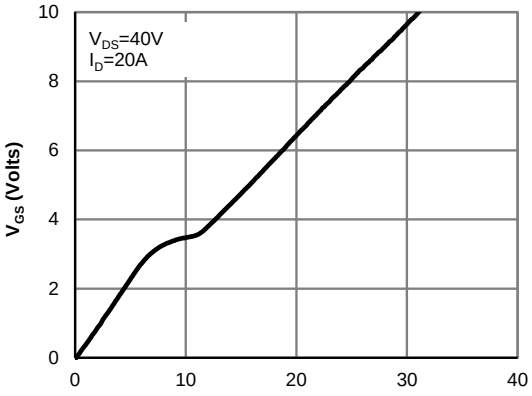



**Figure 7: Gate-Charge Characteristics**

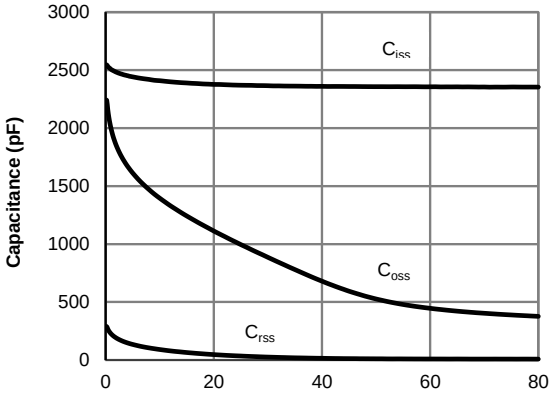



**Figure 8: Capacitance Characteristics**

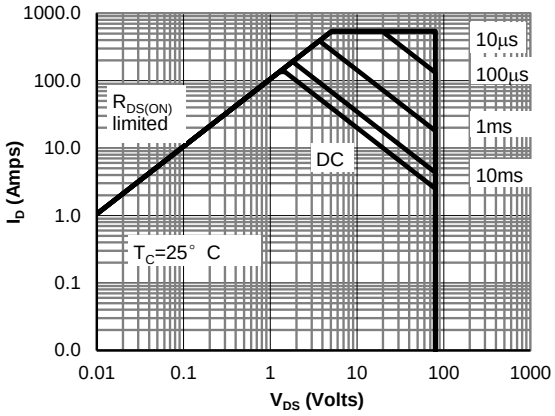



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

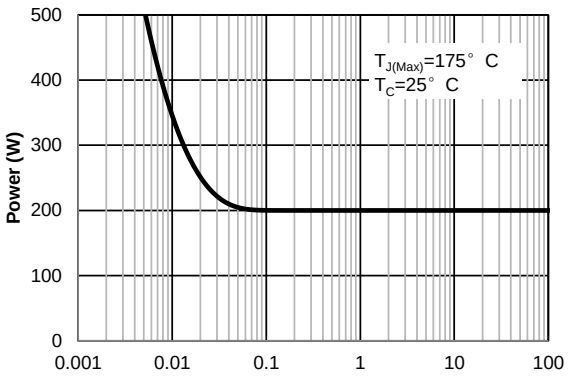



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

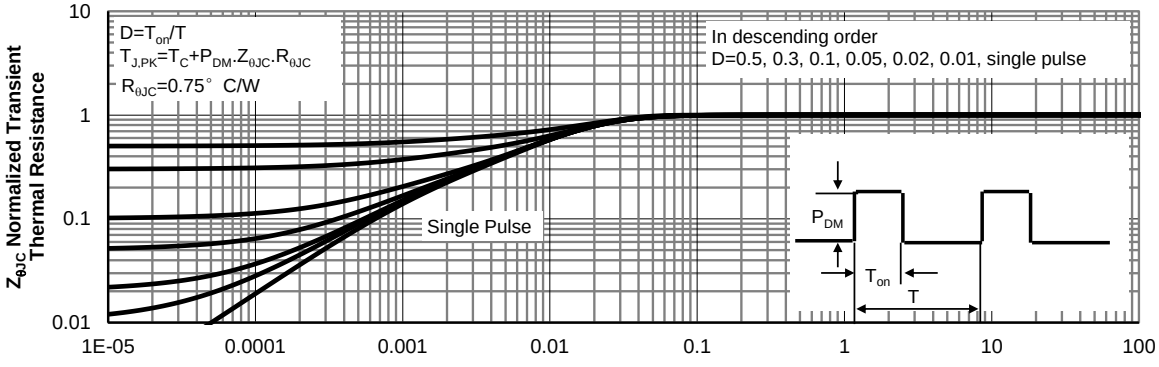



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

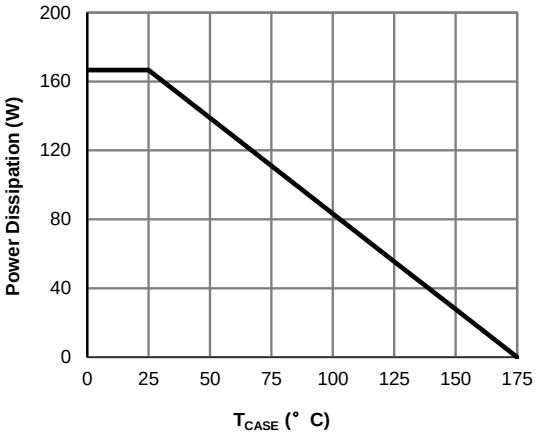



**Figure 12: Power De-rating (Note F)**

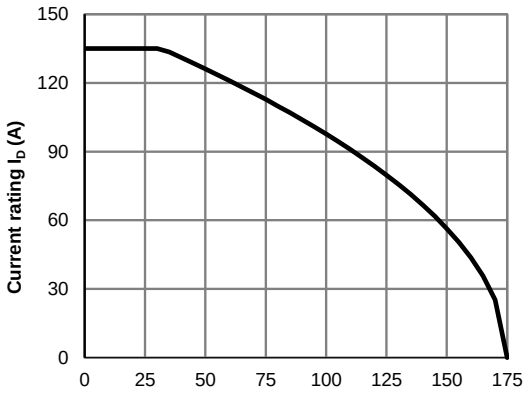



**Figure 13: Current De-rating (Note F)**

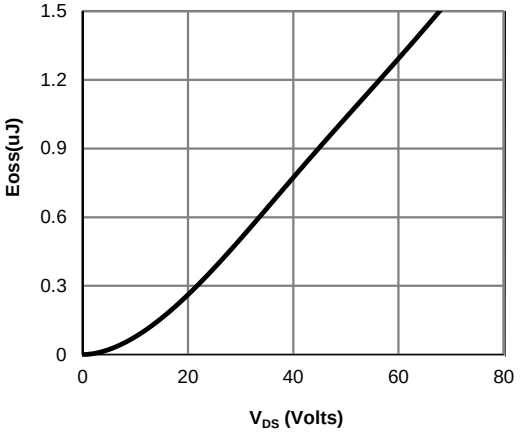



**Figure 14: Coss stored Energy**

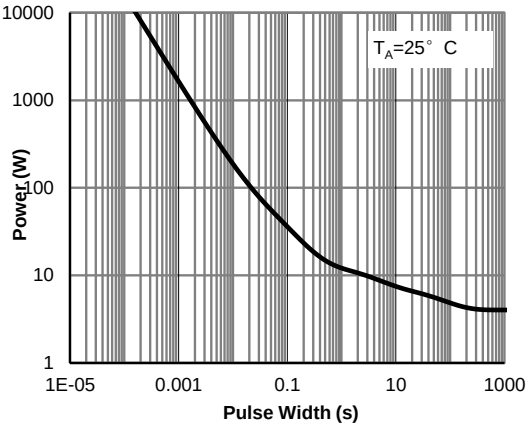



**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

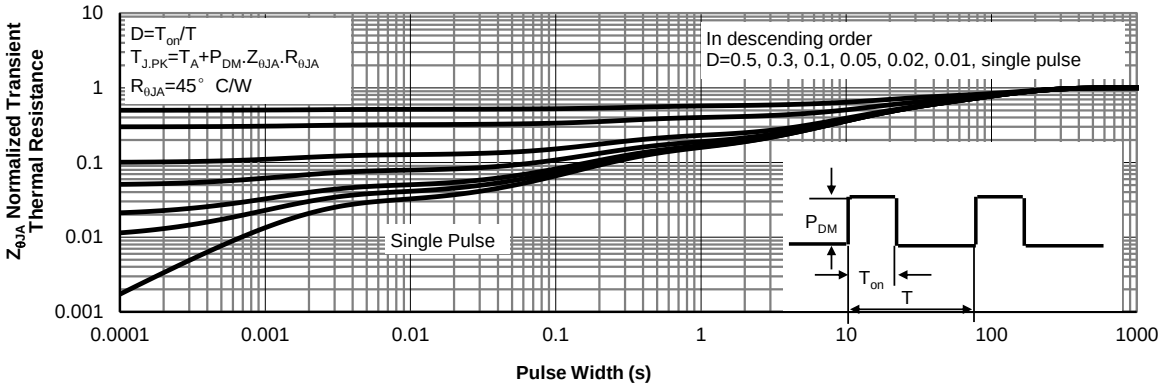



**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

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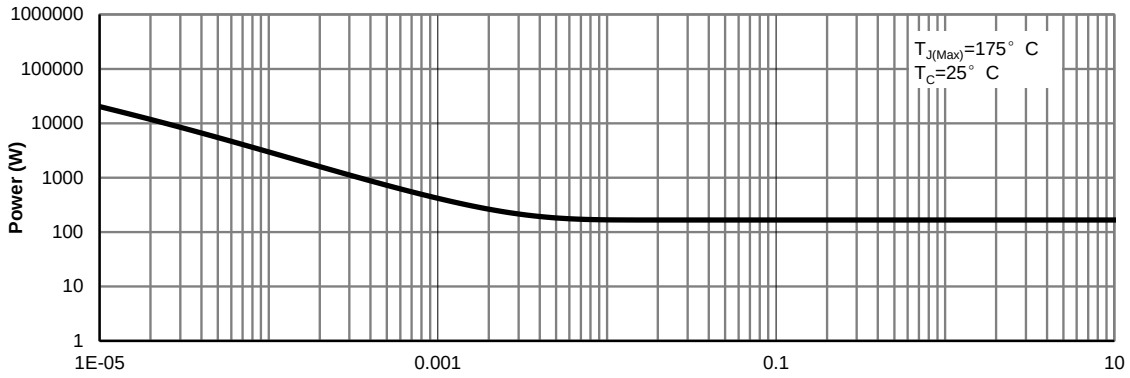



**Figure 17: Single Pulse Power Rating Junction-to-Case-Top (Note F)**

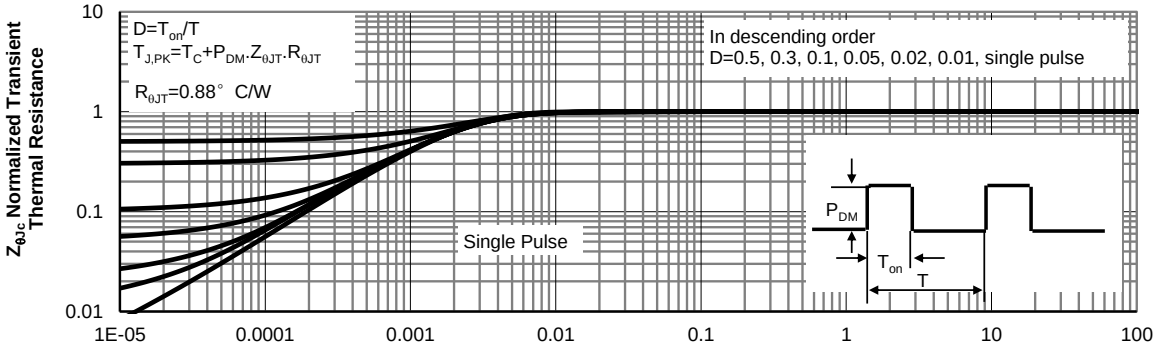



**Figure 18: Normalized Maximum Transient Thermal Impedance-Top (Note F)**

Figure A: Gate Charge Test Circuit & Waveforms

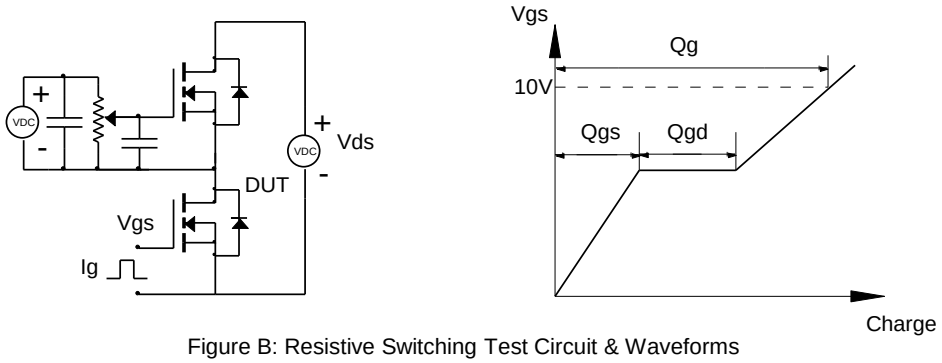



Figure B: Resistive Switching Test Circuit & Waveforms

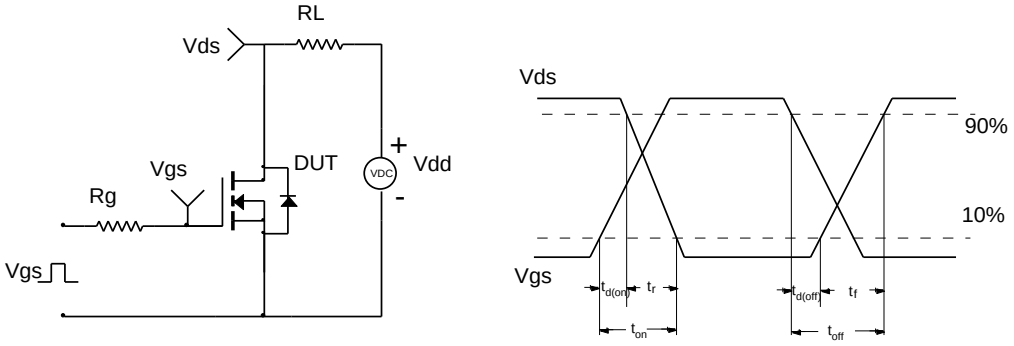



Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

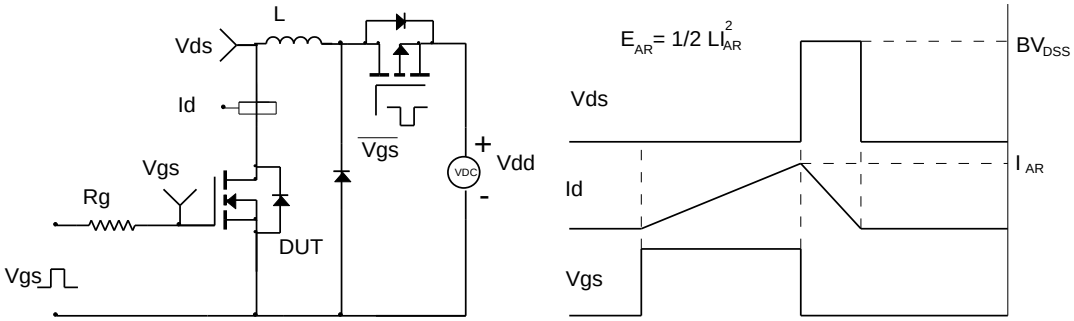



Figure D: Diode Recovery Test Circuit & Waveforms

