

### General Description

- AlphaSGT™ N-Channel Power MOSFET technology
- Source down package with center gate
- Low  $R_{DS(ON)}$
- Logic level
- Low Gate Charge
- High Current Capability
- RoHS 2.0 and Halogen-Free Compliant

### Applications

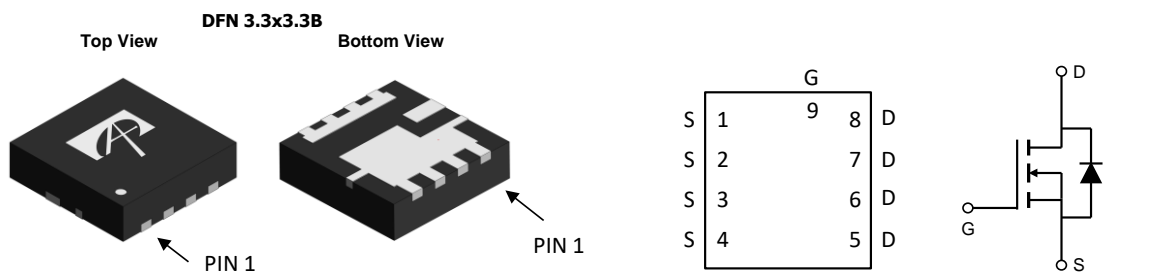
- Synchronous Rectification
- OR-ing FET

### Product Summary

$V_{DS}$	25V
$I_D$ (at $V_{GS}=10V$ )	345A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 0.69m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=7V$ )	< 0.85m $\Omega$

100% UIS Tested  
 100% Rg Tested

Max  $T_j=175^{\circ}C$



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONK40206	DFN3.3x3.3B	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 16$	V
Continuous Drain Current	$I_D$	$T_C=25^{\circ}C$	345
		$T_C=100^{\circ}C$	245
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	1380	A
Avalanche Current <sup>C</sup>	$I_{AS}$	60	A
Avalanche energy $L=0.01mH$ <sup>C</sup>	$E_{AS}$	18	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^{\circ}C$	136
		$T_C=100^{\circ}C$	68
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^{\circ}C$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	20	25	$^{\circ}C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		35	45	$^{\circ}C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	-	1.1	$^{\circ}C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	25			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±16V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.05	1.65	2.25	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		0.57	0.69	mΩ
		V <sub>GS</sub> =7V, I <sub>D</sub> =20A		0.75	0.92	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		130		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.67	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				160	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =12.5V, f=1MHz		4460		pF
C <sub>oss</sub>	Output Capacitance			1660		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			190		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.4	0.85	1.3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =12.5V, I <sub>D</sub> =20A		56	80	nC
Q <sub>g(7V)</sub>	Total Gate Charge			38	55	
Q <sub>gs</sub>	Gate Source Charge			15.5		
Q <sub>gd</sub>	Gate Drain Charge			4.1		
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =12.5V, R <sub>L</sub> =0.625Ω, R <sub>GEN</sub> =3Ω		9.7		ns
t <sub>r</sub>	Turn-On Rise Time			16		
t <sub>D(off)</sub>	Turn-Off DelayTime			41		
t <sub>f</sub>	Turn-Off Fall Time			10		
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, di/dt=100A/μs		36		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, di/dt=100A/μs		27		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

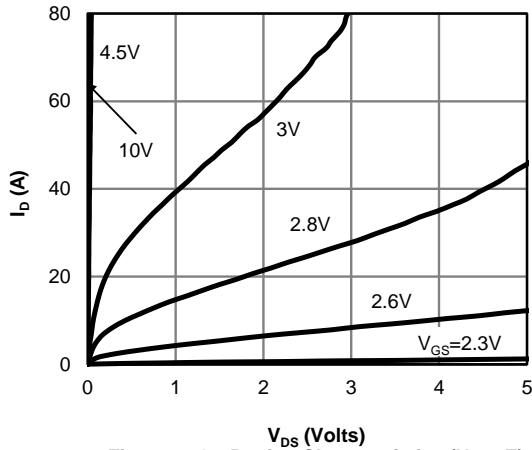
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

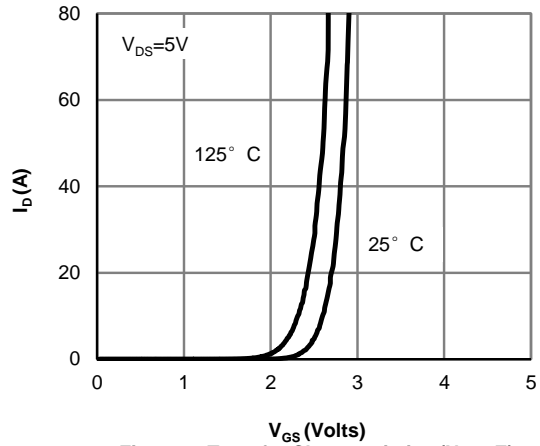
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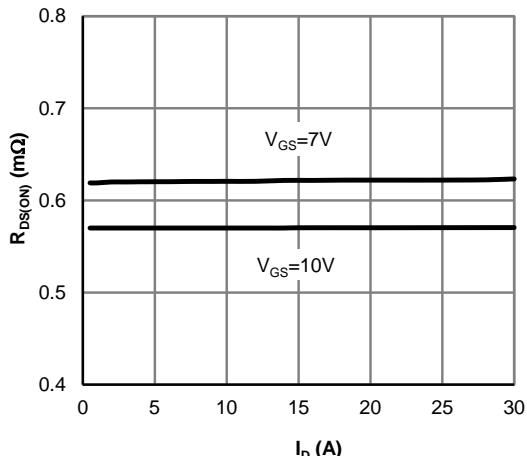
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



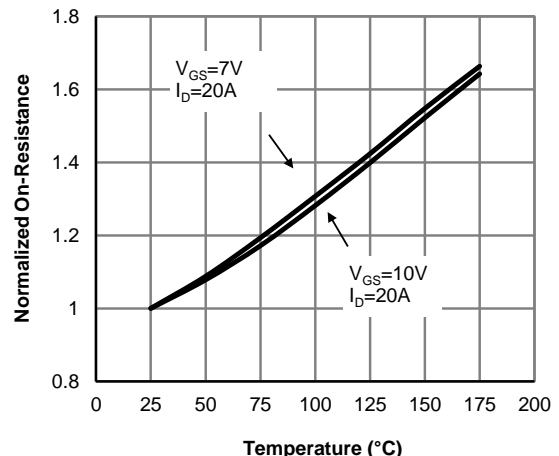
**Figure 1: On-Region Characteristics (Note E)**



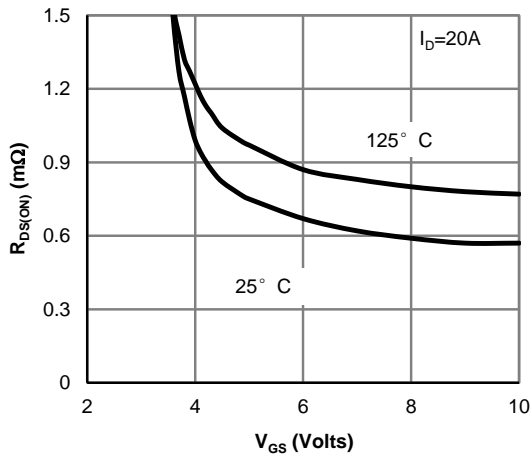
**Figure 2: Transfer Characteristics (Note E)**



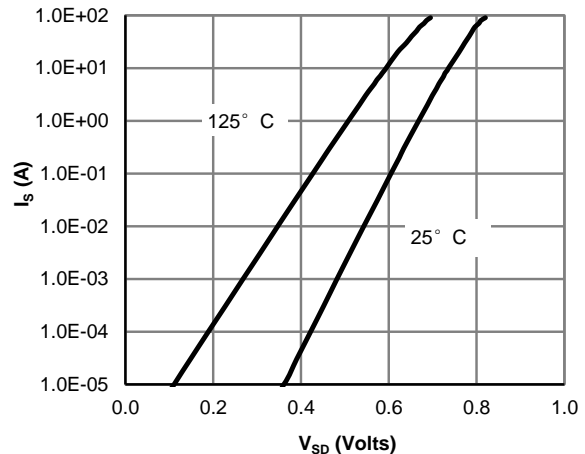
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

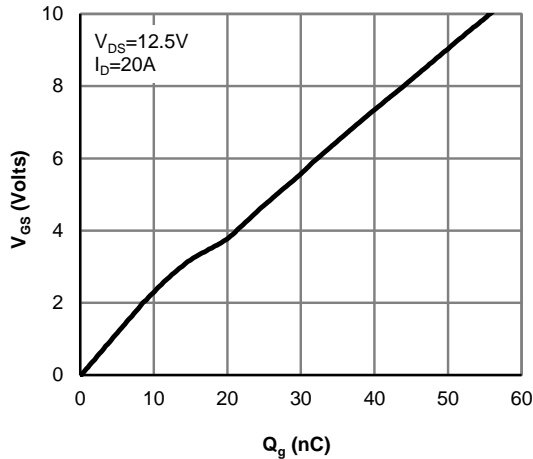


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

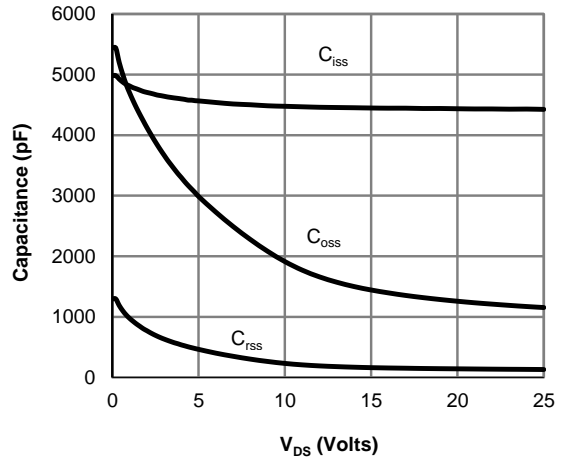


**Figure 6: Body-Diode Characteristics (Note E)**

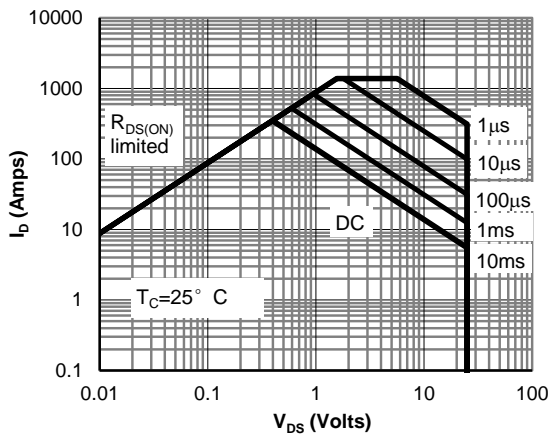
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



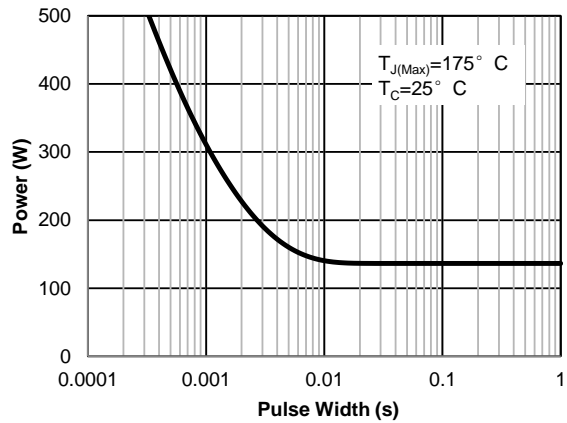
**Figure 7: Gate-Charge Characteristics**



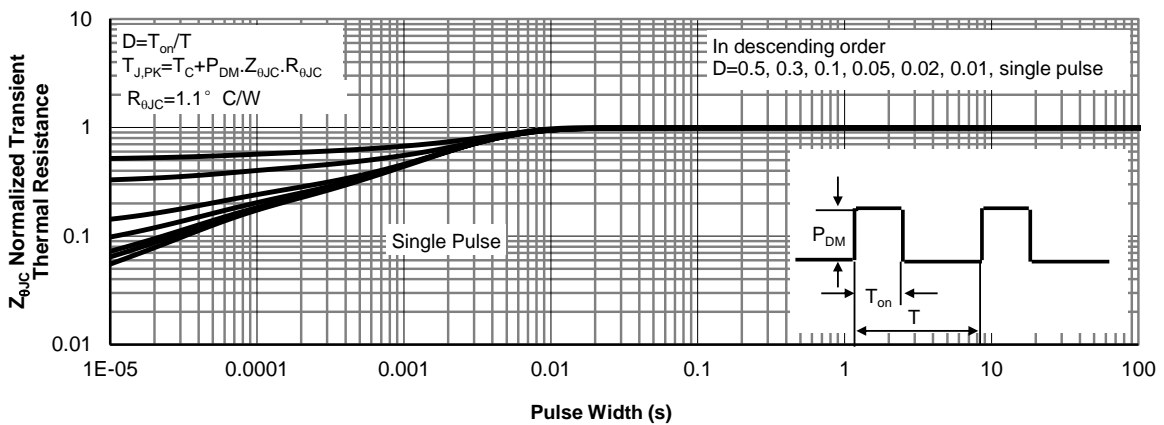
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

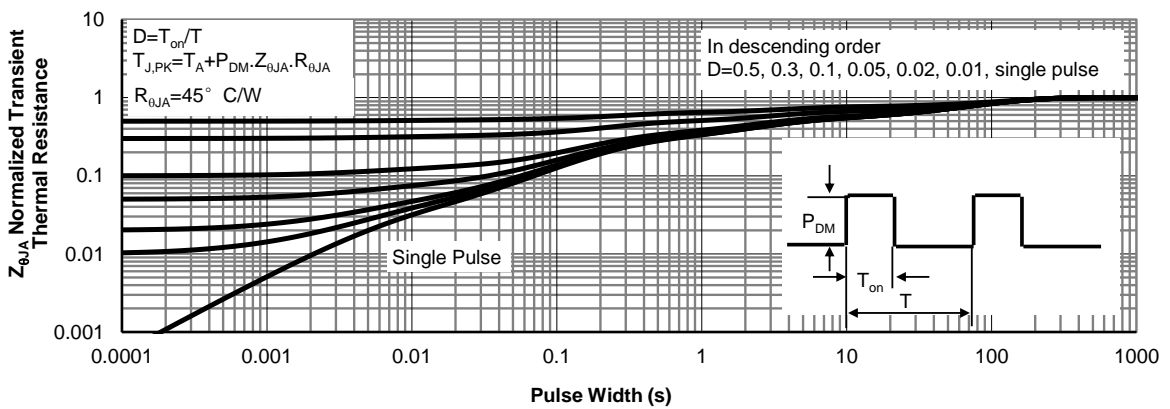
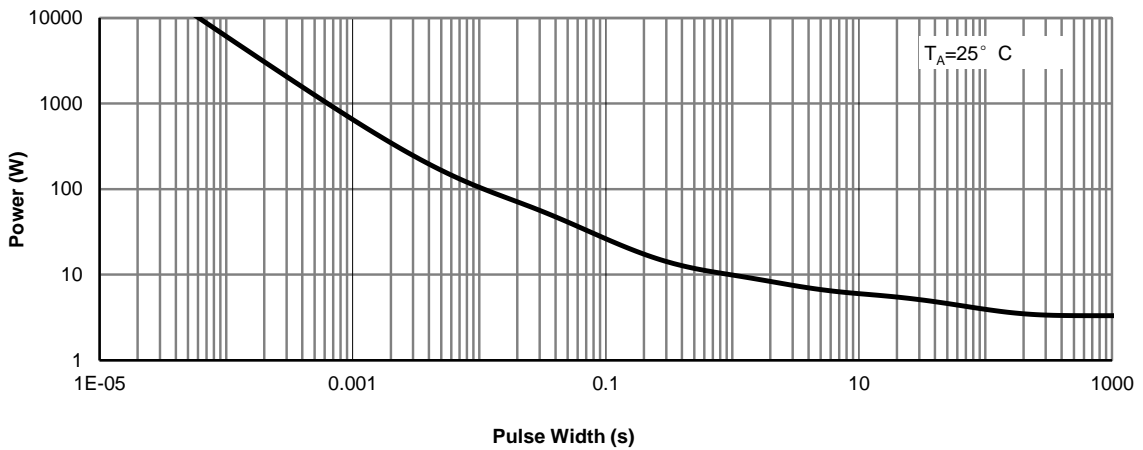
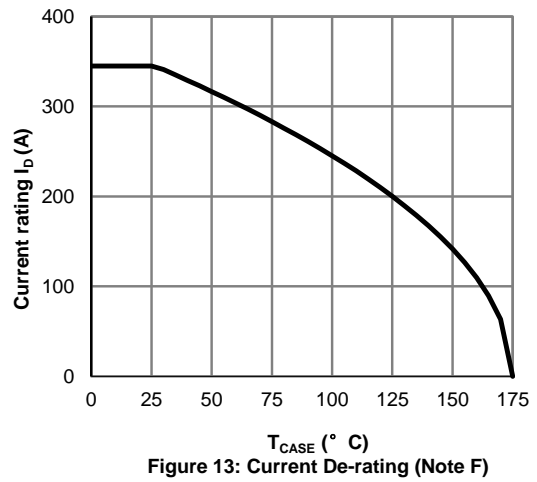
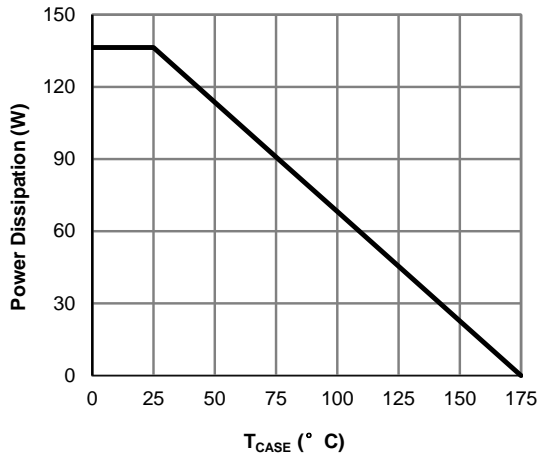


Figure A: Gate Charge Test Circuit & Waveforms

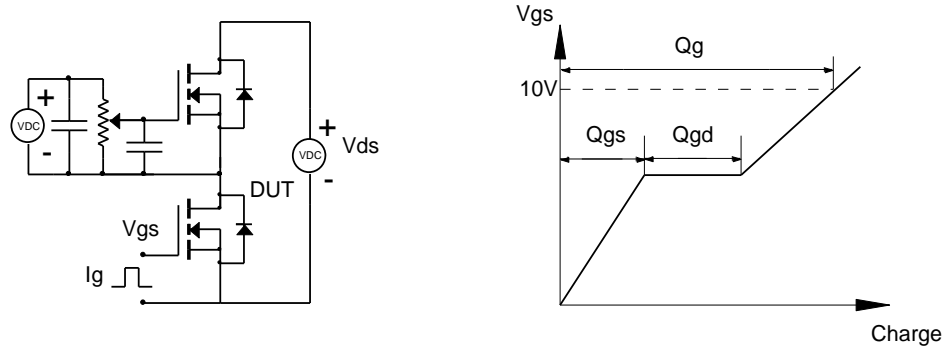


Figure B: Resistive Switching Test Circuit & Waveforms

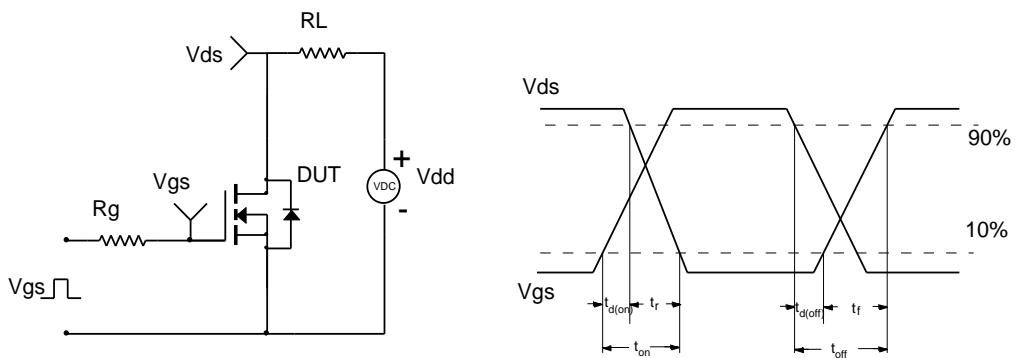


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

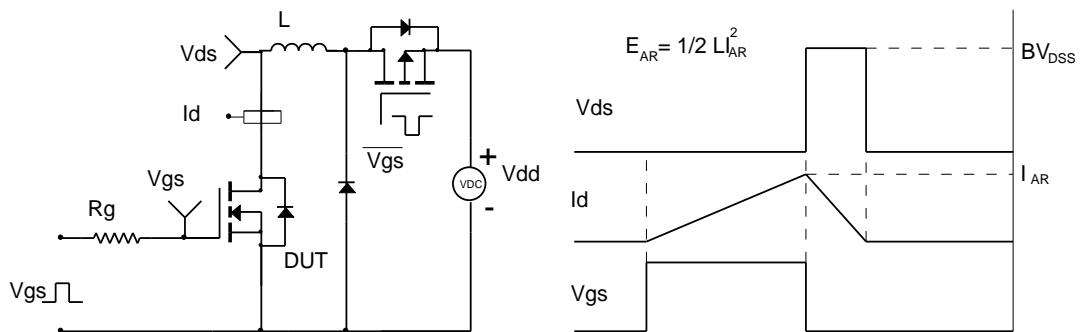


Figure D: Diode Recovery Test Circuit & Waveforms

