AONL32328

30V Complementary MOSFET

General Description

- Pch+Nch Complementary MOSFET
- Trench Power MOSFET
- Low $R_{DS(ON)}$
- Low Gate Charge
- Excellent Thermal Performance
- RoHS and Halogen Free Compliant

Product Summary

P-channel(Q1/Q3)	N-channel(Q2/Q4)	
V_{DS} (V) = -30V	V_{DS} (V) = 30V	
I_D = -7A	I_D = 8A	(V_{GS} = ±10V)
$R_{DS(ON)}$ < 27mΩ	$R_{DS(ON)}$ < 21mΩ	(V_{GS} = ±10V)
$R_{DS(ON)}$ < 45mΩ	$R_{DS(ON)}$ < 32mΩ	(V_{GS} = ±4.5V)

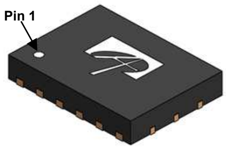
100% UIS Tested
100% Rg Tested

Applications

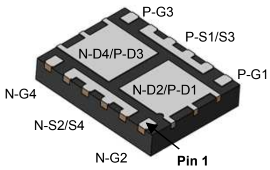
- Motor Drive
- DC-FAN

DFN4x3A_12L

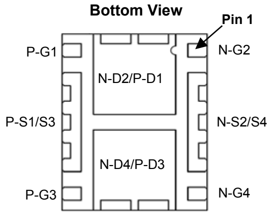
Top View

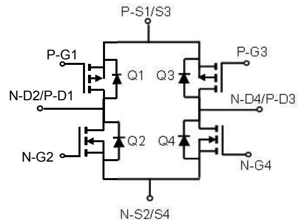


Bottom View



Bottom View





Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONL32328	DFN 4x3A	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max P-Channel Q1/Q3	Max N-Channel Q2/Q4	Units
Drain-Source Voltage		V_{DS}	-30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_A=25°C	I_D	-7	8	A
	T_A=70°C		-6	7	
Pulsed Drain Current [C]		I_{DM}	-28	32	
Avalanche Current [C]		I_{AS}	-18	12	A
Avalanche energy L=0.1mH [C]		E_{AS}	16	7	mJ
Power Dissipation [B]	T_A=25°C	P_D	2.6	2.6	W
	T_A=70°C		1.6	1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1/Q3	Typ Q2/Q4	Max Q1/Q3	Max Q2/Q4	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	48	60	60	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		75	75	90	90	°C/W

Q1/Q3 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V		-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V				-1	µA
			T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=-250µA		-1.3	-1.85	-2.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-7A			22	27	mΩ
			T_J=125°C		32	40	
		V_{GS}=-4.5V, I_D=-5A			35.5	45	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-7A			18		S
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V			-0.75	-1	V
I_S	Maximum Body-Diode Continuous Current					3	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz			730		pF
C_{oss}	Output Capacitance				140		pF
C_{rss}	Reverse Transfer Capacitance				90		pF
R_g	Gate resistance	f=1MHz			2.1	5	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-7A			12	24	nC
Q_g(4.5V)	Total Gate Charge				5.6	12	nC
Q_{gs}	Gate Source Charge				1.8		nC
Q_{gd}	Gate Drain Charge				3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=2.15Ω, R_{GEN}=3Ω			7.5		ns
t_r	Turn-On Rise Time				8.5		ns
$t_{D(off)}$	Turn-Off DelayTime				15		ns
t_f	Turn-Off Fall Time				4.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-7A, di/dt=500A/µs			9		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-7A, di/dt=500A/µs			17		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300ms pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

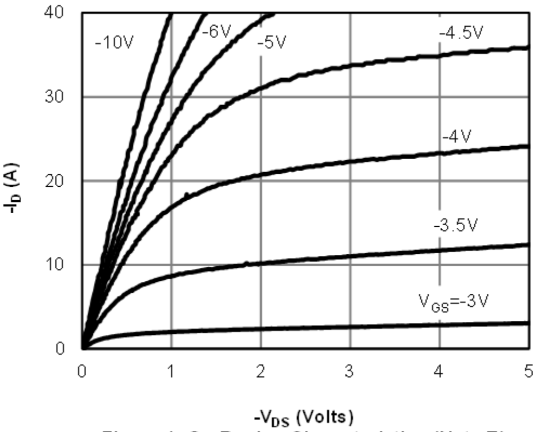


Figure 1: On-Region Characteristics (Note E)

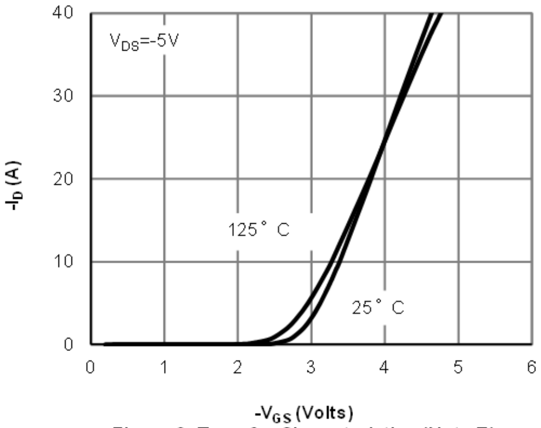


Figure 2: Transfer Characteristics (Note E)

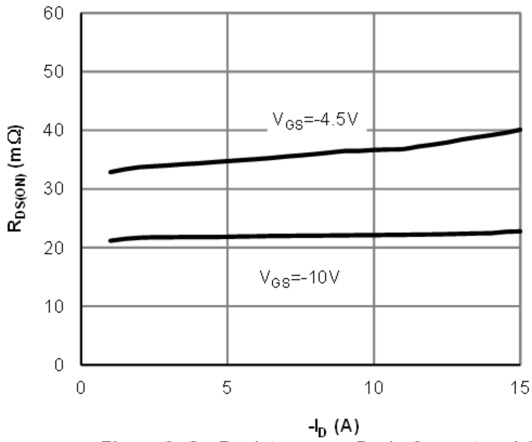


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

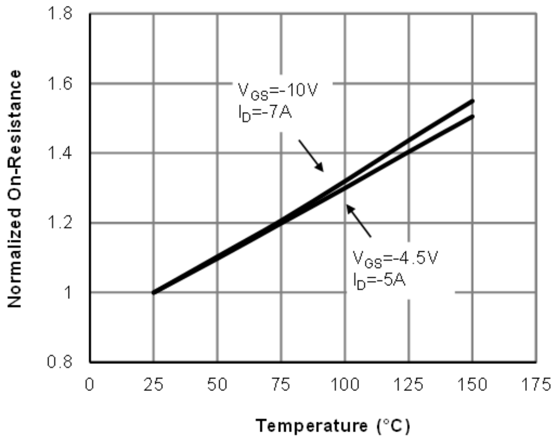


Figure 4: On-Resistance vs. Junction Temperature (Note E)

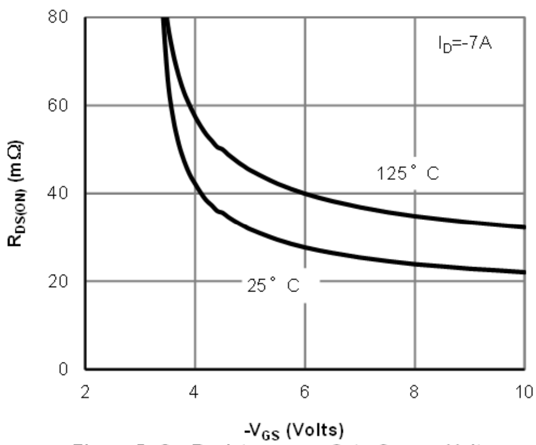


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

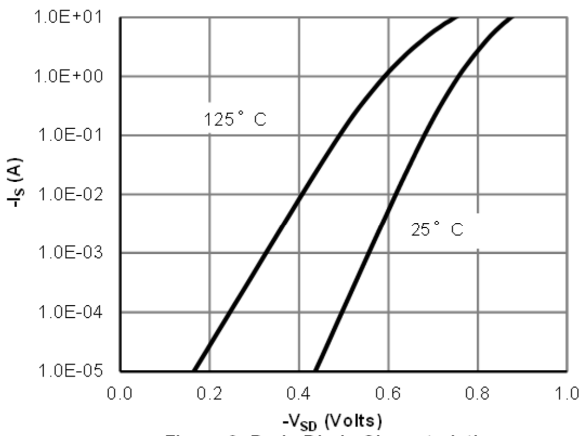


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

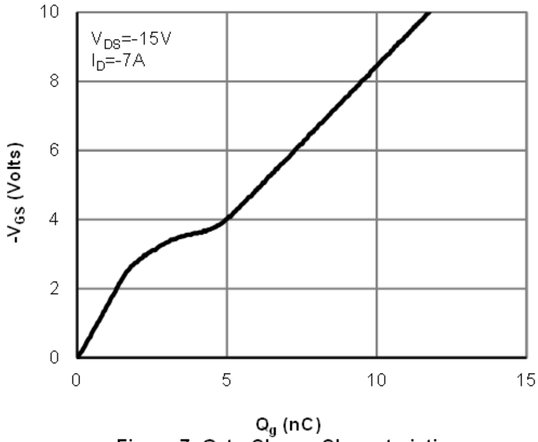


Figure 7: Gate-Charge Characteristics

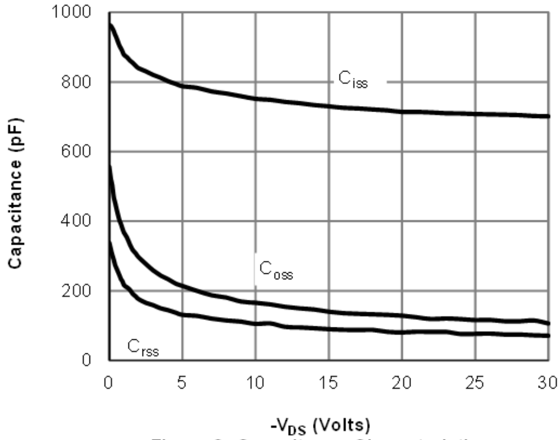
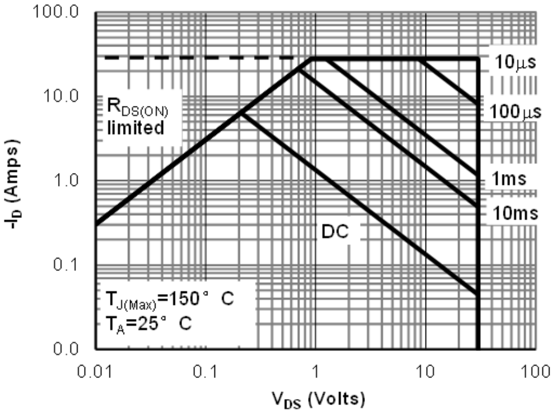


Figure 8: Capacitance Characteristics



$-V_{GS}$> or equal to -4.5V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

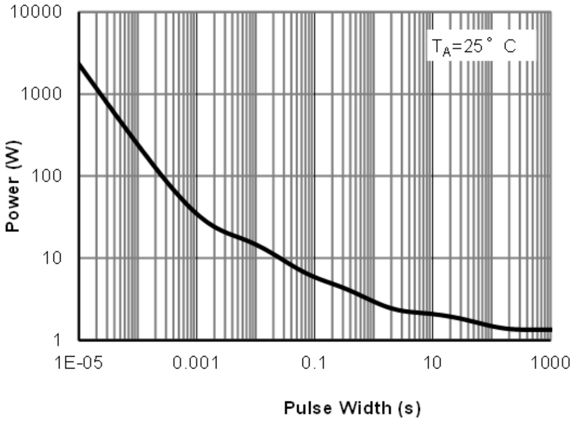


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note F)

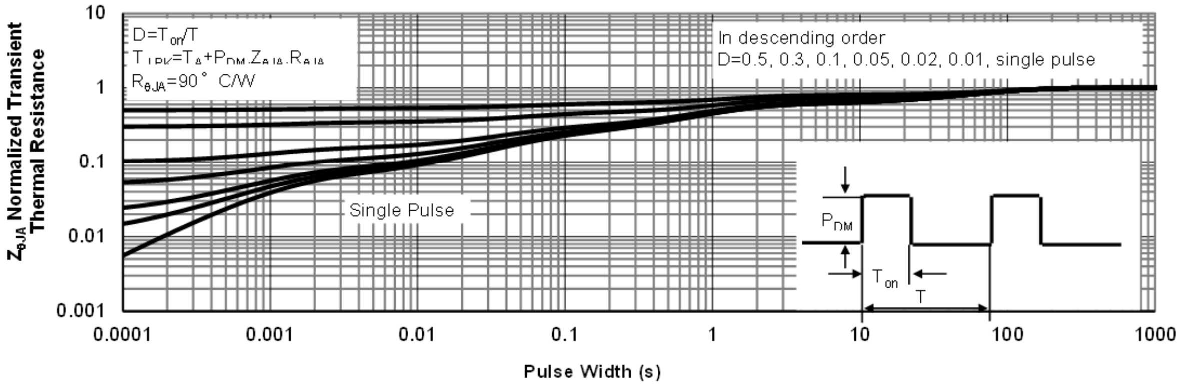


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2/Q4 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA	1.5	2.1	2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8A		17	21	mΩ
		T_J=125°C		25	31	
		V_{GS}=4.5V, I_D=5A		24.5	32	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=8A		20		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.75	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		395		pF
C_{oss}	Output Capacitance			67		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_g	Gate resistance	f=1MHz	0.9	1.8	2.8	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=8A		6.6	15	nC
Q_g(4.5V)	Total Gate Charge			3	7	nC
Q_{gs}	Gate Source Charge			1.1		nC
Q_{gd}	Gate Drain Charge			1.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.80Ω, R_{GEN}=3Ω		5		ns
t_r	Turn-On Rise Time			3		ns
$t_{D(off)}$	Turn-Off DelayTime			15		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=8A, di/dt=500A/µs		7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=8A, di/dt=500A/µs		8		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in[2] FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.
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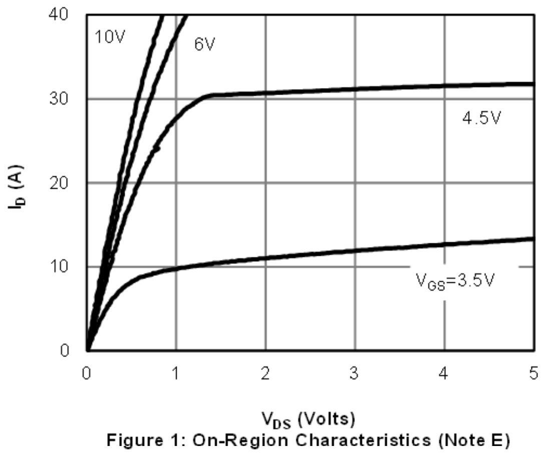
F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in[2] FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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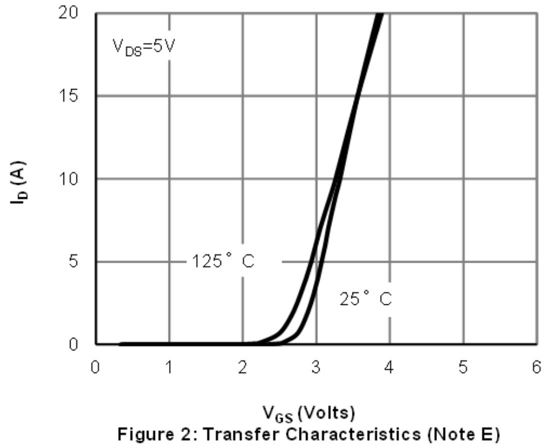


Figure 2: Transfer Characteristics (Note E)

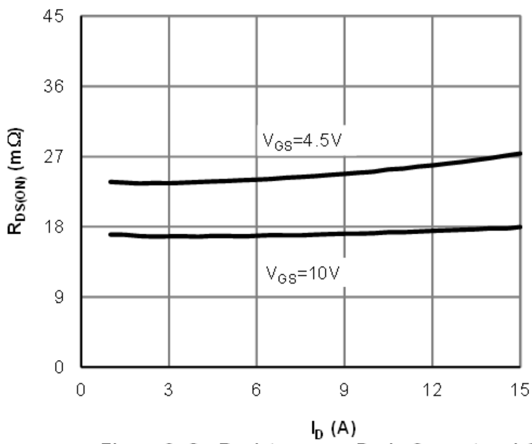
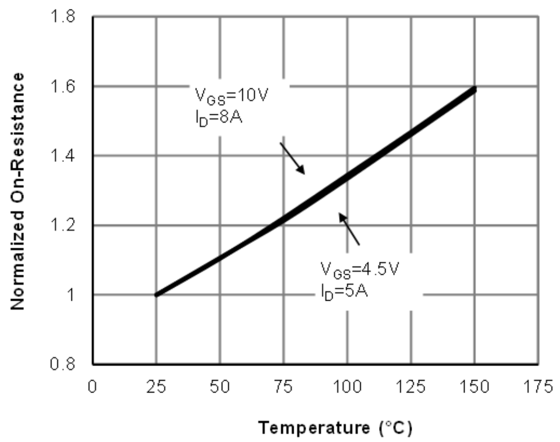


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)



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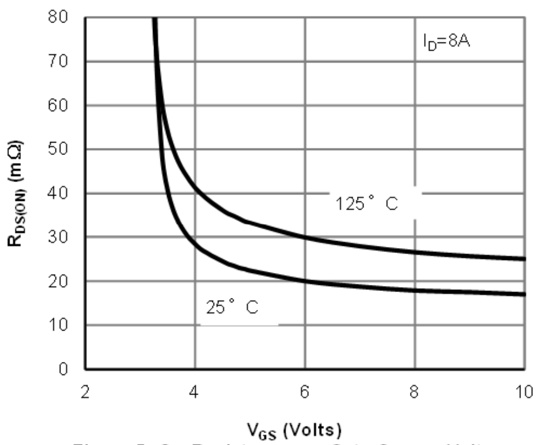


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

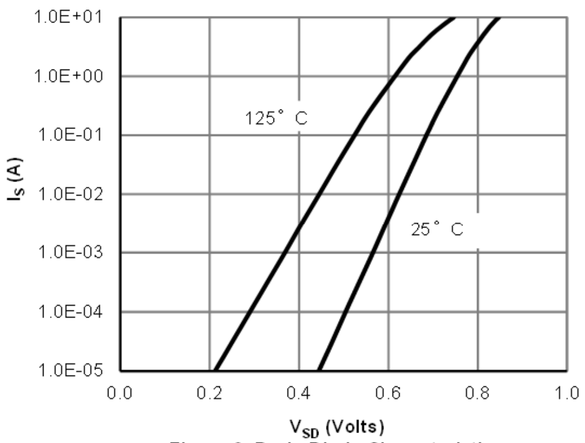


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

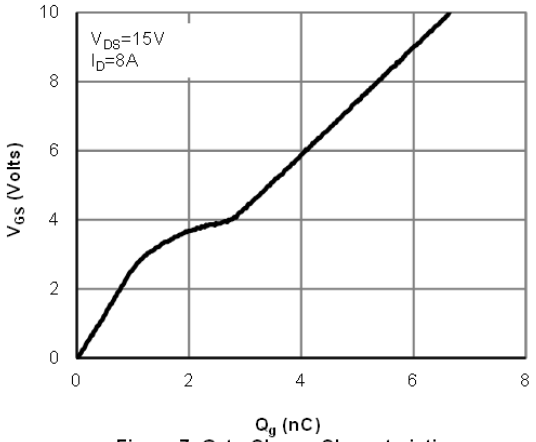


Figure 7: Gate-Charge Characteristics

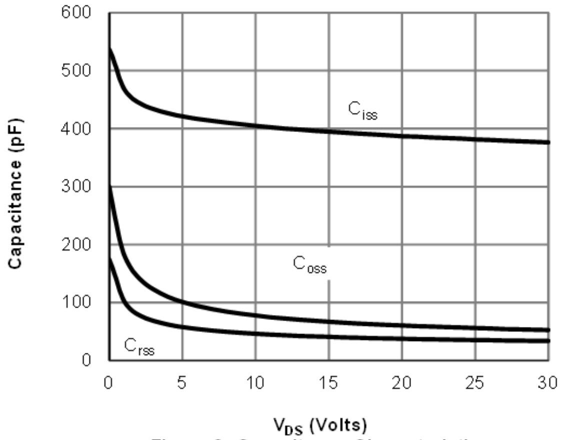
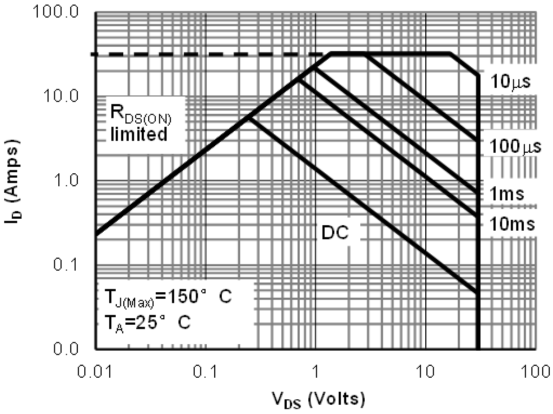
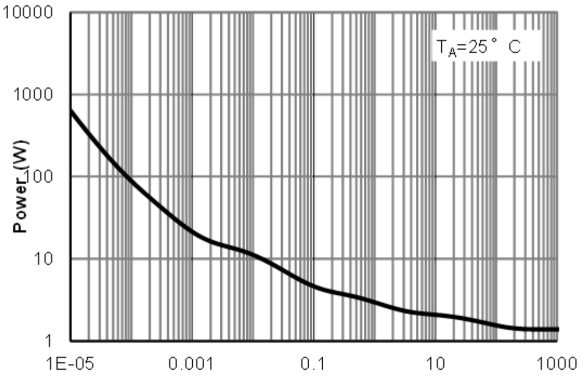


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)



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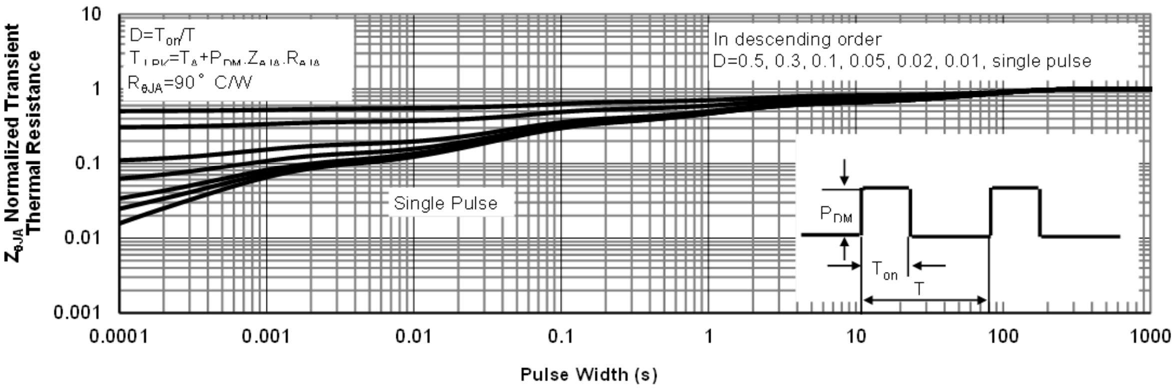
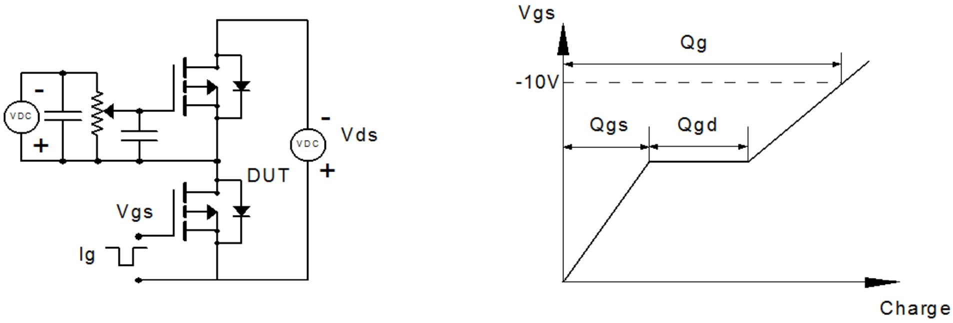
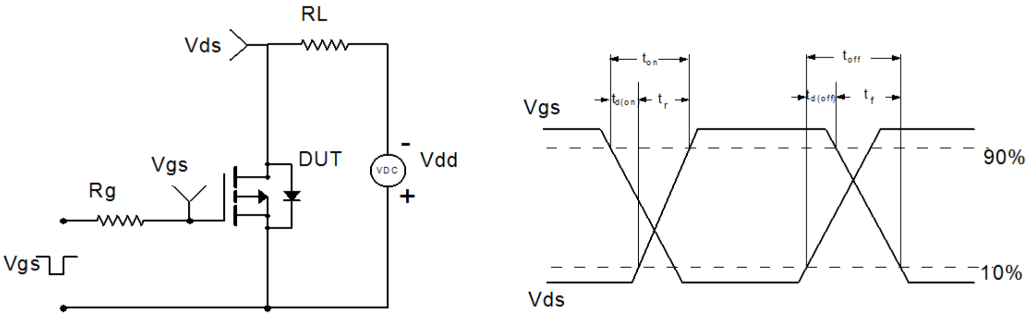


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

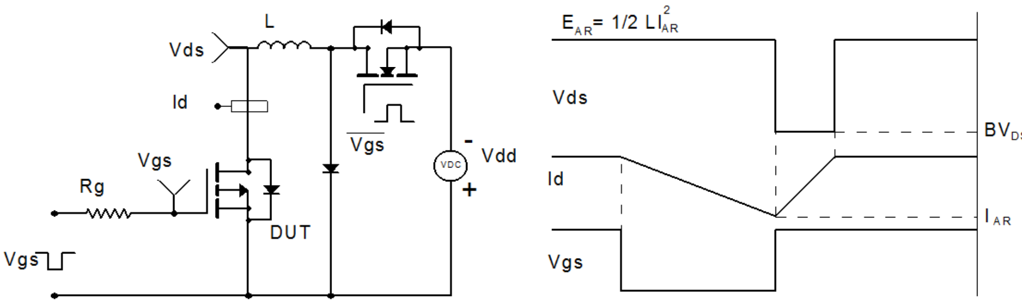
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

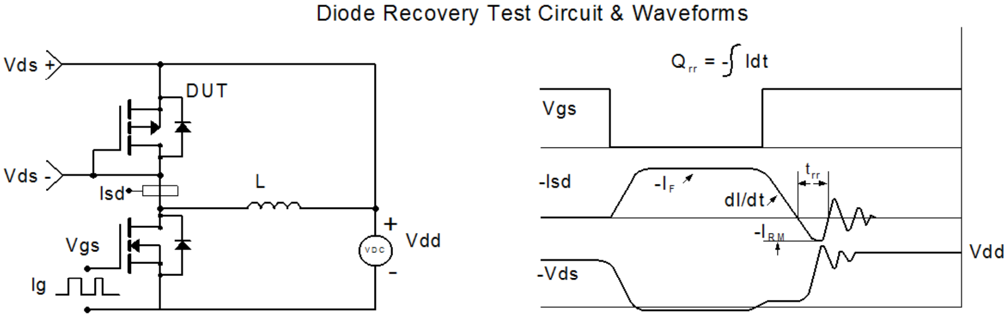


Figure A: Gate Charge Test Circuit & Waveforms

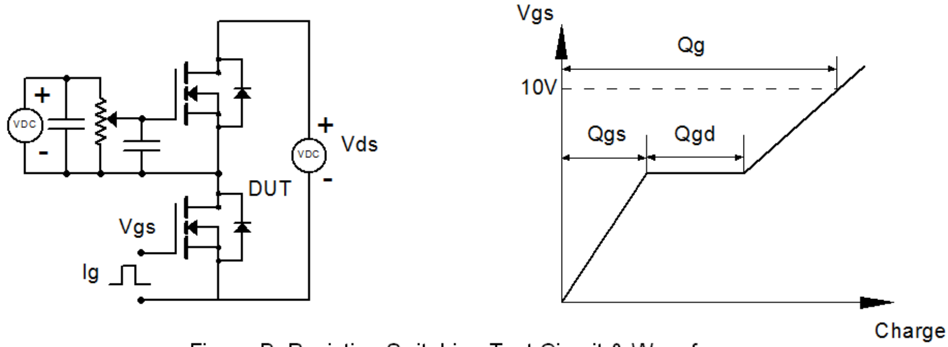


Figure B: Resistive Switching Test Circuit & Waveforms

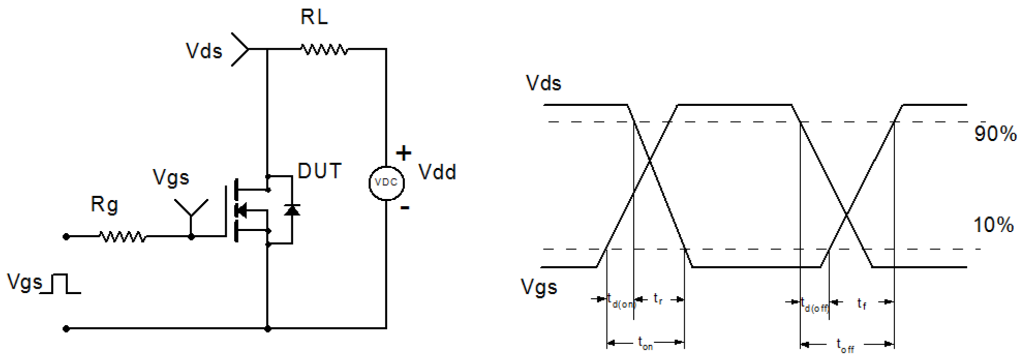


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

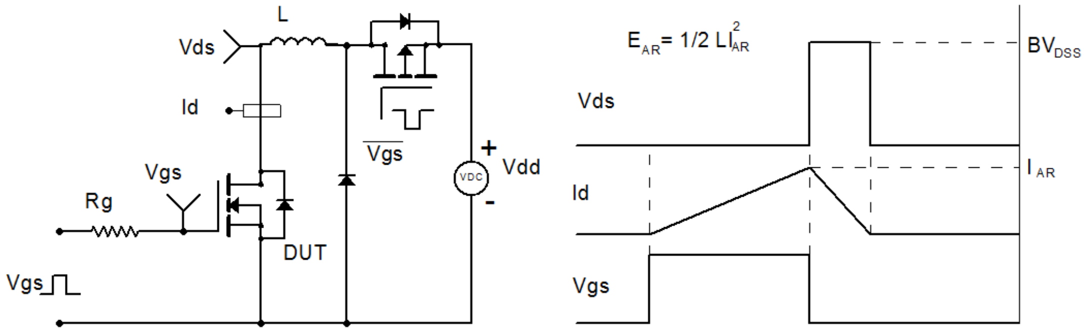


Figure D: Diode Recovery Test Circuit & Waveforms