

General Description

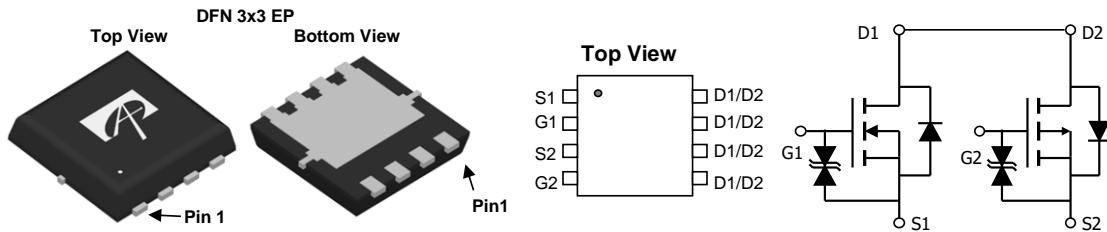
The AONR26309A uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in inverter and other applications.

Product Summary

N-channel	P-channel	
$V_{DS} (V) = 30V$	$V_{DS} (V) = -30V$	
$I_D = 14A$	$I_D = -21A$	$(V_{GS} = \pm 10V)$
$R_{DS(ON)} < 20m\Omega$	$R_{DS(ON)} < 32m\Omega$	$(V_{GS} = \pm 10V)$
$R_{DS(ON)} < 26m\Omega$	$R_{DS(ON)} < 55m\Omega$	$(V_{GS} = \pm 4.5V)$

ESD protection

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max N-channel	Max P-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ C$	14	A
		$T_C=100^\circ C$	9	
Pulsed Drain Current ^C	I_{DM}	35	-44	A
Continuous Drain Current ^A	I_{DSM}	$T_A=25^\circ C$	6.5	W
		$T_A=70^\circ C$	5	
Avalanche Current ^C	I_{AR}	15	-20	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	11	20	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	7	W
		$T_C=100^\circ C$	2.8	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	1.5	W
		$T_A=70^\circ C$	0.9	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$

Thermal Characteristics: N-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	40	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	70	
Maximum Junction-to-Case ^B	$R_{\theta JC}$	15	18	$^\circ C/W$

Thermal Characteristics: P-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	40	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	70	
Maximum Junction-to-Case ^B	$R_{\theta JC}$	5	6	$^\circ C/W$

N-channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.3	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =6.5A T _J =125°C		16 24	20 30	mΩ
		V _{GS} =4.5V, I _D =6A		20	26	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =6.5A		33		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		600		pF
C _{oss}	Output Capacitance			70		pF
C _{riss}	Reverse Transfer Capacitance			60		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.2	2.4	3.6	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =6.5A		12	20	nC
Q _{g(4.5V)}	Total Gate Charge			6	12	nC
Q _{gs}	Gate Source Charge			2.2		nC
Q _{gd}	Gate Drain Charge			2.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =2.307Ω, R _{GEN} =3Ω		4.5		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			20		ns
t _f	Turn-Off Fall Time			4		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =6.5A, di/dt=500A/μs		5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =6.5A, di/dt=500A/μs		6		nC

- A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
- B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C.
- D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C.
- G. The maximum current rating is limited by bond-wires.
- H. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

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N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

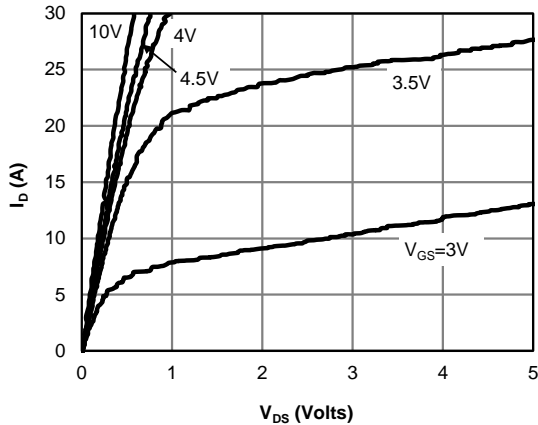


Figure 1: On-Region Characteristics (Note E)

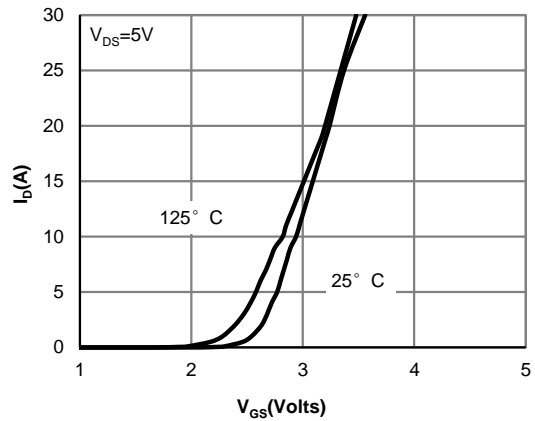


Figure 2: Transfer Characteristics (Note E)

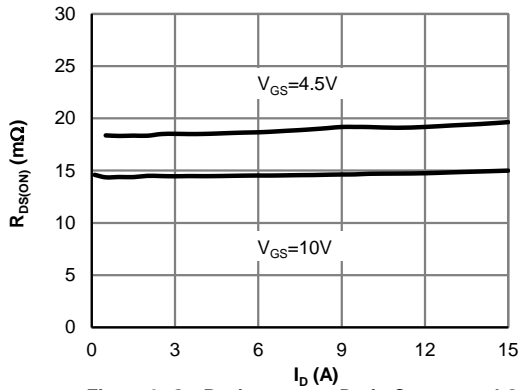


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

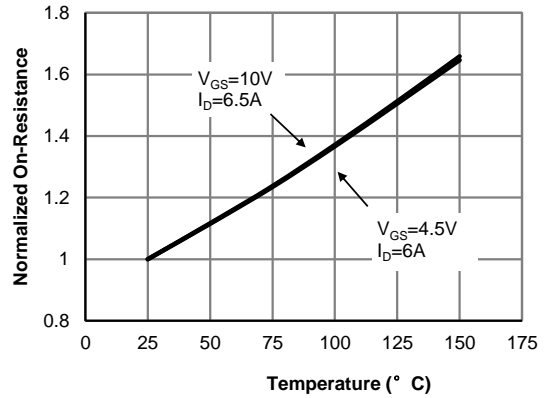


Figure 4: On-Resistance vs. Junction Temperature (Note E)

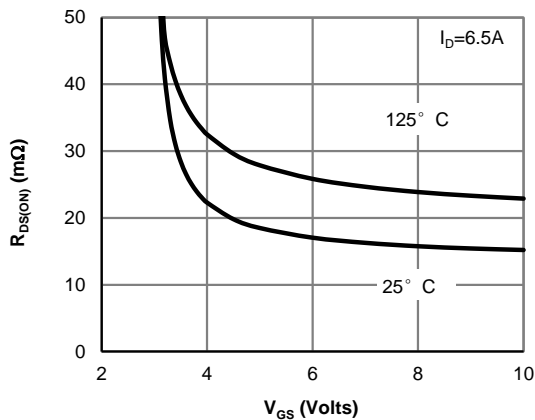


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

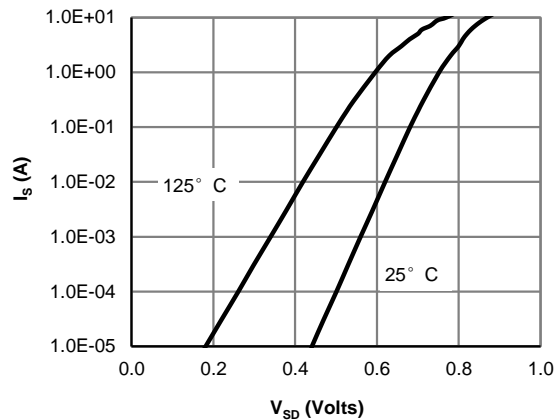


Figure 6: Body-Diode Characteristics (Note E)

N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

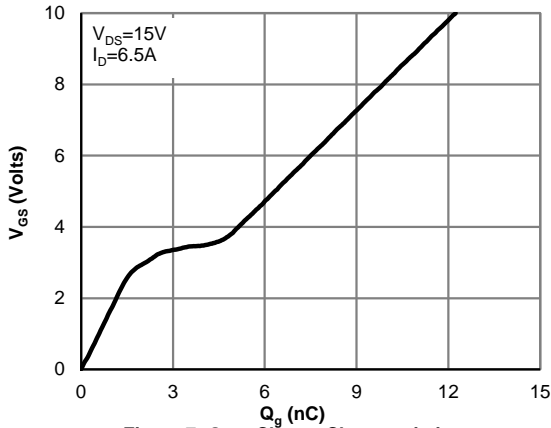


Figure 7: Gate-Charge Characteristics

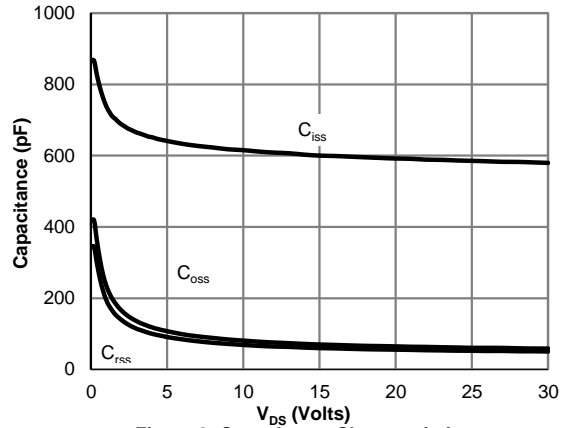


Figure 8: Capacitance Characteristics

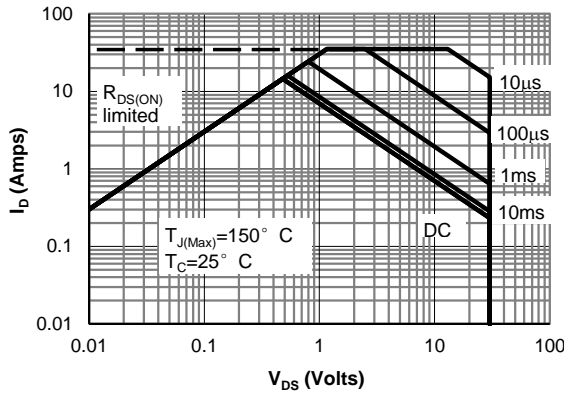


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

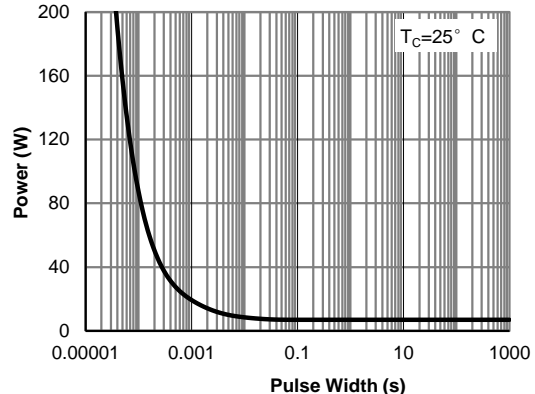


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

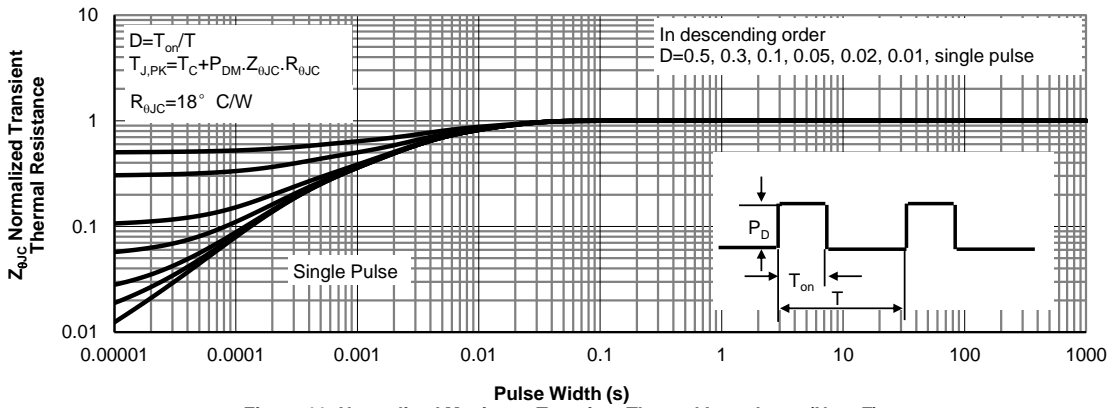


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

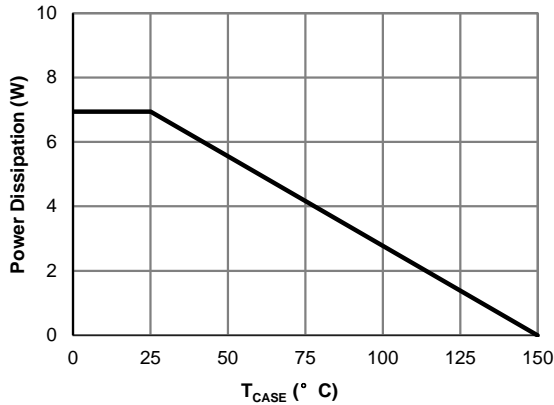


Figure 12: Power De-rating (Note F)

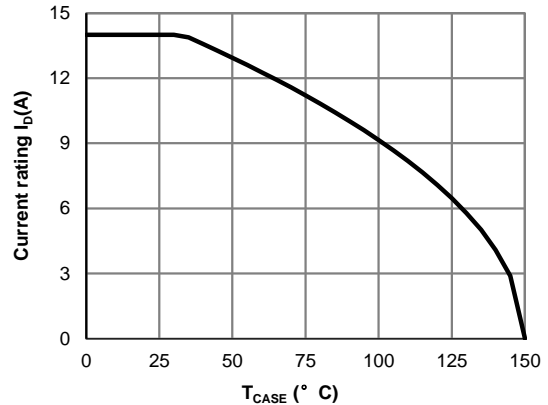


Figure 13: Current De-rating (Note F)

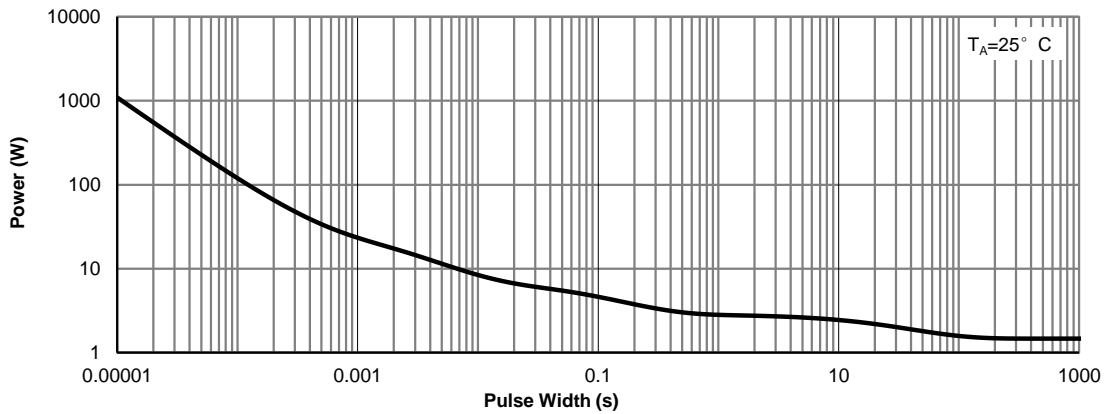


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

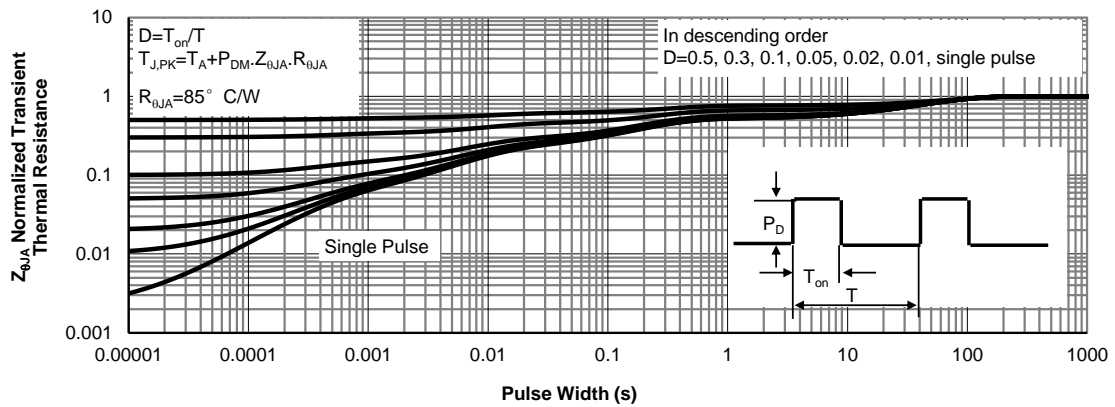
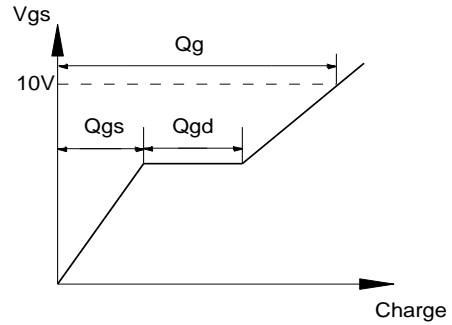
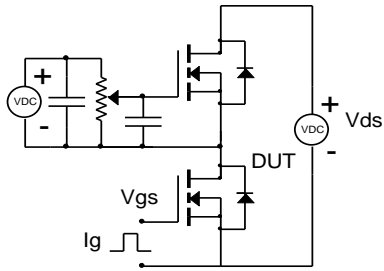
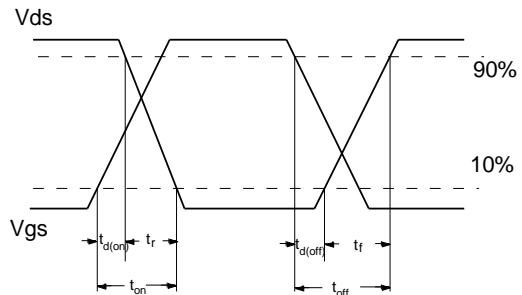
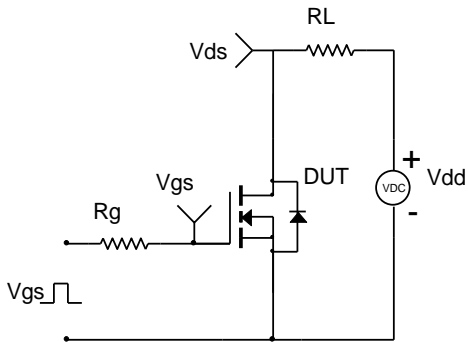


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

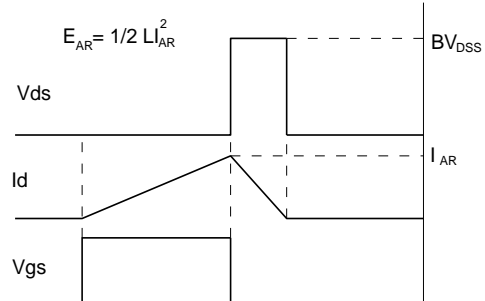
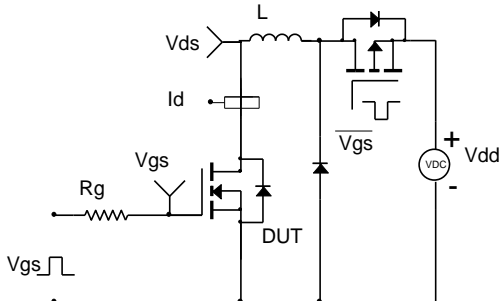
Gate Charge Test Circuit & Waveform



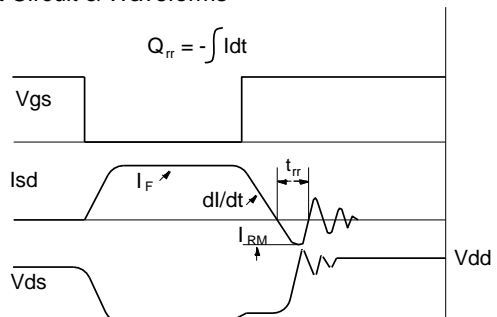
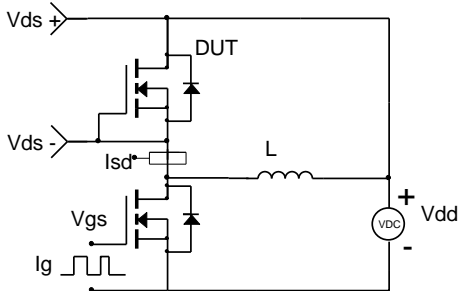
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.2	-1.7	-2.2	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-5.7A T _J =125°C		25 32	32 41	mΩ
		V _{GS} =-4.5V, I _D =-4.4A		35	55	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-5.7A		17		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.8	-1	V
I _S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		1100		pF
C _{oss}	Output Capacitance			120		pF
C _{riss}	Reverse Transfer Capacitance			105		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		11	18	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-5.7A		22	33	nC
Q _{g(4.5V)}	Total Gate Charge			11	18	nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			6.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =2.63Ω, R _{GEN} =3Ω		12		ns
t _r	Turn-On Rise Time			9		ns
t _{D(off)}	Turn-Off DelayTime			55		ns
t _f	Turn-Off Fall Time			19		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =-5.7A, di/dt=500A/μs		12	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-5.7A, di/dt=500A/μs		17		nC

- A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
- B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C.
- D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C.
- G. The maximum current rating is limited by bond-wires.
- H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

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P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

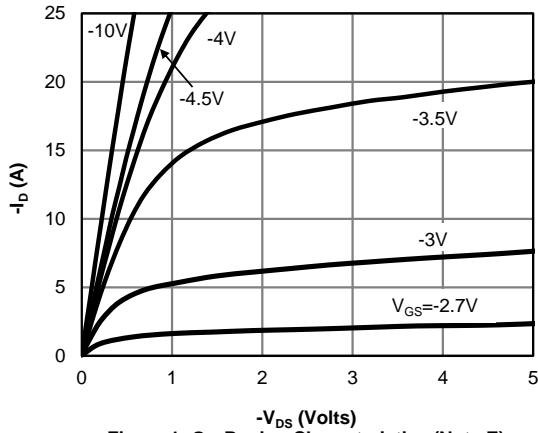


Figure 1: On-Region Characteristics (Note E)

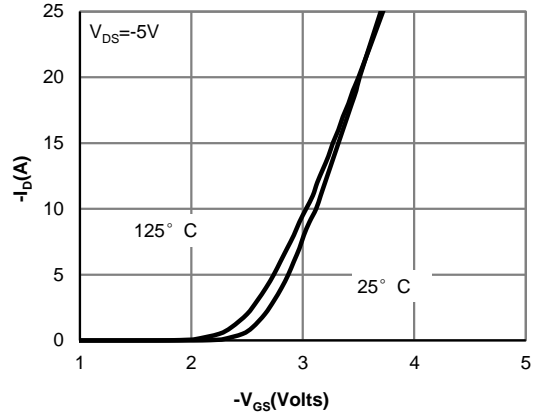


Figure 2: Transfer Characteristics (Note E)

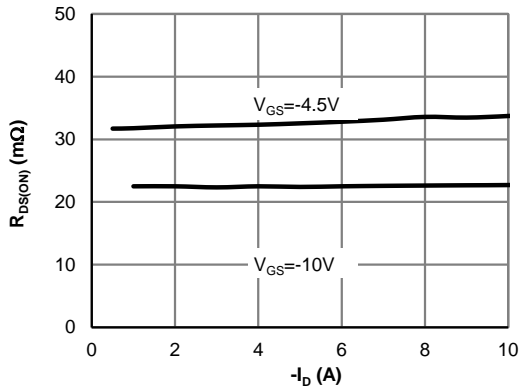


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

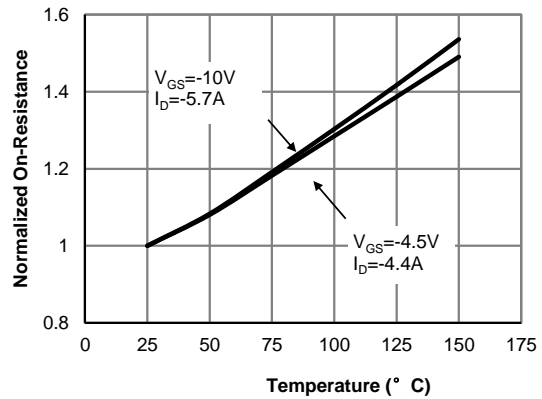


Figure 4: On-Resistance vs. Junction Temperature (Note E)

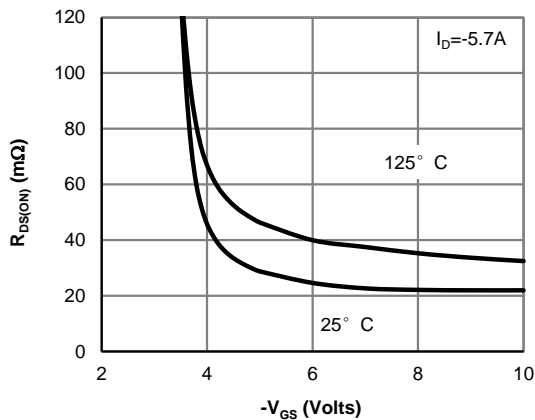


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

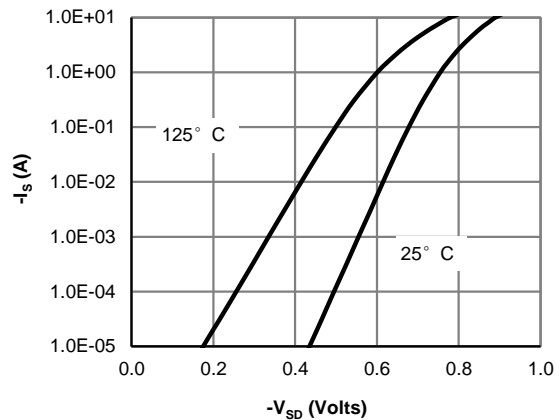


Figure 6: Body-Diode Characteristics (Note E)

P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

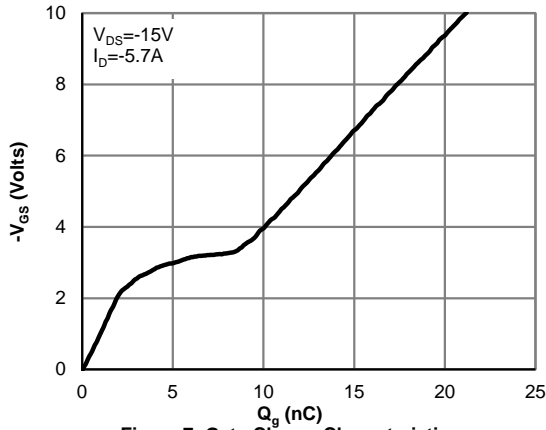


Figure 7: Gate-Charge Characteristics

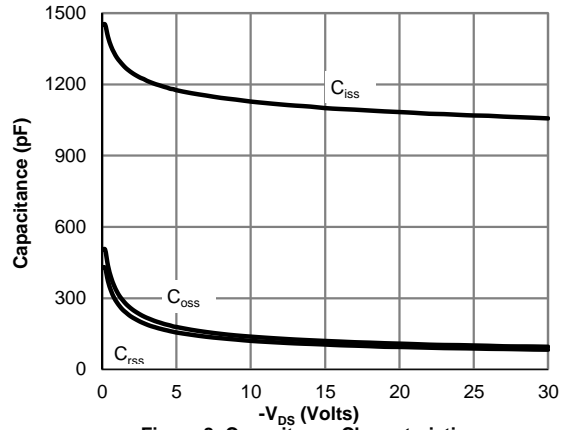


Figure 8: Capacitance Characteristics

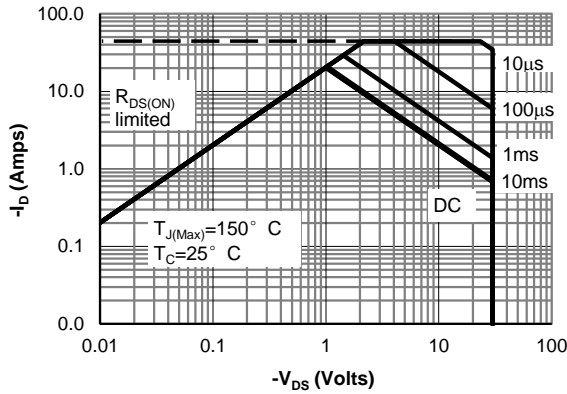


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

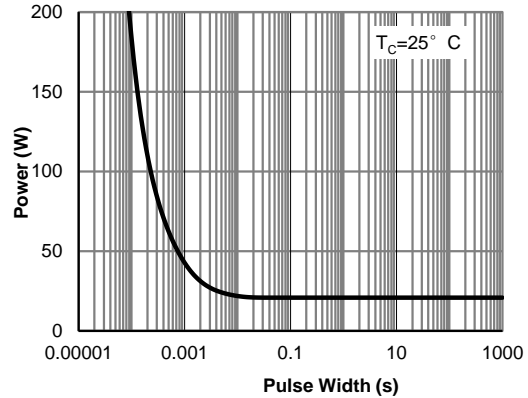


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

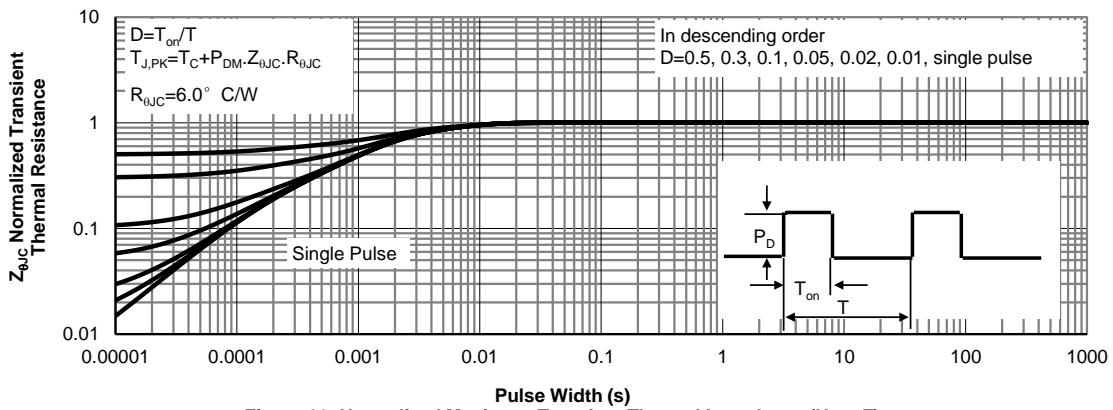


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

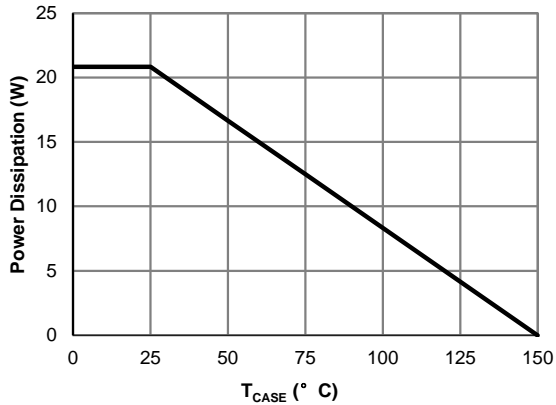


Figure 12: Power De-rating (Note F)

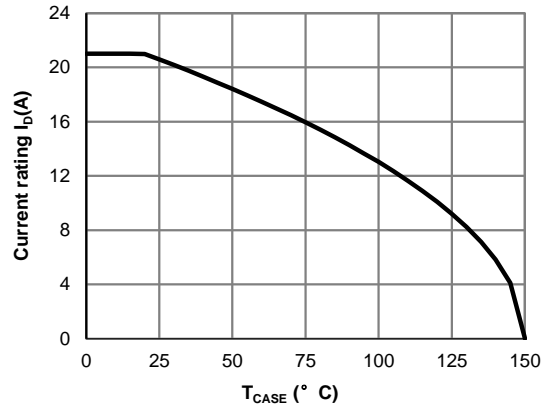


Figure 13: Current De-rating (Note F)

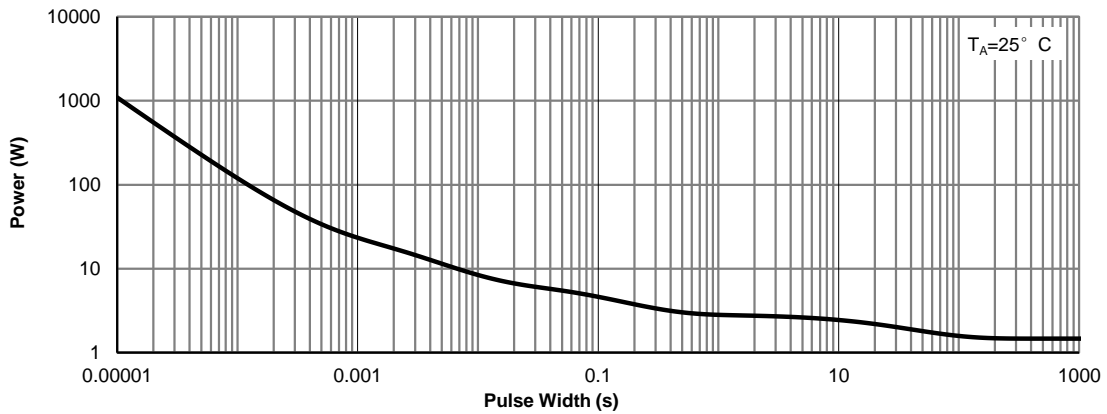


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

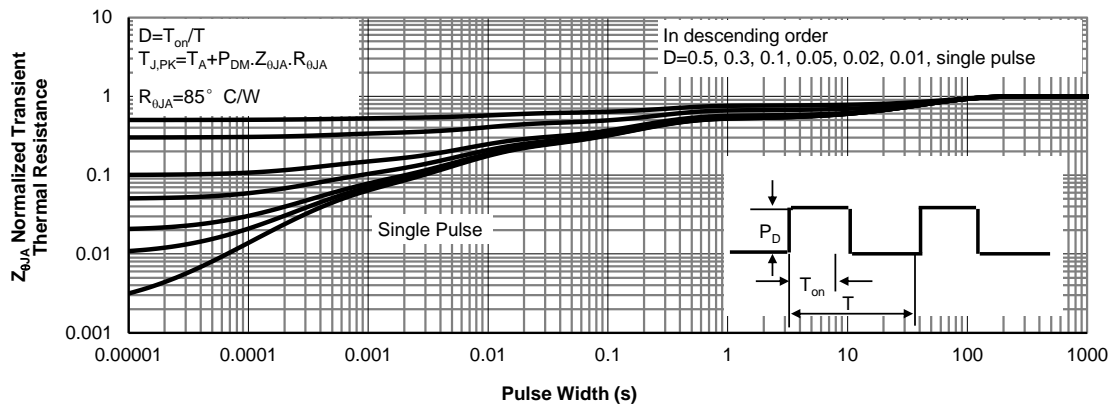
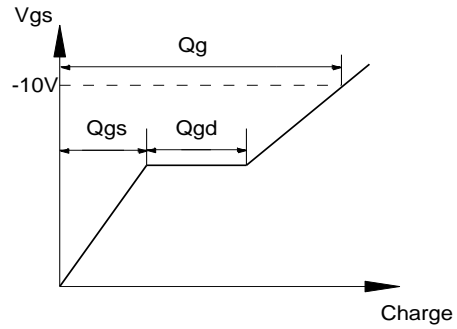
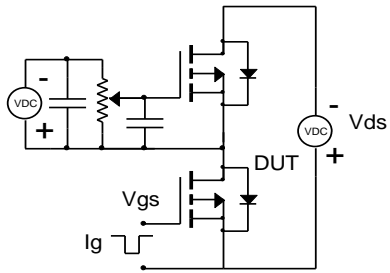
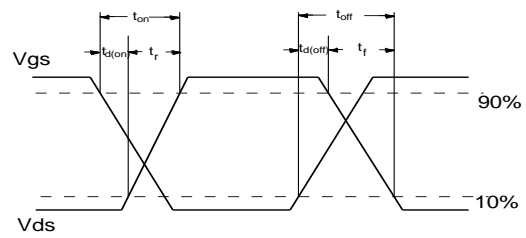
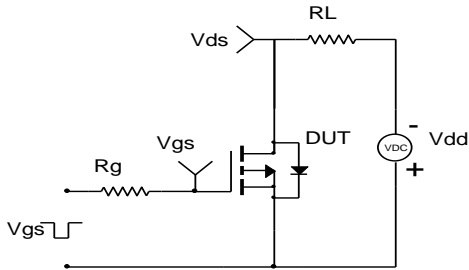


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

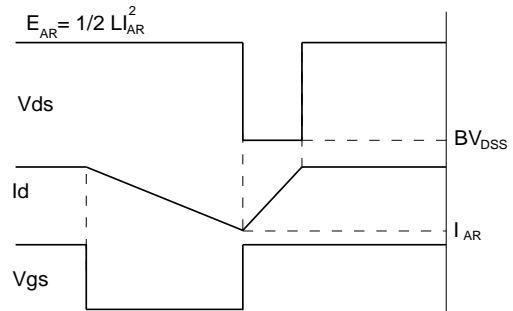
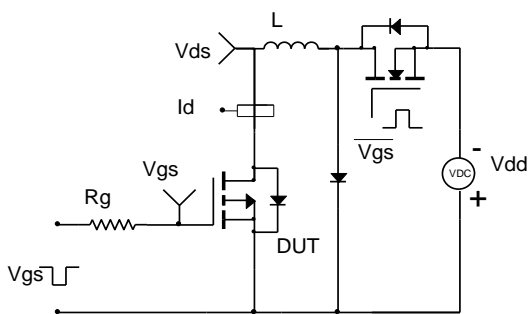
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

