



ALPHA & OMEGA
SEMICONDUCTOR

AONS74306

30V N-Channel MOSFET

General Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

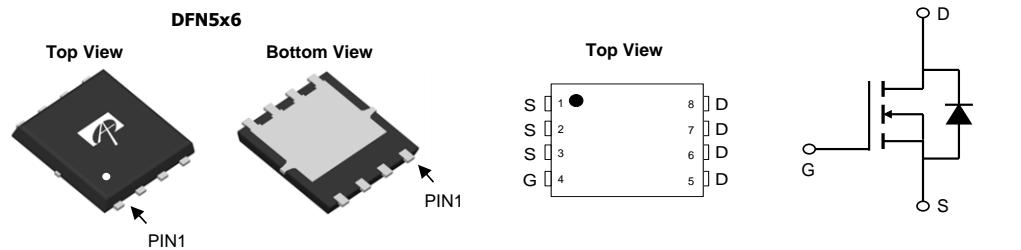
Applications

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial
- See Note I

Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	370A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 0.95mΩ
$R_{DS(ON)}$ (at $V_{GS}=6.5V$)	< 1.2mΩ

100% UIS Tested
100% R_g Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS74306	DFN5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Silicon)	I_D	370	A
$T_C=100^\circ C$		230	
Pulsed Drain Current ^C	I_{DM}	800	
Continuous Drain Current	I_{DSM}	71	A
$T_A=70^\circ C$		57	
Avalanche Current ^C	I_{AS}	50	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	125	mJ
Power Dissipation ^B	P_D	208	W
$T_C=100^\circ C$		83	
Power Dissipation ^A	P_{DSM}	7.3	W
$T_A=70^\circ C$		4.7	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A $t \leq 10s$	R_{0JA}	14	17	°C/W
Maximum Junction-to-Ambient ^{AD} Steady-State		40	55	°C/W
Maximum Junction-to-Case	Steady-State R_{0JC}	0.46	0.6	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm20\text{V}$			±100	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	1.4	2	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_b=20\text{A}$ $T_J=125^\circ\text{C}$		0.75 1.1	0.95 1.4	$\text{m}\Omega$
		$V_{GS}=6.5\text{V}, I_D=20\text{A}$		0.85	1.2	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		120		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.65	1	V
I_S	Maximum Body-Diode Continuous Current				200	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		6200		pF
C_{oss}	Output Capacitance			2000		pF
C_{rss}	Reverse Transfer Capacitance			120		pF
R_g	Gate resistance	$f=1\text{MHz}$		2	3	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$		79	170	nC
Q_{gs}	Gate Source Charge			13		nC
Q_{gd}	Gate Drain Charge			7		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega,$ $R_{\text{GEN}}=3\Omega$		10		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			74		ns
t_f	Turn-Off Fall Time			15		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$		27		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$		88		nC

A. The value of $R_{\text{DS(on)}}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation $P_{\text{DS(on)}}$ is based on $R_{\text{DS(on)}} \leq 10\text{s}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width 260us limited by junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.

D. The $R_{\text{DS(on)}}$ is the sum of the thermal impedance from junction to case R_{JJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300us pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

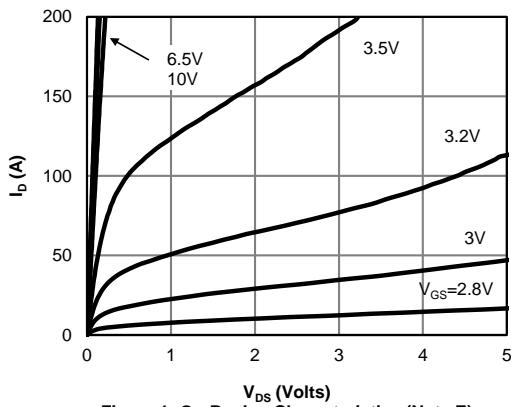
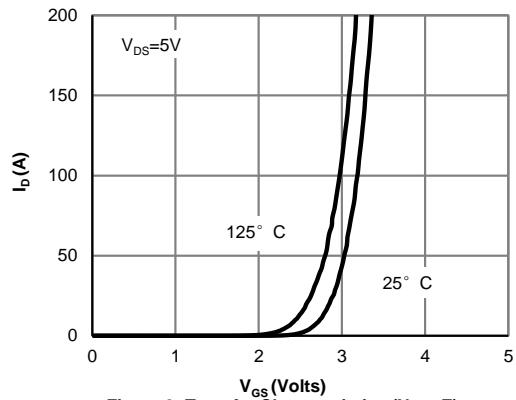
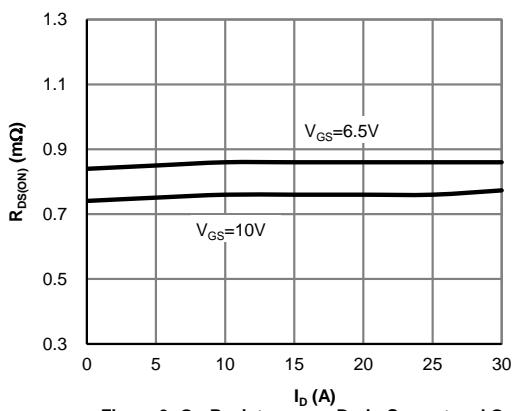
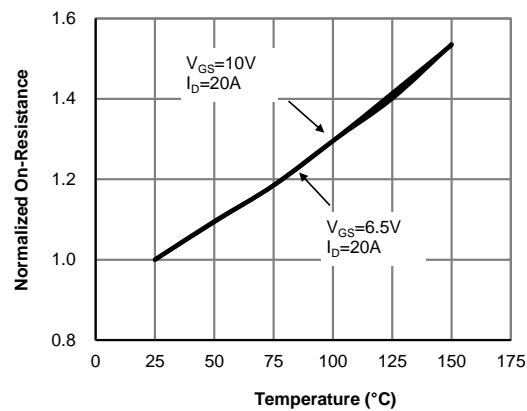
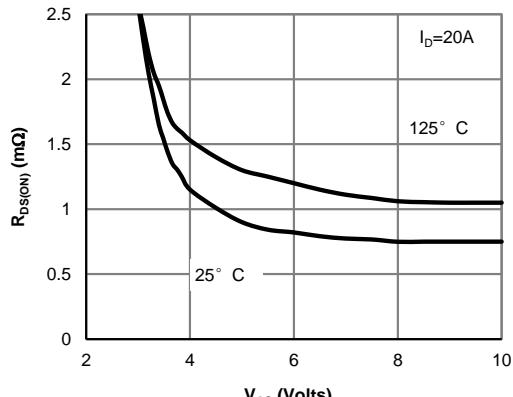
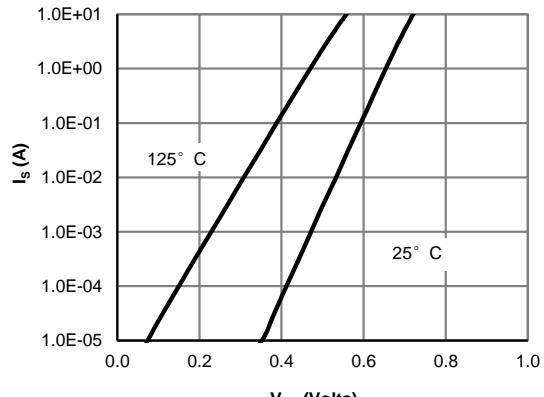
G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

H. For application requiring slow >1ms turn-on/turn-off, please consult AOS FAE for proper product selection.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)

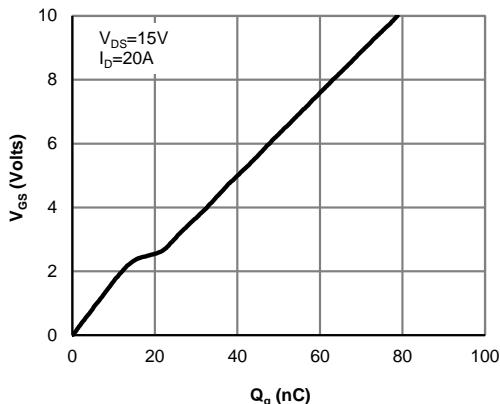
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

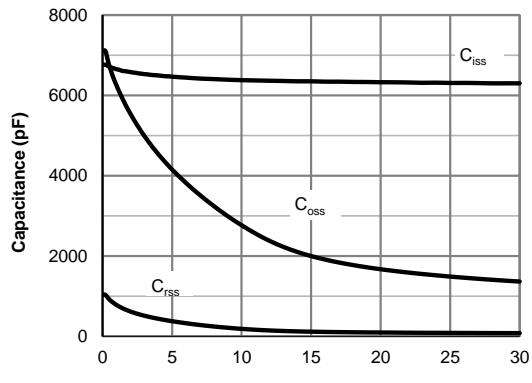


Figure 8: Capacitance Characteristics

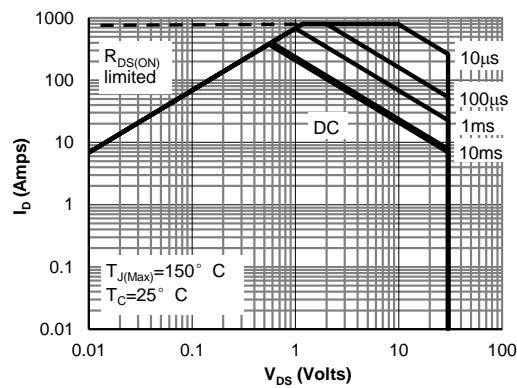


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

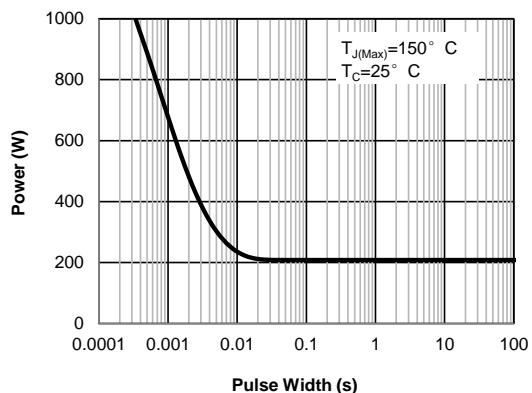


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

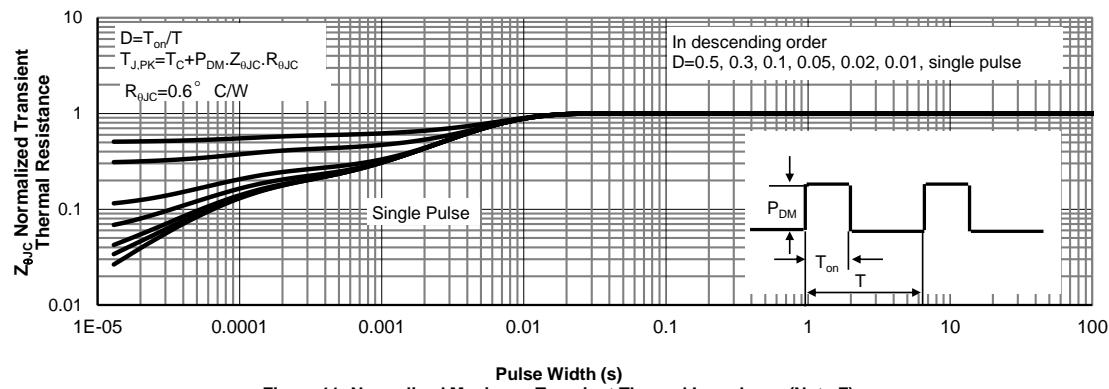


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

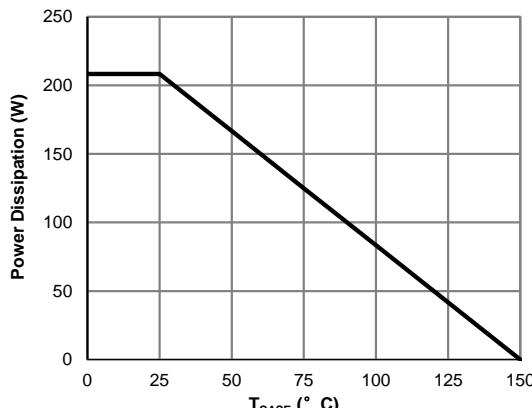
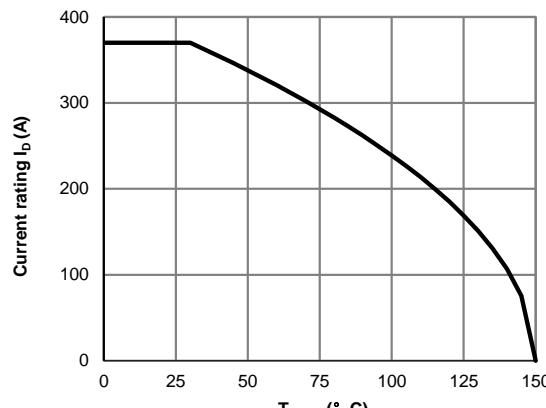
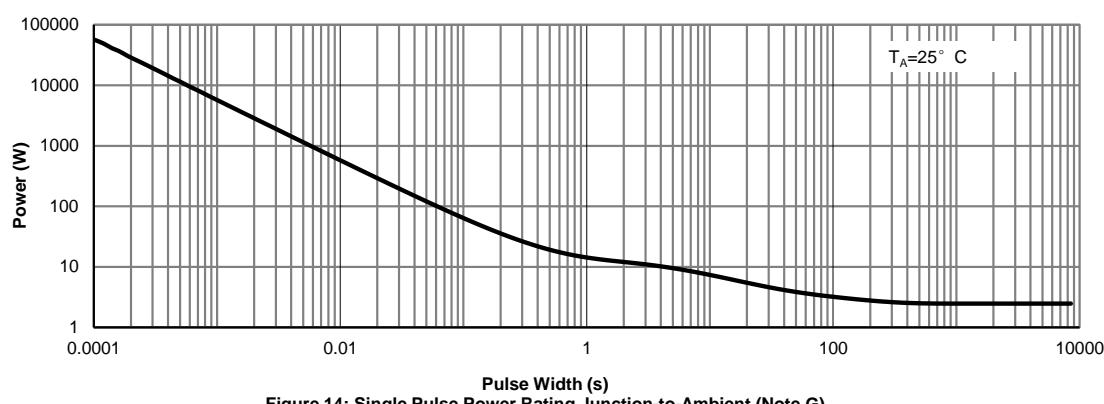
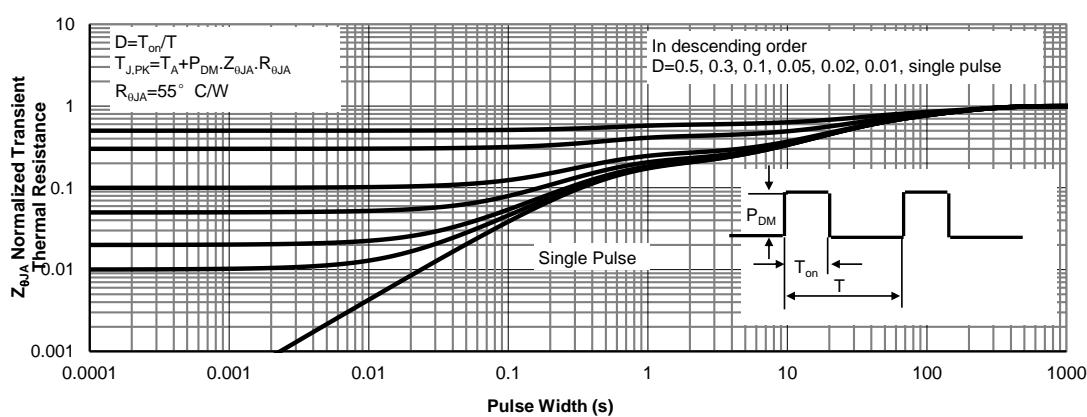
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 12: Power De-rating (Note F)

Figure 13: Current De-rating (Note F)

Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

Figure A: Gate Charge Test Circuit & Waveforms

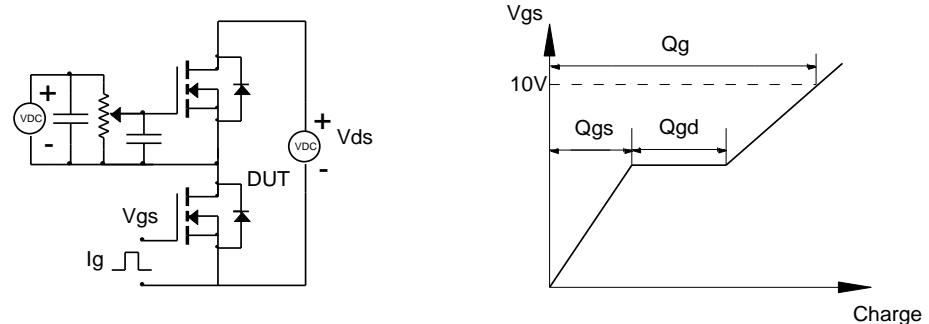


Figure B: Resistive Switching Test Circuit & Waveforms

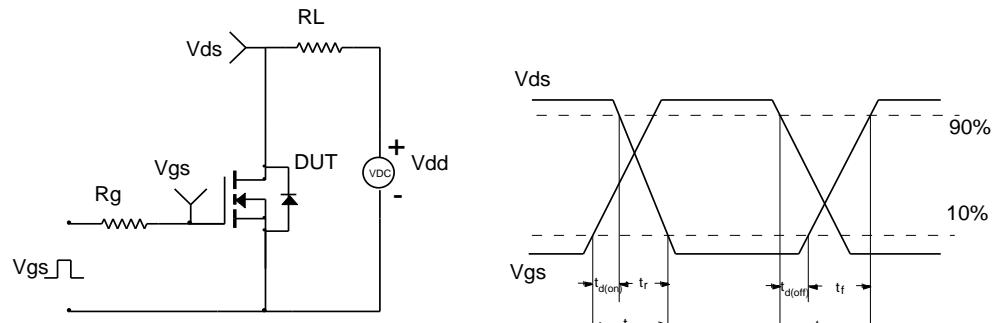


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

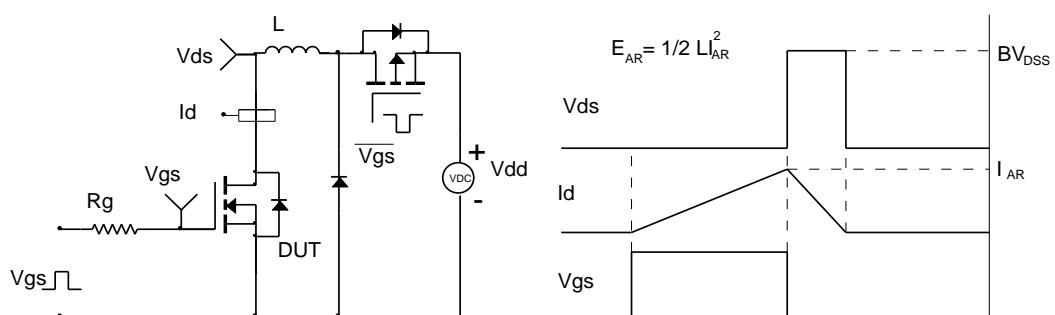


Figure D: Diode Recovery Test Circuit & Waveforms

