ALPHA & OMEGA SEMICONDUCTOR

AOTL025V75X3

750V αSiC Silicon Carbide Power MOSFET

Features

- Proprietary αSiC MOSFET technology
- Low loss, with low $R_{DS,(ON)}$
- Fast switching with low R_G and low capacitance
- Flexible gate voltage range (V_{GS} = 15V to 18V)
- Low reverse recovery diode (Qrr)

Product Summary

V_{DS} @ $T_{J, max}$	750V
I_{DM}	255A
$R_{DS(ON), typ}$	25mΩ
Q_{rr}	73nC
E_{OSS} @ 400V	18μJ
100 % UIS Tested	

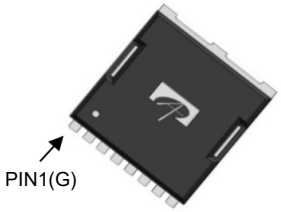
Applications

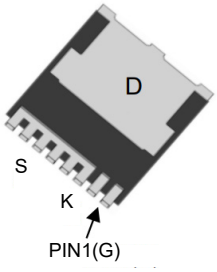
Renewable
- SMPS/AI server
- DC/DC converters
- UPS

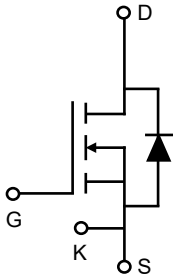
Industrial
- Energy storage
- Solar inverters

GREEN Product

Pin Configuration







Ordering Part Number	Package Type	Form	Shipping Quantity
AOTL025V75X3	TOLL	Tape and Reel	2000/Reel

Absolute Maximum Ratings

T_A = 25°C, unless otherwise specified.

Symbol	Parameter		AOTL025V75X3	Units
V_{DS}	Drain-Source Voltage		750	V
$V_{GS, MAX}$	Gate-Source Voltage	Maximum	-8/+23	
$V_{GS, OP, TRANS}$		Max Transient[A]	-10/+25	
$V_{GS, OP, ON}$		Recommended Operating[B]	15...18	
$V_{GS, OP, OFF}$			-3...0	
I_D	Countinuous Drain Current[C]	T_C = 25ºC	82	A
		T_C = 100ºC	58	
I_{DM}	Pulsed Drain Current[D]		255	
E_{AS}	Single Pulsed Avalanche Energy[F]		563	J
P_D	Power Dissipation[E]	T_C = 25ºC	254	W
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 175	ºC
T_L	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		260	ºC

Electrical Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V, T_J = 25°C		750			V
		I_D = 250µA, V_{GS} = 0V, T_J = 150°C		750			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 750V, V_{GS} = 0V				100	µA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = +18/-3V				200	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 16mA		2.2	3	4.3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 15V, I_D = 16A	T_J = 25°C		30	42	mΩ
			T_J = 175°C		40		
		V_{GS} = 18V, I_D = 16A	T_J = 25°C		25	35	
			T_J = 175°C		38		
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 16A			5		s
V_{SD}	Diode Forward Voltage	I_S = 16A,V_{GS} = -3V			4	5	V
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 400V, f = 100kHz			2379		pF
C_{oss}	Output Capacitance				192		
C_{rss}	Reverse Transfer Capacitance				14		
E_{oss}	C_{oss} Stored Energy				18		µJ
$C_{o(er)}$	Effective output capacitance, energy related[L]	V_{GS} = 0V, V_{DS} = 0 to 400V, f = 100kHz			216		pF
$C_{o(tr)}$	Effective output capacitance, time related[M]				282		
R_G	Gate Resistance	f = 1MHz			1.4		Ω
SWITCHING							
Q_g	Total Gate Charge	V_{GS} = -3/+18V, V_{DS} = 520V, I_D = 16A			94		nC
Q_{gs}	Gate Source Charge				24		
Q_{gd}	Gate Drain Charge				25		
$t_{D(on)}$	Turn-On Delay Time	V_{GS} = -3V/+18V, V_{DS} = 400V, I_D = 30A, $R_{G,ON}$ = $R_{G,OFF}$ = 2Ω L = 47.5µH FWD: AOTL025V75X3			9		ns
t_r	Turn-On Rise Time				8		ns
$t_{D(off)}$	Turn-Off Delay Time				18		ns
t_f	Turn-Off Fall Time				7		ns
E_{on}	Turn-On Energy				104		µJ
E_{off}	Turn-Off Energy				11		µJ
E_{tot}	Total Switching Energy				115		µJ
t_{rr}	Body Diode Reverse Recovery Time	I_F = 30A, dI/dt = 1500A/µs, V_{DS} = 400V			16		ns
I_{rm}	Peak Reverse Recovery Current				10		A
Q_{rr}	Body Diode Reverse Recovery Charge				73		nC

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient[G,H]		40	ºC/W
$R_{\theta JC}$	Maximum Junction-to-Case[I]	0.49	0.59	ºC/W

Note:

A. t_{ON} < 1µs, t < 25 hrs over lifetime. t_{ON} is duration of V_{GS} transient and t is total time spent at $V_{GS,OP,TRANS}$ over product lifetime.
B. Device can be operated at V_{GS} = 0/18V. Actual operating V_{GS} will depend on application specifics such as parasitic inductance and dV/dt but should not exceed maximum ratings.
C. Continuous drain current is calculated based on maximum $R_{\theta JC}$ and typical R_{DSON} at 175°C.
D. I_{DM} obtained using a V_{GS} = 18V, 10ms pulse, and limiting the device to a maximum junction temperature of 175°C.
E. The power dissipation P_D is based on $T_{J(MAX)}$ = 175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
F. L = 5mH, I_{AS} = 15A, R_G = 10Ω, Starting T_J = 25°C.
G. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C.
H. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
I. The value of $R_{\theta JC}$ is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ = 175°C.
J. The static characteristics in Figures 1 to 8 are obtained using < 300µs pulses, duty cycle 0.5% max.
K. These curves are based on $R_{\theta JC}$ which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ =175°C. The SOA curve provides a single pulse rating.
L. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$.
M. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$.

Typical Electrical and Thermal Characteristics

T_A = 25°C, unless otherwise specified.

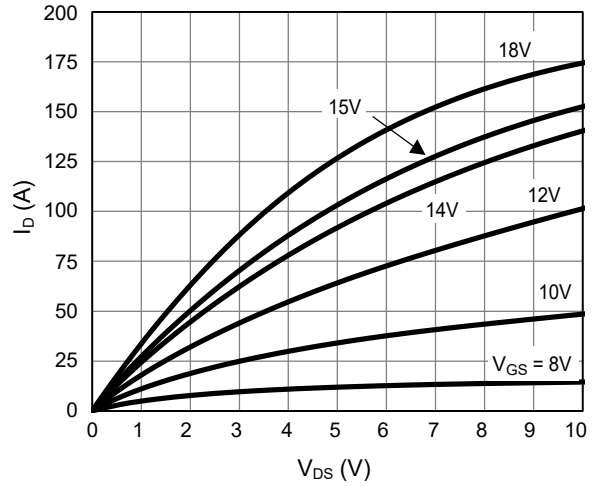


Figure 1. On-Region Characteristics T_J = 25ºC

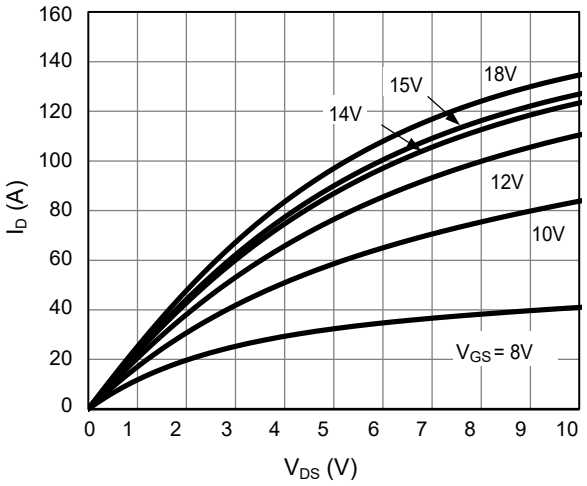


Figure 2. On-Region Characteristics T_J = 175ºC

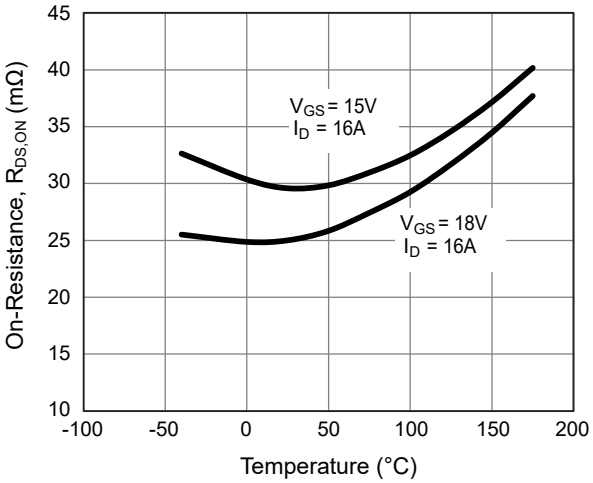


Figure 3. On-Resistance vs. Junction Temperature

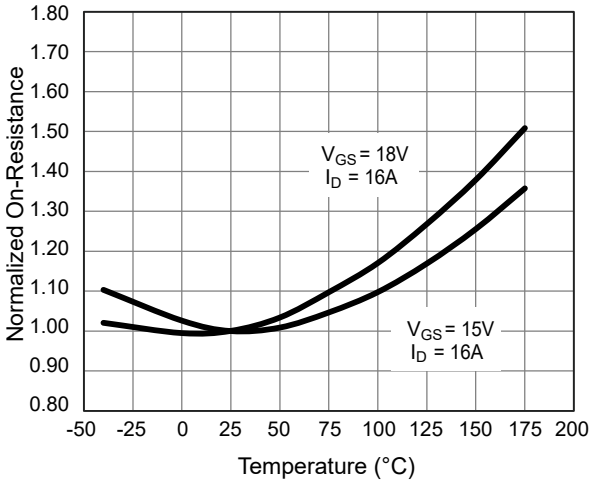


Figure 4. Normalized On-Resistance vs. Junction Temperature

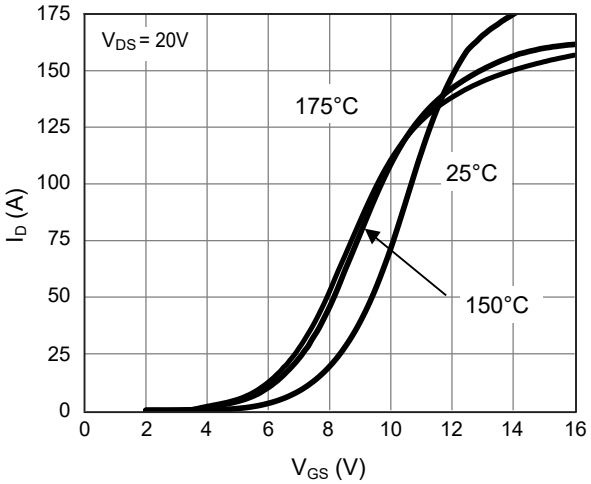


Figure 5. Transfer Characteristics

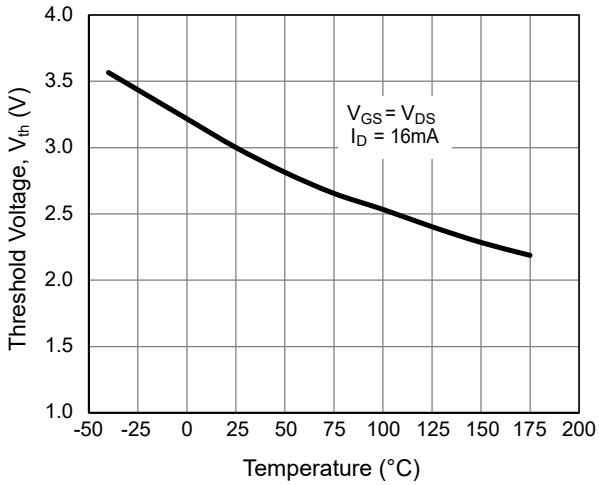


Figure 6. Threshold Voltage vs. Junction Temperature

Typical Electrical and Thermal Characteristics *(Continued)*

T_A = 25°C, unless otherwise specified.

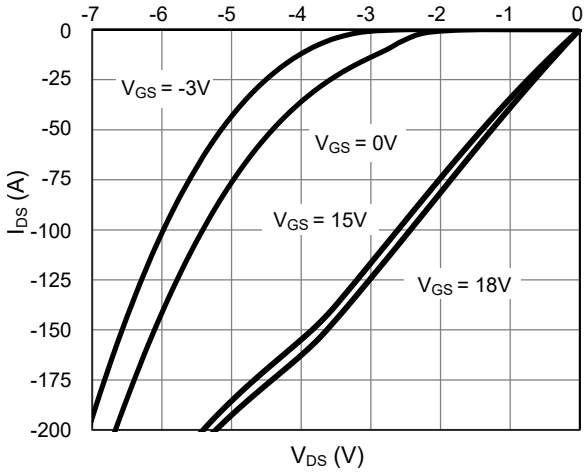


Figure 7. Body-Diode Characteristics at 25ºC

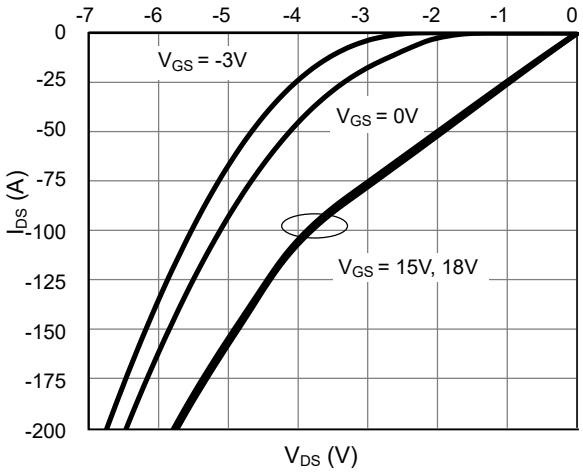


Figure 8. Body-Diode Characteristics at 175ºC

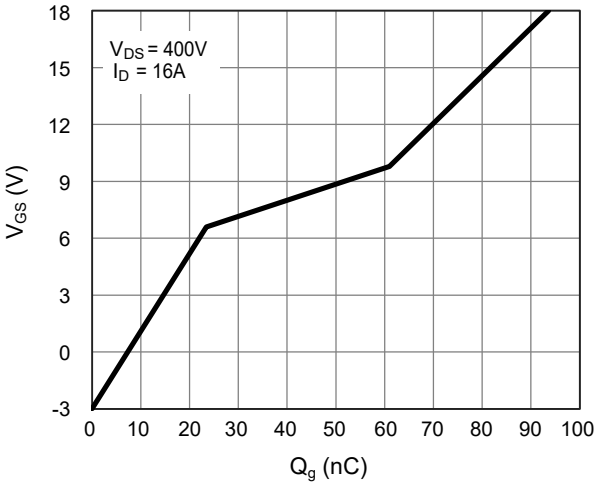


Figure 9. Gate Charge Characteristics

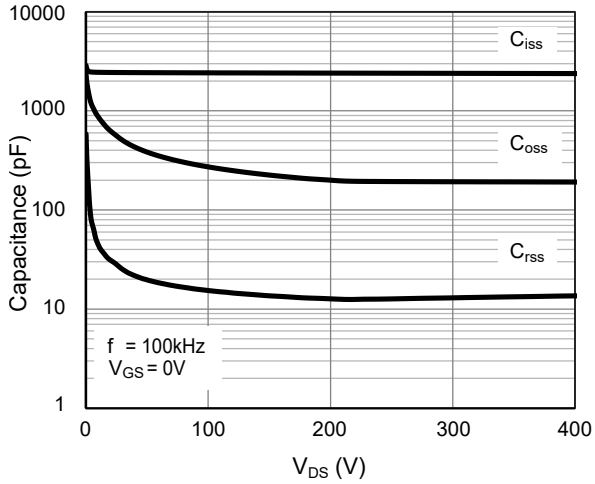


Figure 10. Capacitance Characteristics

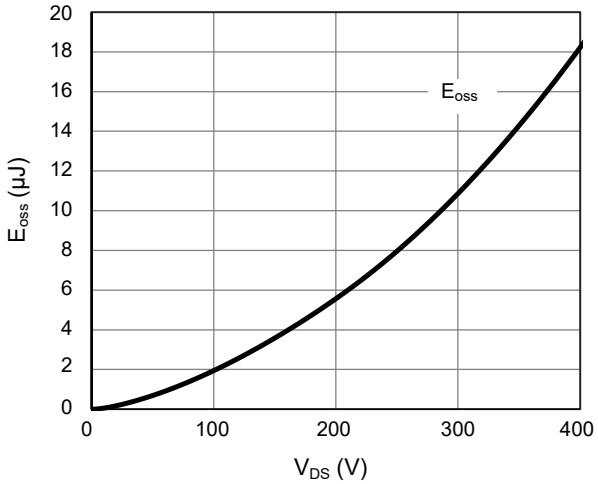


Figure 11. Coss stored Energy

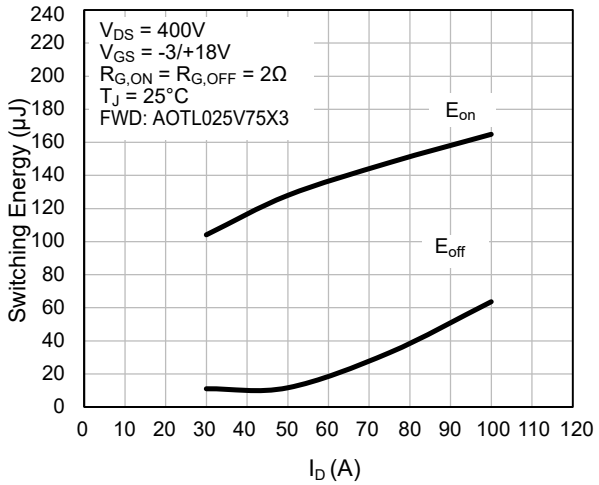


Figure 12. Switching Energy vs. Drain Current

Typical Electrical and Thermal Characteristics *(Continued)*

T_A = 25°C, unless otherwise specified.

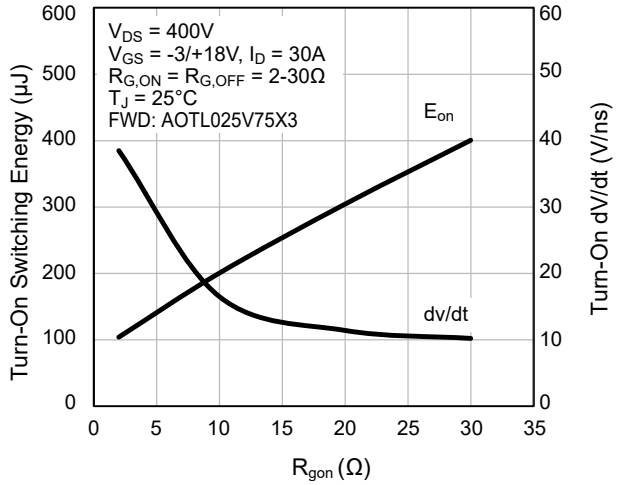


Figure 13. Turn-On Energy and dV/dt vs. External Gate Resistance

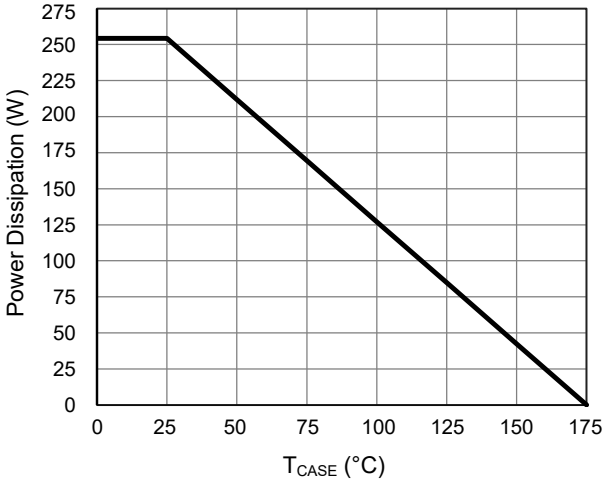


Figure 14. Power De-rating (Note I)

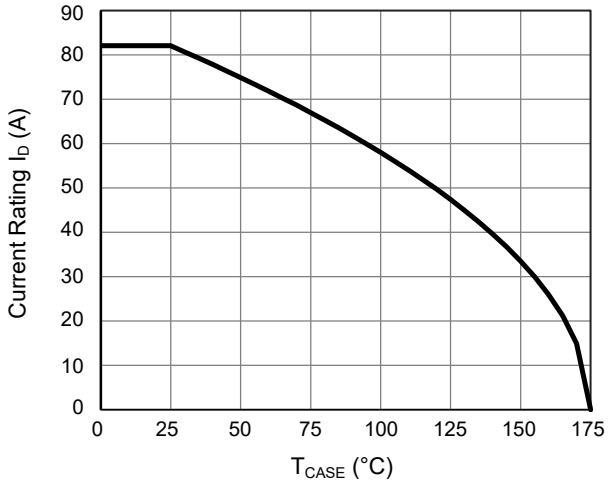


Figure 15. Current De-rating (Note C, K)

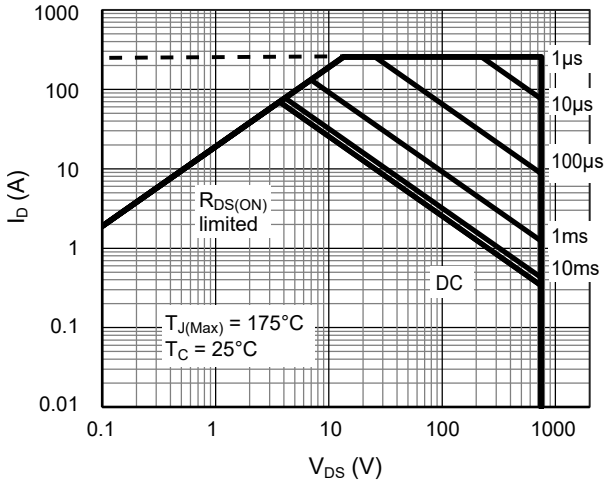


Figure 16. Maximum Forward Biased Safe Operating Area for AOTL025V75X3 (Note K)

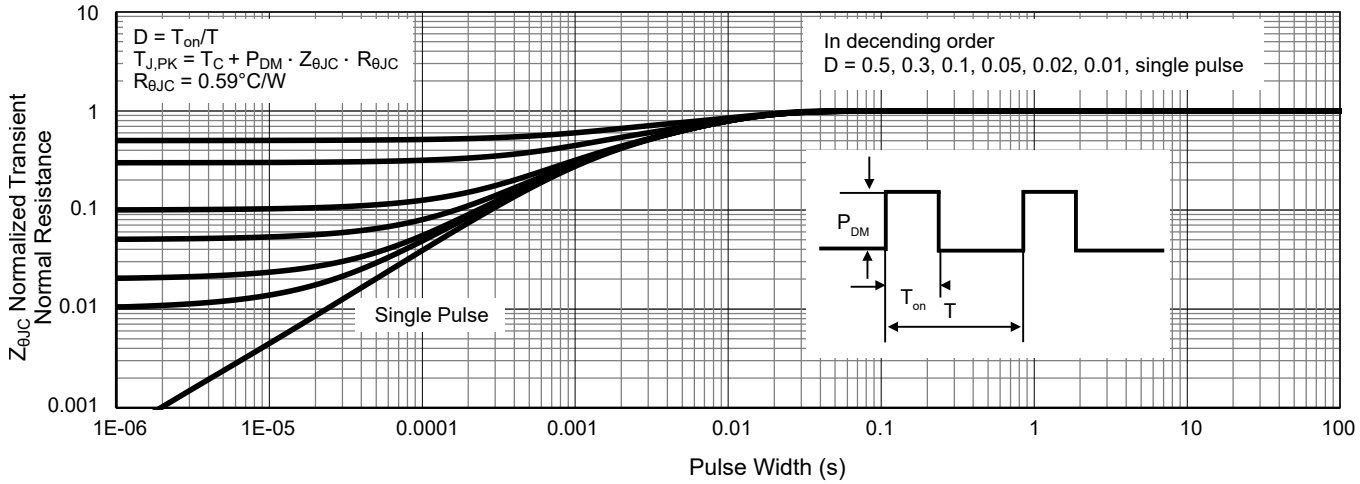


Figure 17. Normalized Maximum Transient Thermal Impedance for AOTL025V75X3 (Note K)

Test Circuits and Waveforms

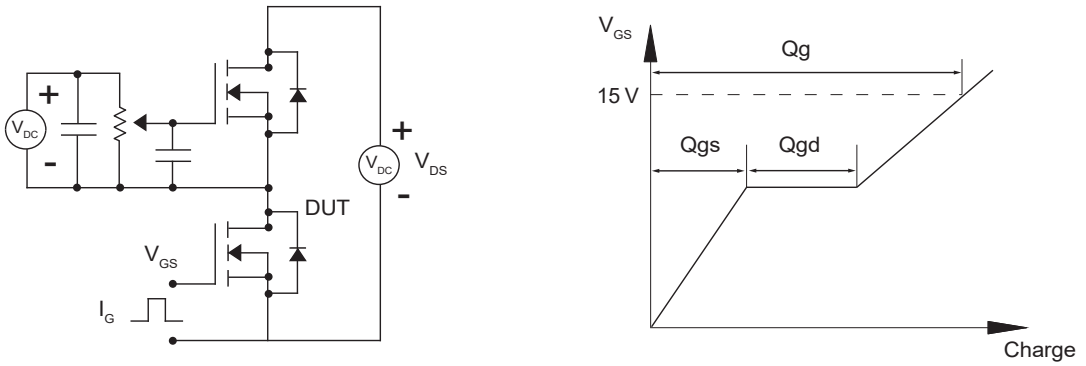


Figure 18. Gate Charge Test Circuits and Waveforms

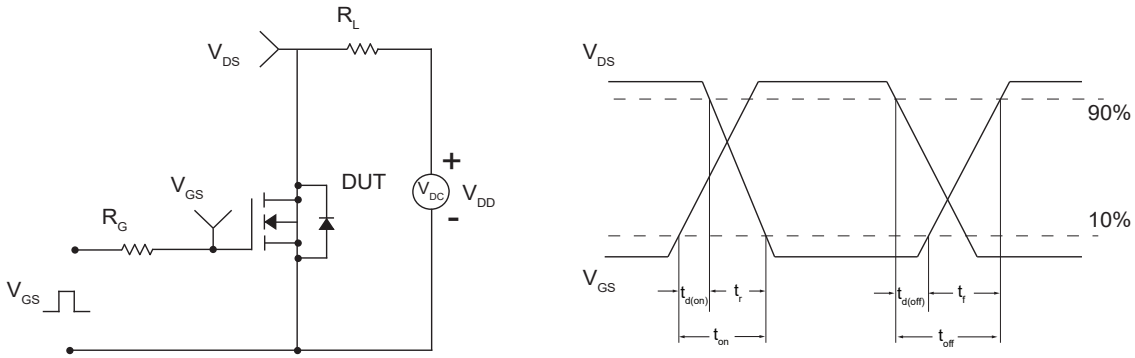


Figure 19. Resistive Switching Test Circuit and Waveforms

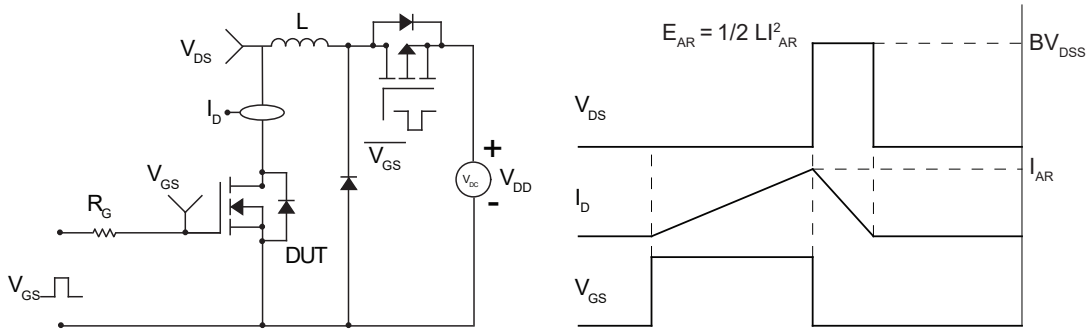


Figure 20. Unclamped Inductive Switching (UIS) Test Circuit and Waveforms

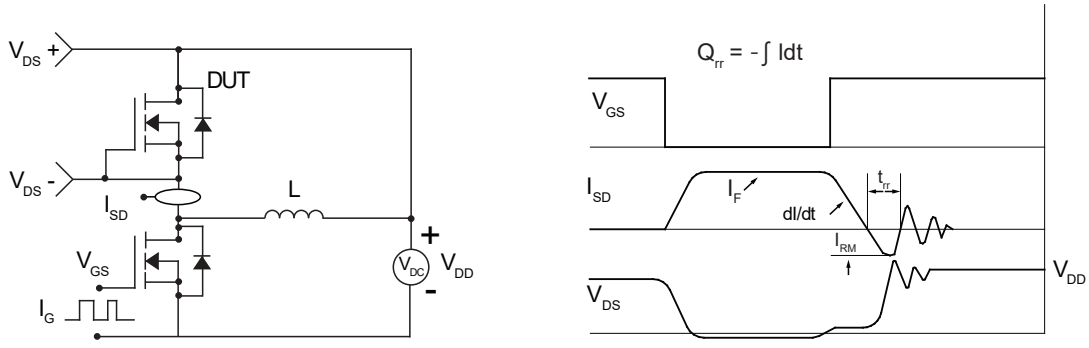
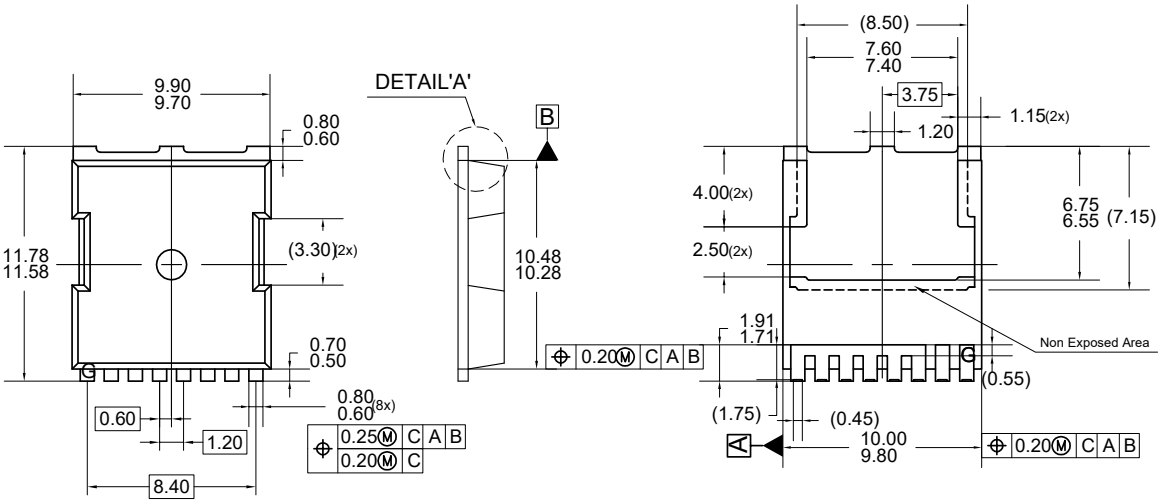
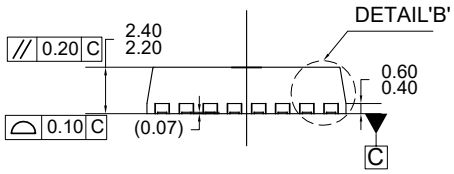


Figure 21. Diode Recovery Test Circuits and Waveforms

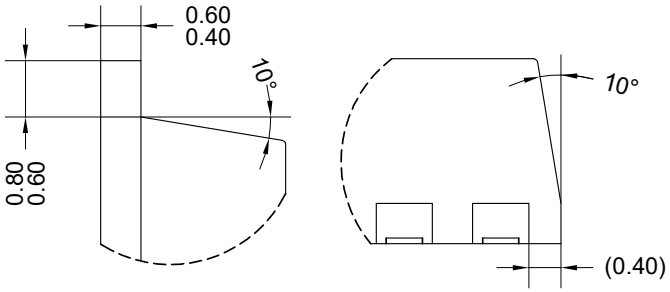
Package Dimensions, TOLL



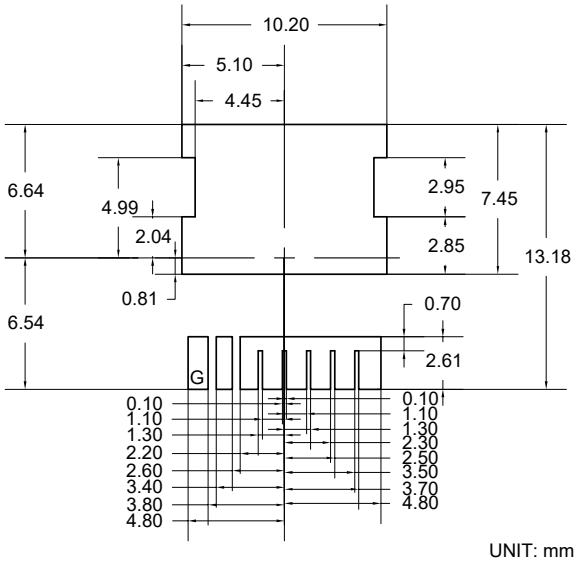
TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW



DETAIL 'A' DETAIL 'B'



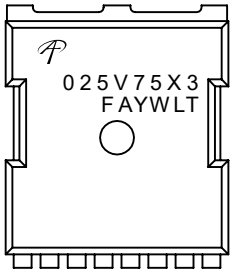
UNIT: mm

LAND PATTERN RECOMMENDATIONS

NOTE:

A) PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
B) TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
C) CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
D) ( ) IS REFERENCE.
E) THIS PACKAGE WAS QUALIFIED USING IR REFLOW PROCESS (JEDEC STANDARD). FOR USAGE IN OTHER SOLDERING PROCESSES, PLEASE CONTACT LOCAL AOS REPRESENTATIVES.

Part Marking



LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. Alpha and Omega Semiconductor does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.