AOTL040V65X2

650V αSiC Silicon Carbide Power MOSFET

Features

- Proprietary αSiC MOSFET technology
- Low loss, with low $R_{DS,(ON)}$
- Fast switching with low R_G and low capacitance
- Optimized gate drive voltage (V_{GS} = 15V)
- Low reverse recovery diode (Qrr)

Applications

Renewable
- EV Charger
- Solar Inverters

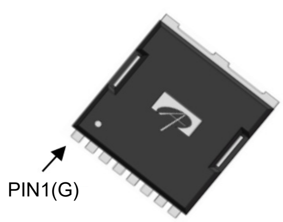
Industrial
- UPS
- SMPS
- Motor Drives

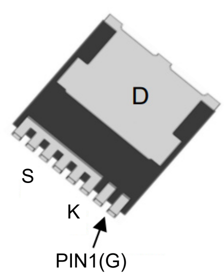
Product Summary

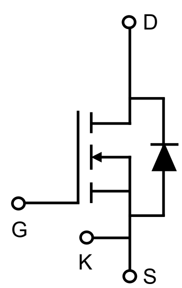
V_{DS} @ $T_{J, max}$	650V
I_{DM}	70A
$R_{DS(ON), typ}$	40mΩ
Q_{rr}	56nC
E_{OSS} @ 400V	13.4μJ
100 % UIS Tested	

GREEN Product

Pin Configuration







Ordering Part Number	Package Type	Form	Shipping Quantity
AOTL040V65X2	TOLL	Tape & Reel	2000/Reel

Absolute Maximum Ratings

(T_A = 25°C, unless otherwise noted)

Symbol	Parameter		AOTL040V65X2	Units
V_{DS}	Drain-Source Voltage		650	V
$V_{GS, MAX}$	Gate-Source Voltage	Maximum	-8/+18	V
$V_{GS,OP,TRANS}$		Max Transient(A)	-8/+20	
$V_{GS,OP}$		Recommended Operating(B)	-5/+15	
I_D	Continuous Drain Current	T_C = 25°C	37	A
		T_C = 100°C	26	
I_{DM}	Pulsed Drain Current(C)		70	
E_{AS}	Single Pulsed Avalanche Energy(D)		490	mJ
P_D	Power Dissipation(C)	T_C = 25°C	113	W
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 175	°C
T_L	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		260	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient(E,F)		40	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case(G)	1.10	1.32	°C/W

Electrical Characteristics

(T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V, T_J = 25°C		650			V
		I_D = 250µA, V_{GS} = 0V, T_J = 150°C		650			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V				100	µA
I_{GSS}	Gate-Body Leakage Current	V_{DS} = 0V, V_{GS} = +15/-5V				250	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 9mA		1.8	2.5	3.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 15V, I_D = 9A	T_J = 25°C		40	54	mΩ
			T_J = 175°C		61		
		V_{GS} = 18V, I_D = 9A	T_J = 25°C		33	45	
			T_J = 175°C		62		
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 9A			8		S
V_{SD}	Diode Forward Voltage	I_S = 9A, V_{GS} = -5V			4	5	V
DYNAMIC							
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 400V, f = 100kHz			1713		pF
C_{oss}	Output Capacitance				143		pF
C_{rss}	Reverse Transfer Capacitance				8		pF
E_{oss}	C_{oss} Stored Energy				13.4		µJ
R_G	Gate Resistance	f = 1MHz			1.4		Ω
SWITCHING							
Q_g	Total Gate Charge	V_{GS} = -5/+15V, V_{DS} = 520V, I_D = 9A			61		nC
Q_{gs}	Gate Source Charge				20		nC
Q_{gd}	Gate Drain Charge				16		nC
$t_{D(on)}$	Turn-On Delay Time	V_{GS} = -5V/+15V, V_{DS} = 400V, I_D = 30A, $R_{G,ON}$ = 2Ω, $R_{G,OFF}$ = 0Ω, L = 60µH, FWD: AOTL040V65X2			8.5		ns
t_r	Turn-On Rise Time				8		ns
$t_{D(off)}$	Turn-Off Delay Time				13		ns
t_f	Turn-Off Fall Time				4		ns
E_{on}	Turn-On Energy				87		µJ
E_{off}	Turn-Off Energy				5		µJ
E_{tot}	Total Switching Energy				92		µJ
t_{rr}	Body Diode Reverse Recovery Time	I_F = 30A, dI/dt = 1500A/µs, V_{DS} = 400V			13		ns
I_{rm}	Peak Reverse Recovery Current				9		A
Q_{rr}	Body Diode Reverse Recovery Charge				56		nC

Notes:
A. t_{ON} < 1% *(Duty Cycle)/(Frequency), t < 25 hrs over lifetime
B. Device can be operated at V_{GS} = 0/15V. Actual operating V_{GS} will depend on application specifics such as parasitic inductance and dV/dt but should not exceed maximum ratings.
C. The power dissipation P_D is based on $T_{J(MAX)}$ = 175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
D. L = 5mH, I_{AS} = 14A, R_G = 10Ω, Starting T_J = 25°C.
E. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A = 25°C.
F. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
G. The value of $R_{\theta JC}$ is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ = 175°C.
H. The static characteristics in Figures 1 to 8 are obtained using < 300µs pulses, duty cycle 0.5% max.
I. These curves are based on $R_{\theta JC}$ which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ = 175°C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

T_A = 25°C, unless otherwise specified.

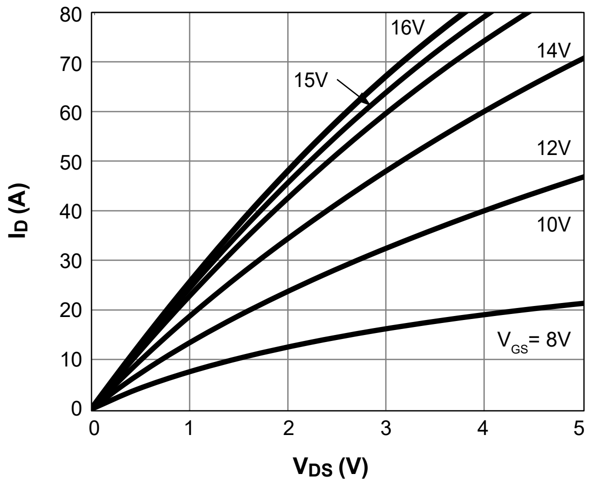


Figure 1. On-region Characteristics T_J = 25°C

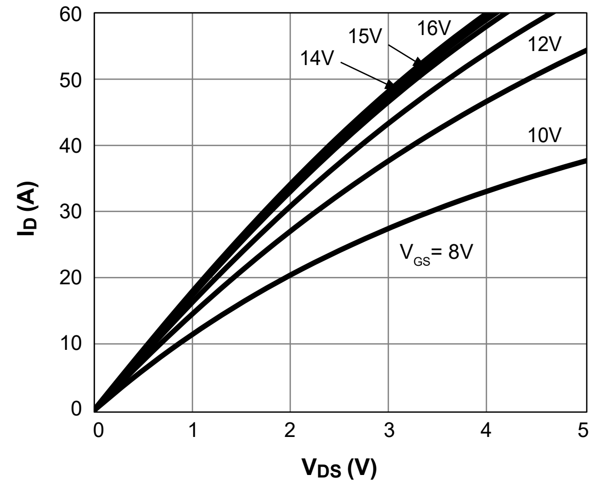


Figure 2. On-region Characteristics T_J = 175°C

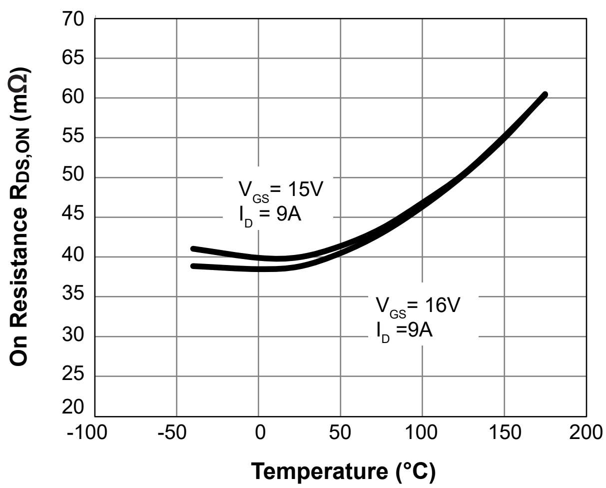


Figure 3. On-resistance vs. Junction Temperature

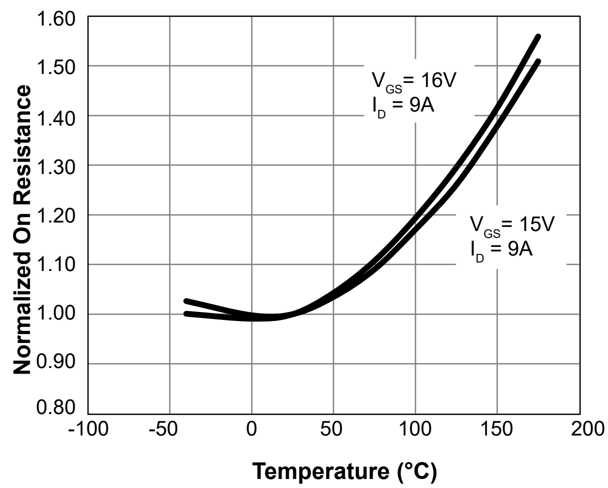


Figure 4. Normalized On-resistance vs. Junction Temperature

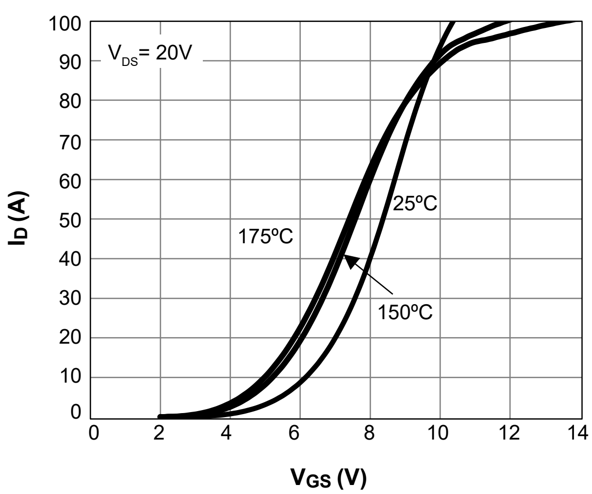


Figure 5. Transfer Characteristics

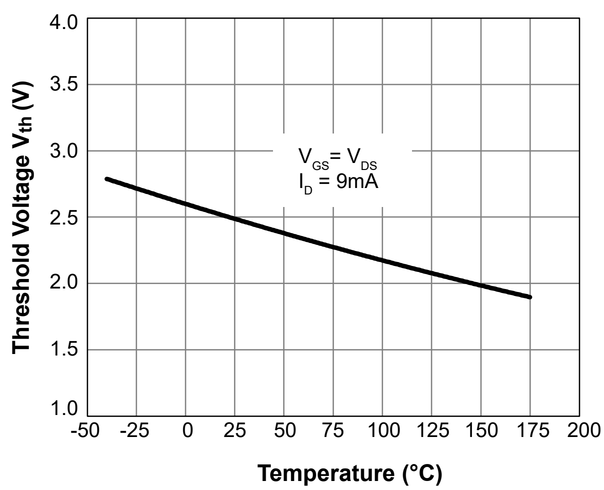


Figure 6. Threshold Voltage vs. Junction Temperature

Typical Electrical and Thermal Characteristics

T_A = 25°C, unless otherwise specified.

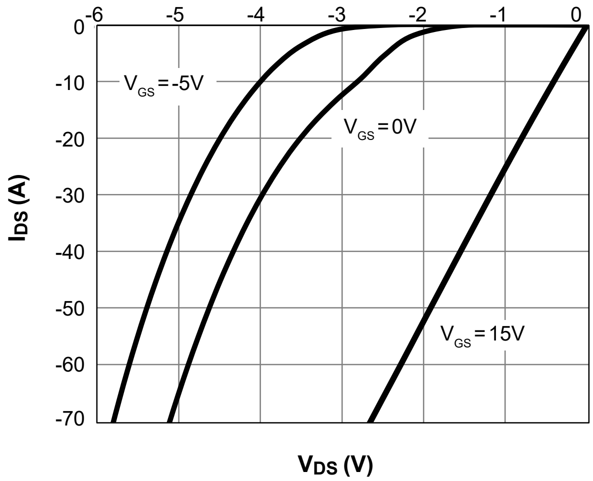


Figure 7. Body-diode Characteristics T_J = 25°C

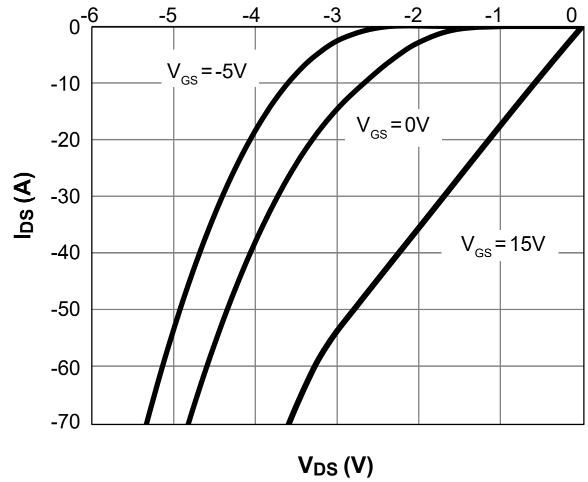


Figure 8. Body-diode Characteristics T_J = 175°C

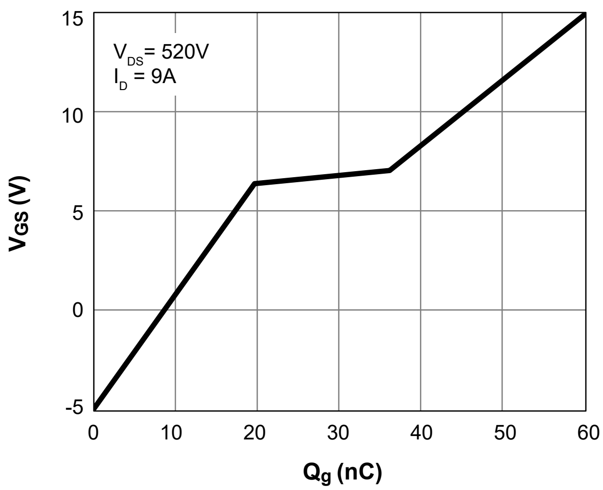


Figure 9. Gate-charge Characteristics

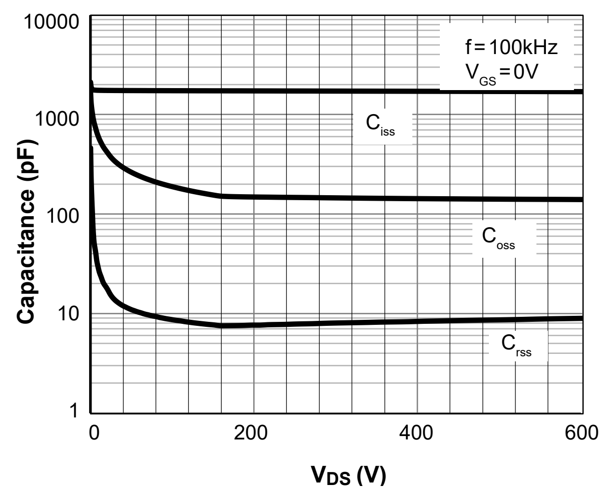


Figure 10. Capacitance Characteristics

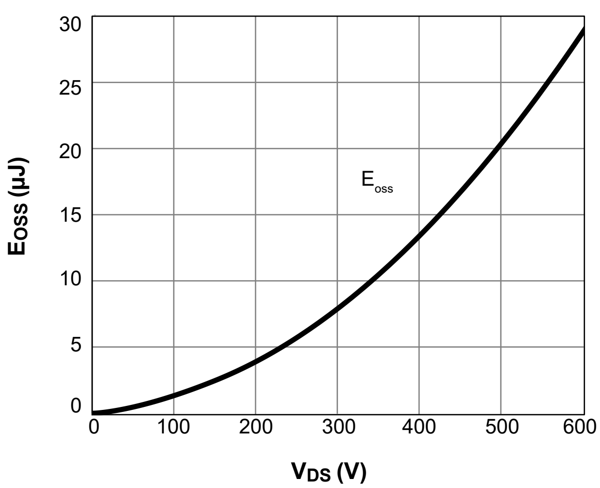


Figure 11. Coss Stored Energy

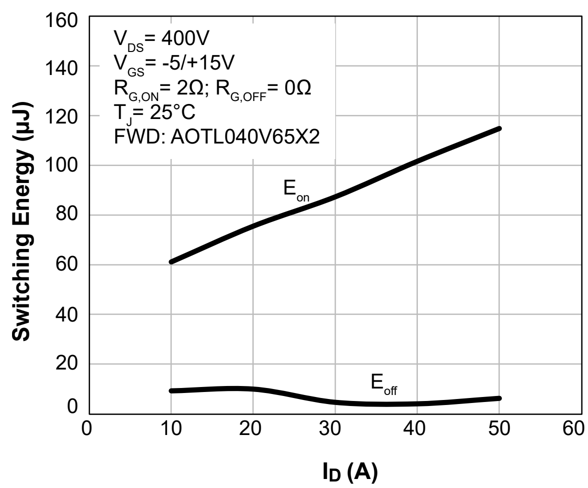


Figure 12. Switching Energy vs. Drain Current

Typical Electrical and Thermal Characteristics *(Continued)*

T_A = 25°C, unless otherwise specified.

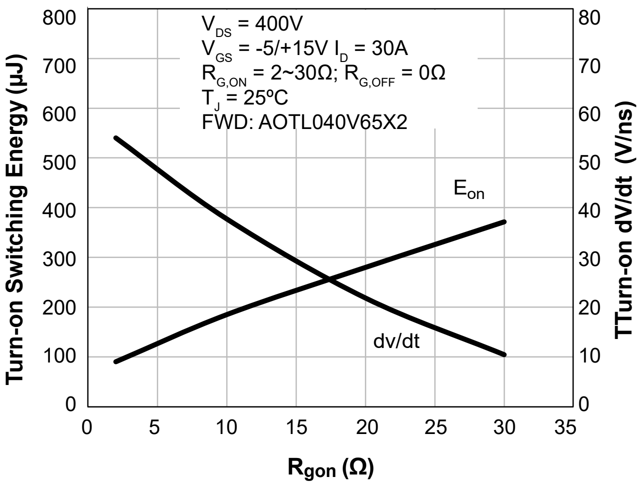


Figure 13. Turn-On Energy and dV/dt vs. External Gate Resistance

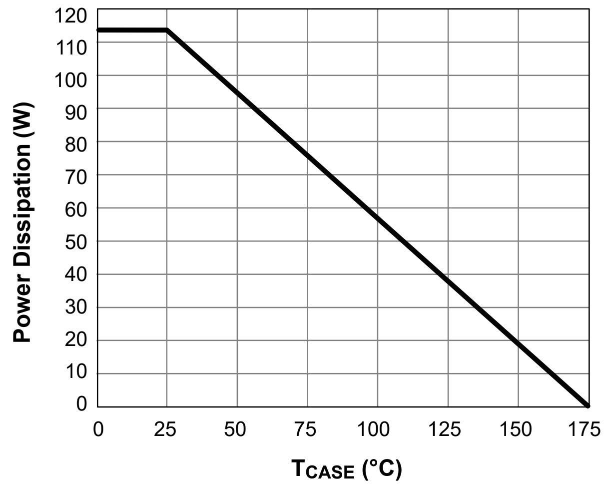


Figure 14. Power De-rating (Note I)

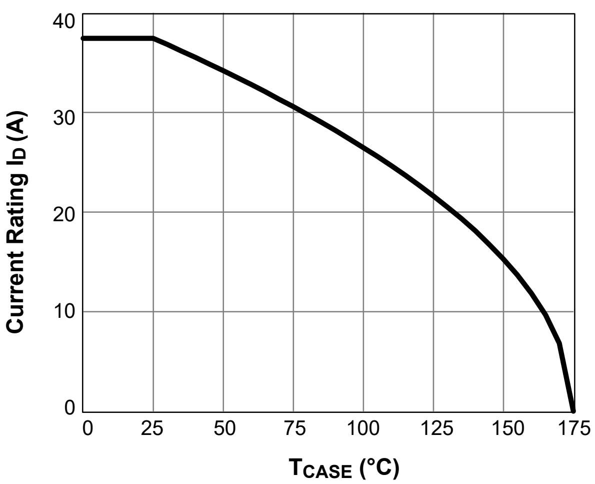


Figure 15. Current De-rating (Note I)

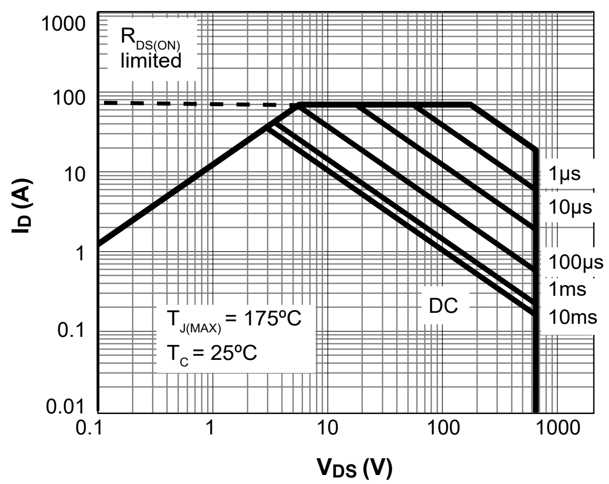


Figure 16. Maximum Forward Biased Safe Operating Area for AOTL040V65X2 (Note I)

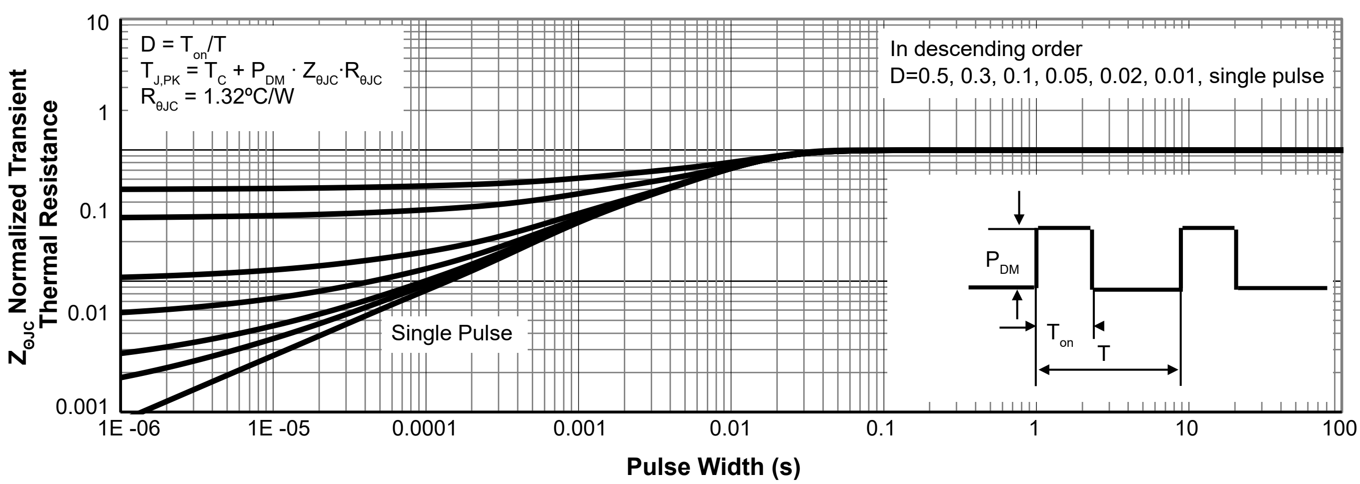


Figure 17. Normalized Maximum Transient Thermal Impedance for AOTL040V65X2 (Note I)

Test Circuits and Waveforms

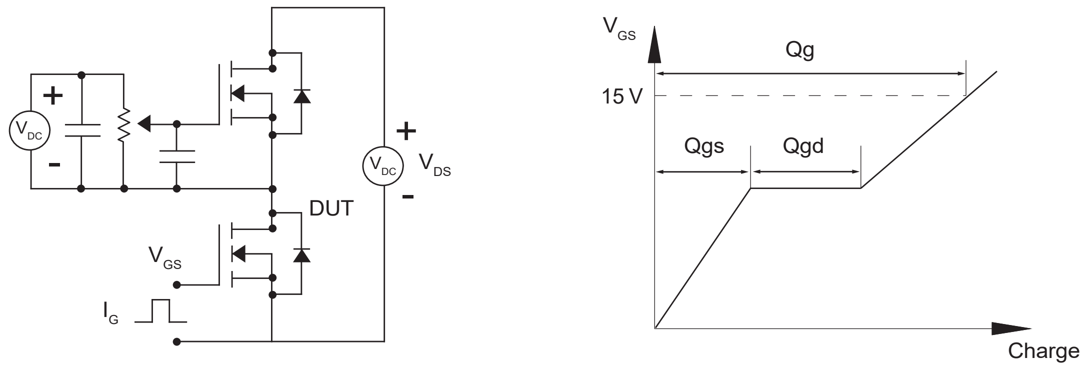


Figure 18. Gate Charge Test Circuits and Waveforms

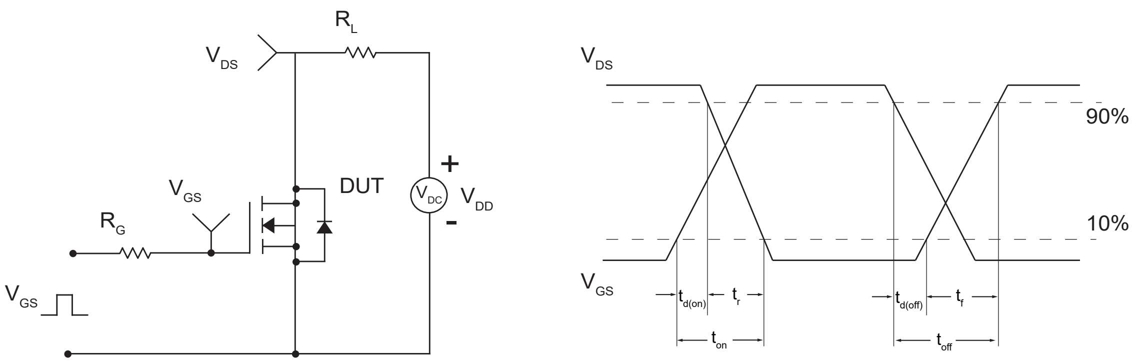


Figure 19. Resistive Switching Test Circuit and Waveforms

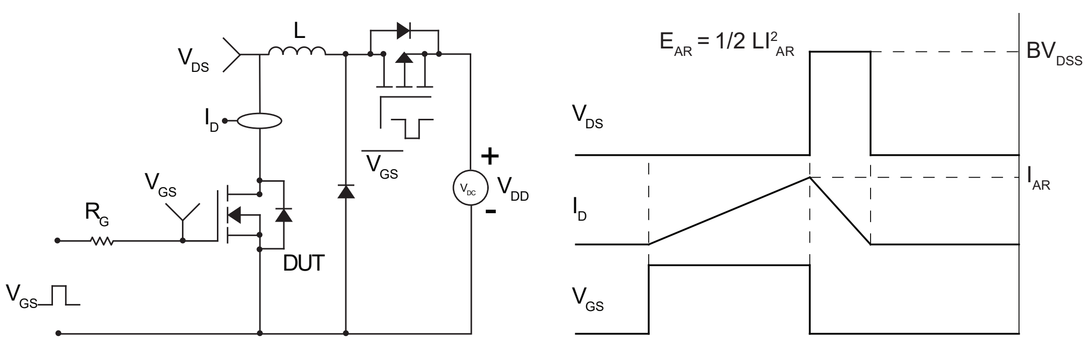


Figure 20. Unclamped Inductive Switching (UIS) Test Circuit and Waveforms

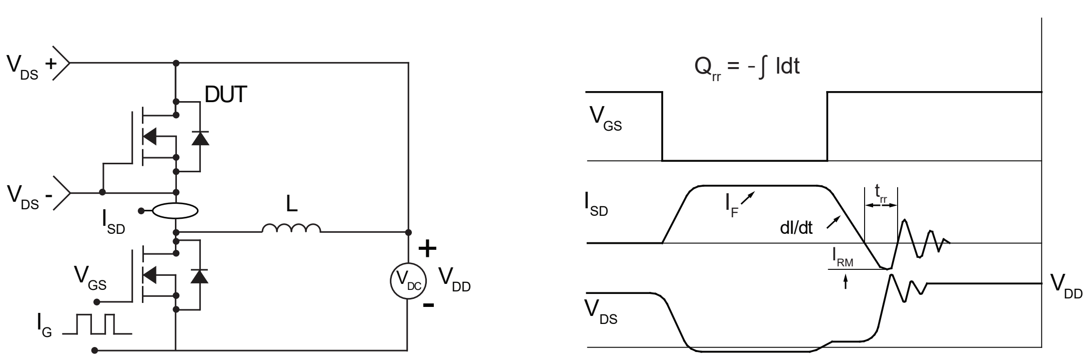
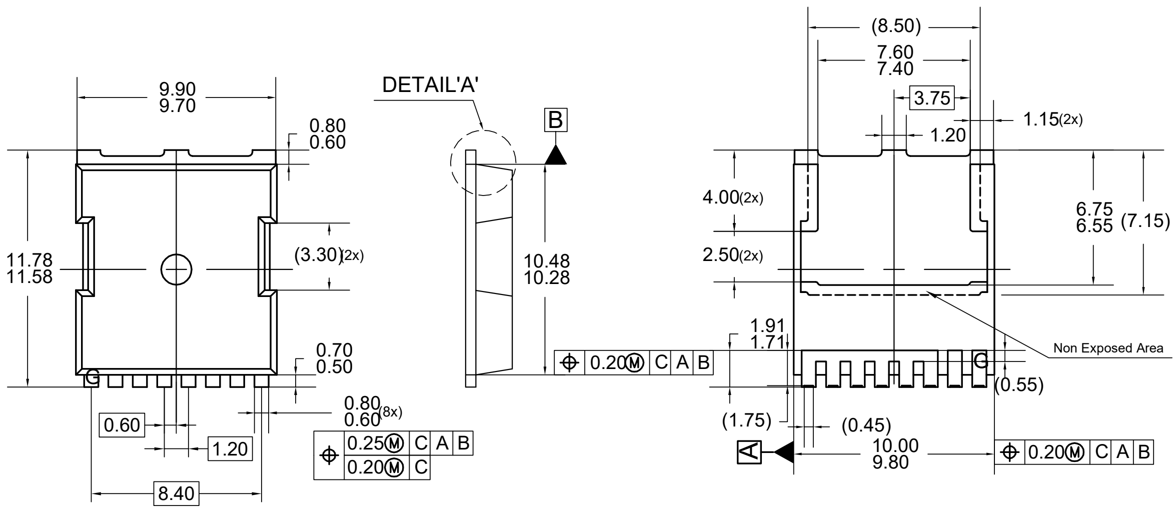
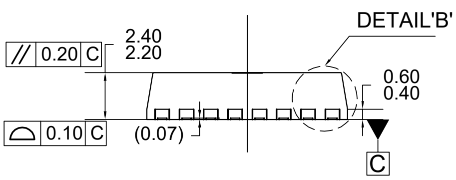


Figure 21. Diode Recovery Test Circuits and Waveforms

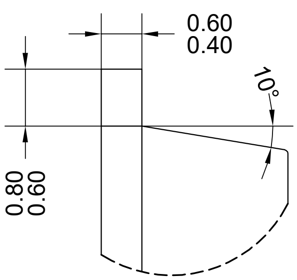
Package Dimensions, TOLL



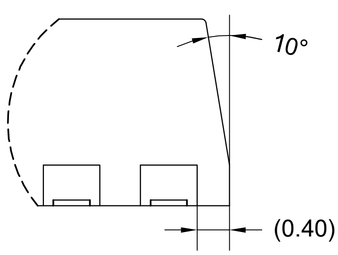
TOP VIEW SIDE VIEW BOTTOM VIEW



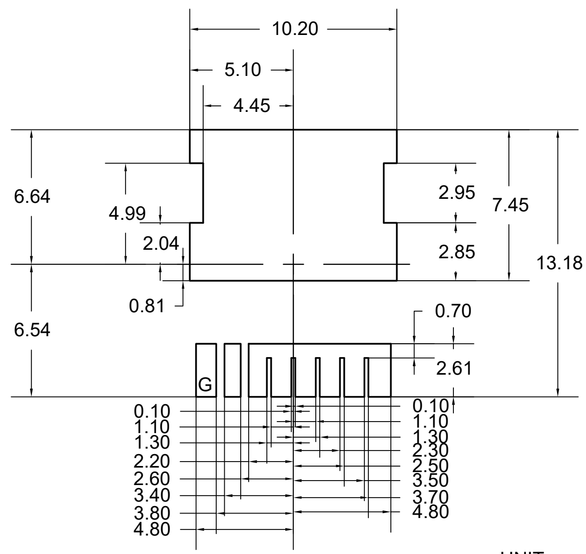
SIDE VIEW



DETAIL 'A'



DETAIL 'B'



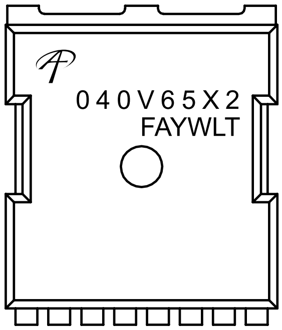
UNIT: mm

LAND PATTERN RECOMMENDATIONS

NOTE:

A) PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
B) TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
C) CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
D) ( ) IS REFERENCE.
E) THIS PACKAGE WAS QUALIFIED USING IR REFLOW PROCESS (JEDEC STANDARD). FOR USAGE IN OTHER SOLDERING PROCESSES, PLEASE CONTACT LOCAL AOS REPRESENTATIVES.

Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.