ALPHA & OMEGA SEMICONDUCTOR

AOTL66518Q

150V N-Channel AlphaSGT™

AEC-Q101 Qualified

General Description

- AEC-Q101 Qualified
- Trench Power MOSFET - AlphaSGT™ technology
- Combined of low $R_{DS(ON)}$ and wide safe operatiing area (SOA)
- Higher in-rush current enabled for faster start-up and shorter down time
- RoHS 2.0 and Halogen-Free Compliant

Applications

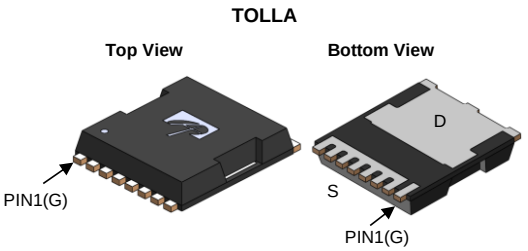
- Load switch
- BMS
- Motor

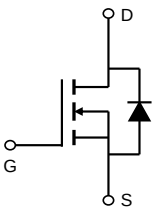
Product Summary

V_{DS}	150V
I_D (at V_{GS}=10V)	206A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 4.7mΩ
$R_{DS(ON)}$ (at V_{GS}=8V)	< 5.3mΩ

100% UIS Tested
100% Rg Tested

Max Tj=175°C





Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOTL66518Q	TOLLA	Tape & Reel	2000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	206	A
	T_C=100°C		145	
Pulsed Drain Current [C] (≤100μS)		I_{DM}	824	
Continuous Drain Current	T_A=25°C	I_{DSM}	29	A
	T_A=70°C		24	
Avalanche Current [C]		I_{AS}	70	A
Avalanche energy L=0.3mH [C]		E_{AS}	735	mJ
Diode reverse recovery V_{DS}=0 to 75V, I_F≤300A, T_J≤125°C		di/dt	500	A/us
Power Dissipation [B]	T_C=25°C	P_D	500	W
	T_C=100°C		250	
Power Dissipation [A]	T_A=25°C	P_{DSM}	10	W
	T_A=70°C		7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	10	15	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		35	45	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.2	0.3	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	150			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=150V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	2.7	3.2	3.7	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=100A		3.9	4.7	mΩ
		T_J=175°C		9.7	12	
		V_{GS}=8V, I_D=75A		4.2	5.3	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.68	1	V
I_S	Maximum Body-Diode Continuous Current				200	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=75V, f=1MHz		6460		pF
C_{oss}	Output Capacitance			820		pF
C_{rss}	Reverse Transfer Capacitance			5		pF
R_g	Gate resistance	f=1MHz	1.1	2.3	3.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=75V, I_D=20A		80	115	nC
Q_{gs}	Gate Source Charge			32		nC
Q_{gd}	Gate Drain Charge			15		nC
Q_{oss}	Output Charge	V_{GS}=0V, V_{DS}=75V		273		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=75V, R_L=3.75Ω, R_{GEN}=3Ω		27		ns
t_r	Turn-On Rise Time			20		ns
$t_{D(off)}$	Turn-Off DelayTime			49		ns
t_f	Turn-Off Fall Time			28		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs		86		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs		920		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

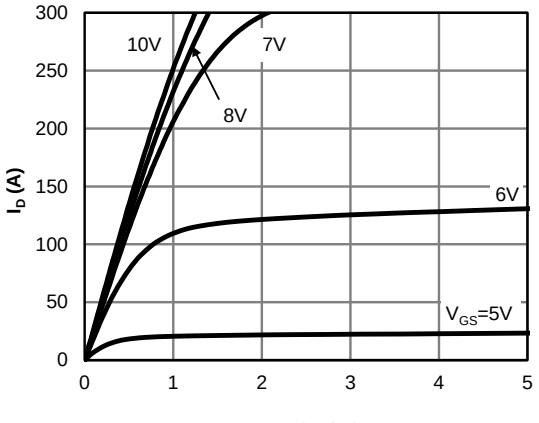


Figure 1: On-Region Characteristics (Note E)

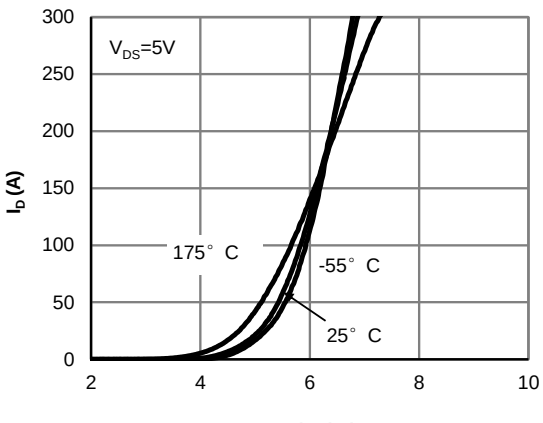


Figure 2: Transfer Characteristics (Note E)

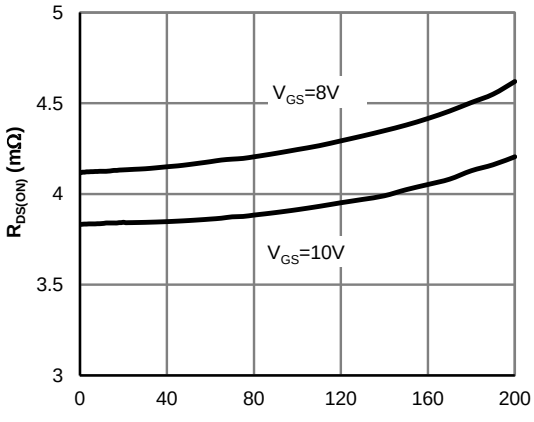


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

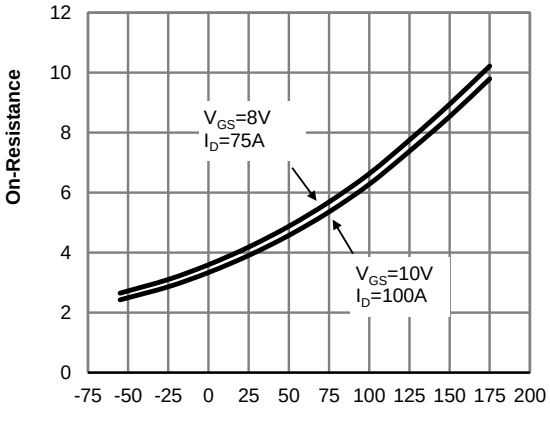


Figure 4: On-Resistance vs. Junction Temperature (Note E)

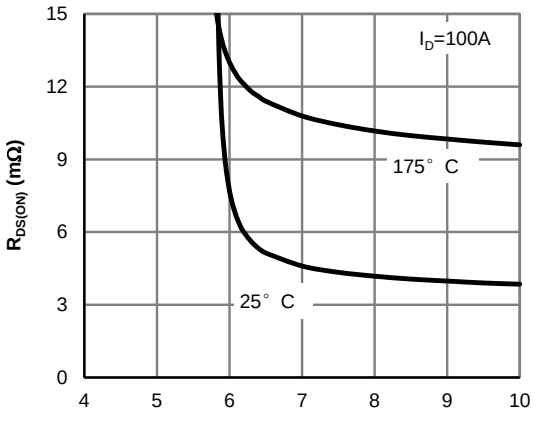


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

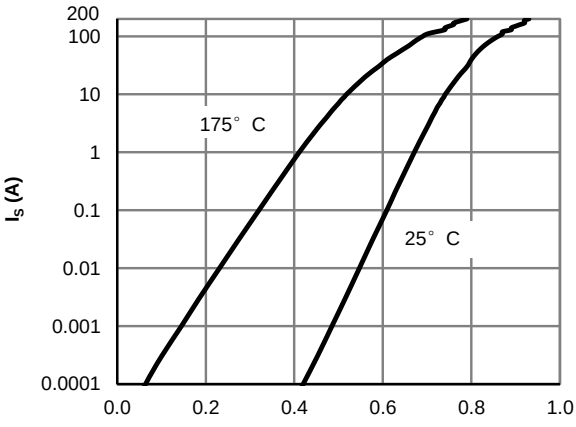


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

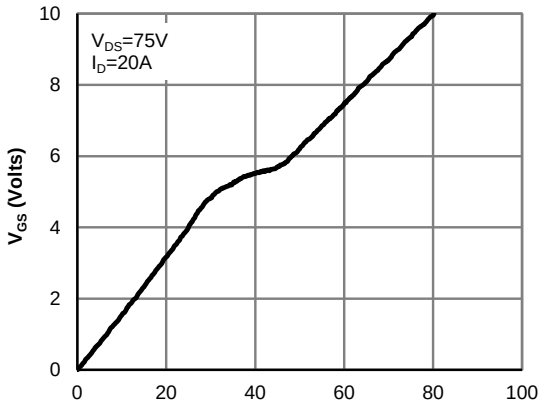


Figure 7: Gate-Charge Characteristics

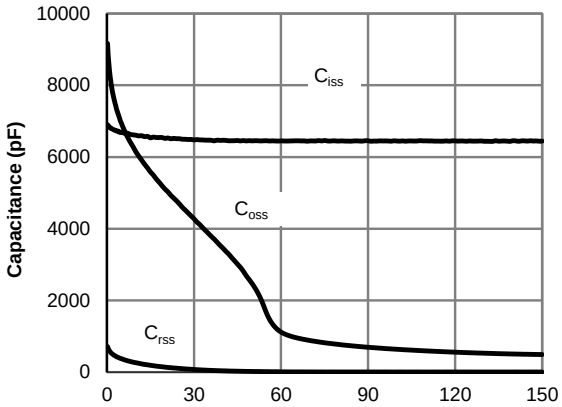
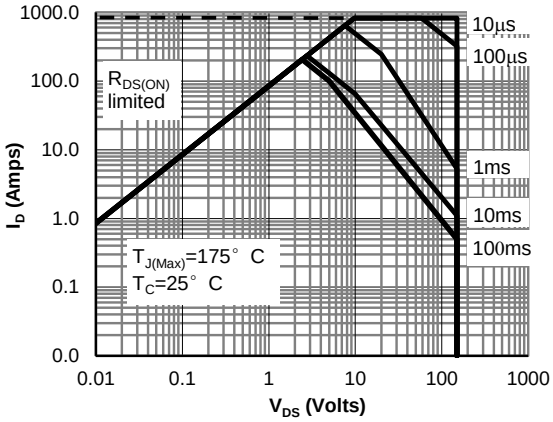


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 8V

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

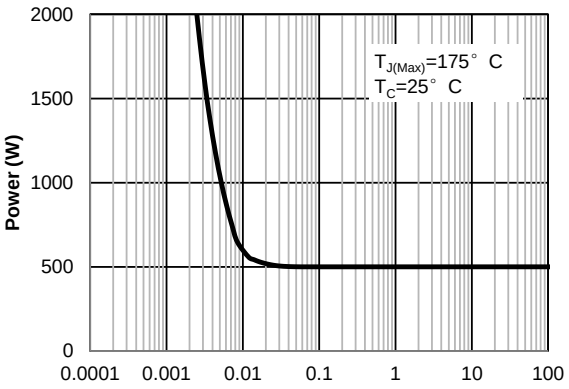


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

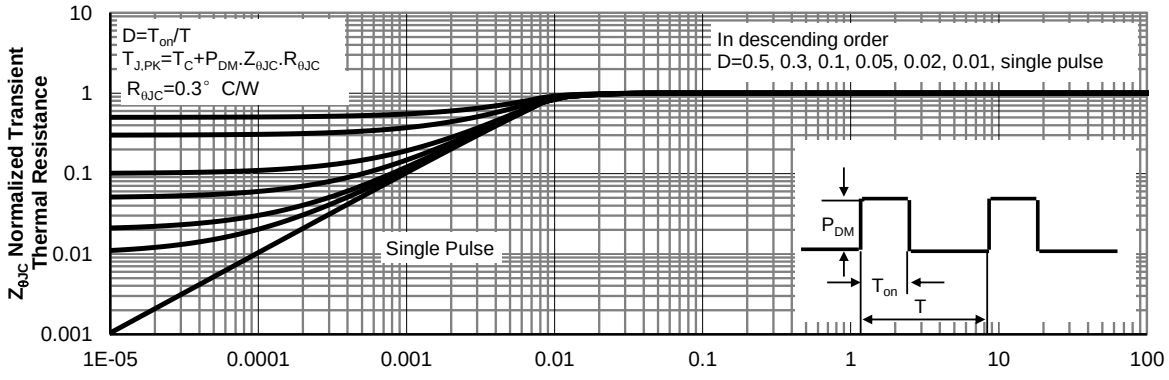


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

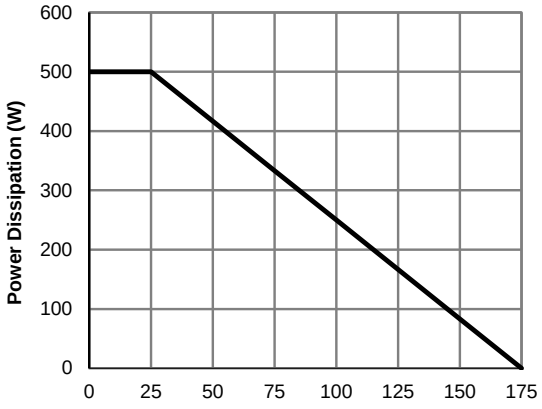


Figure 12: Power De-rating (Note F)

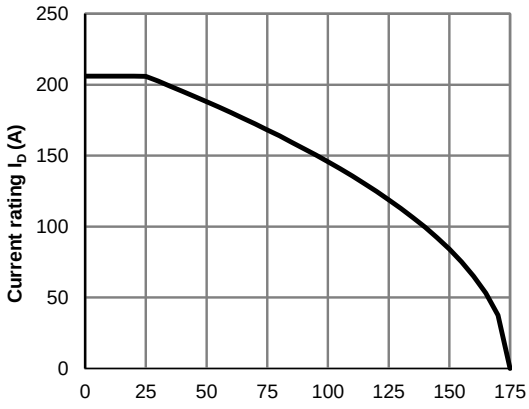


Figure 13: Current De-rating (Note F)

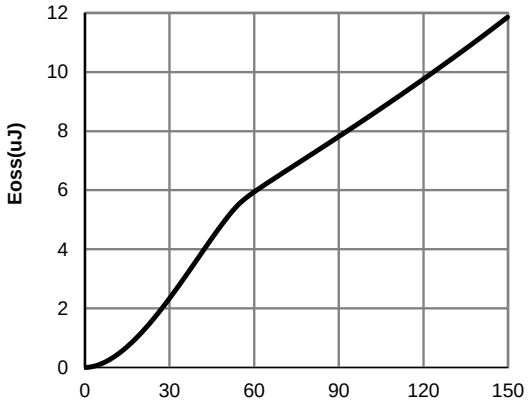


Figure 14: Coss stored Energy

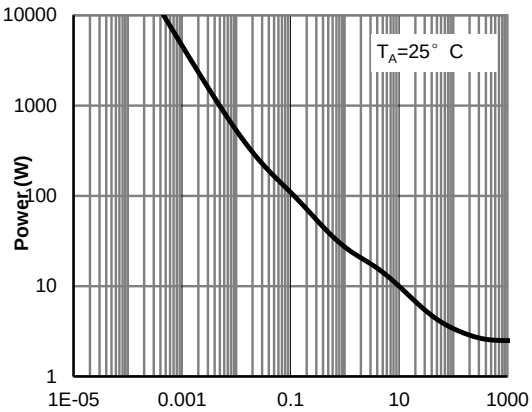


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

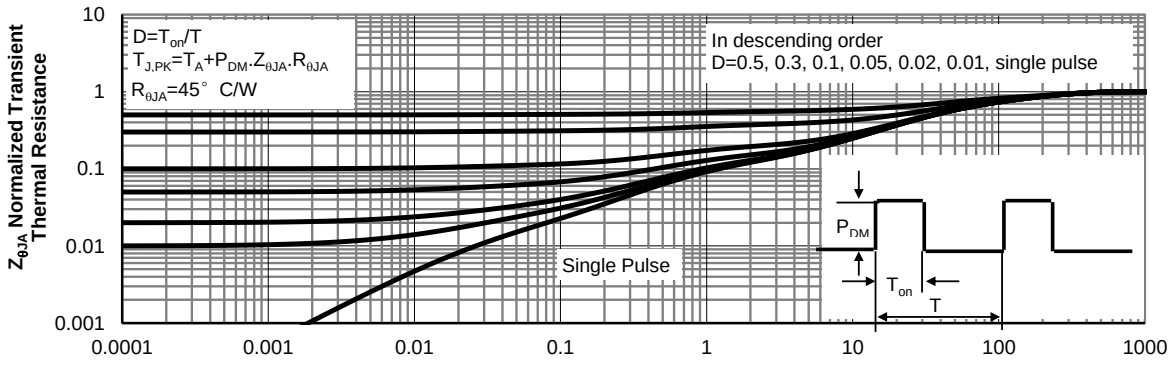


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

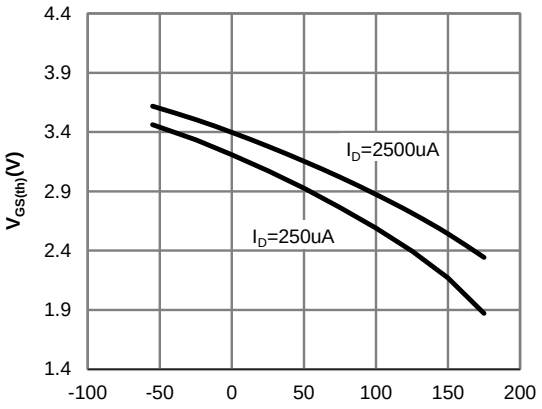


Figure 17: $E_{GS(th)}$ vs Junction Temperature

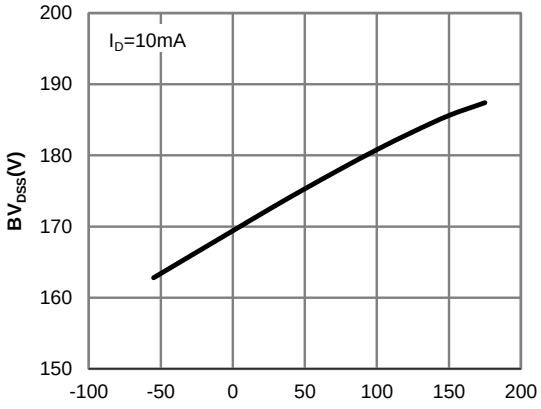


Figure 18: Drain-source breakdown voltage vs. Junction Temperature

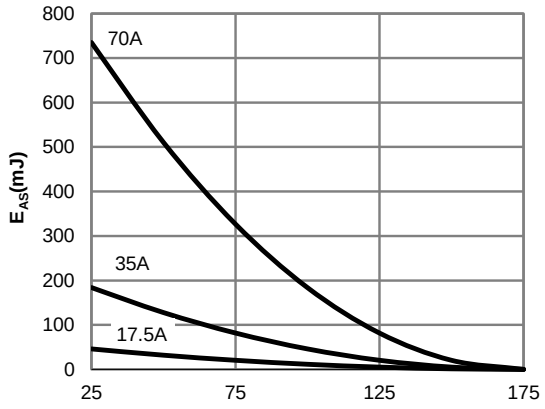


Figure 19: EAS vs. Junction Temperature

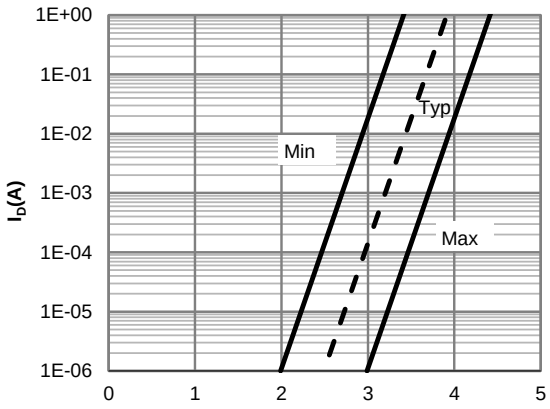


Figure 20: Transfer Characteristics (Note E)

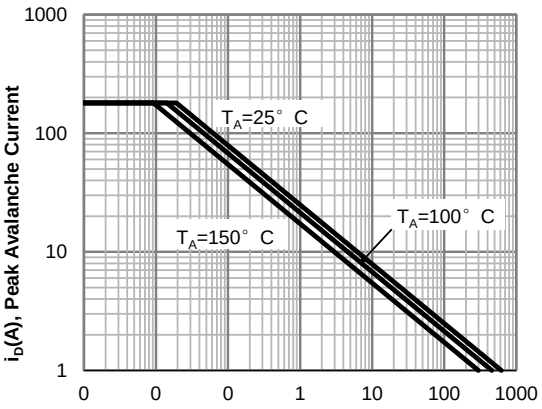


Figure 21: Single Pulse Avalanche capability

Figure A: Gate Charge Test Circuit & Waveforms

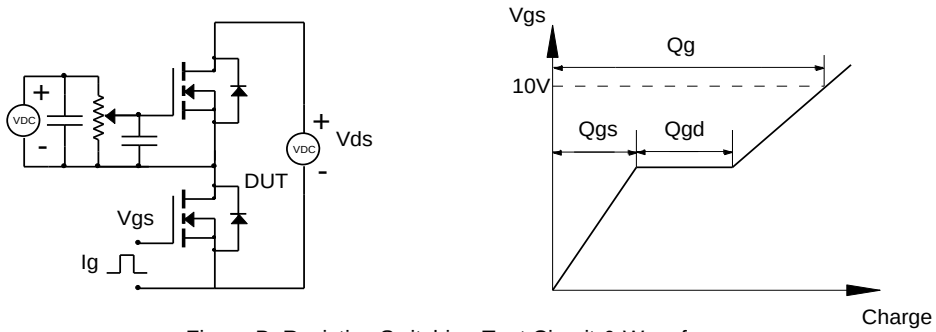


Figure B: Resistive Switching Test Circuit & Waveforms

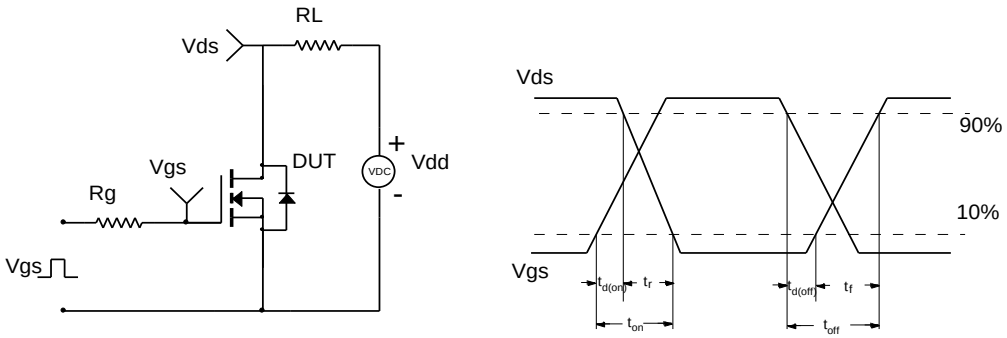


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

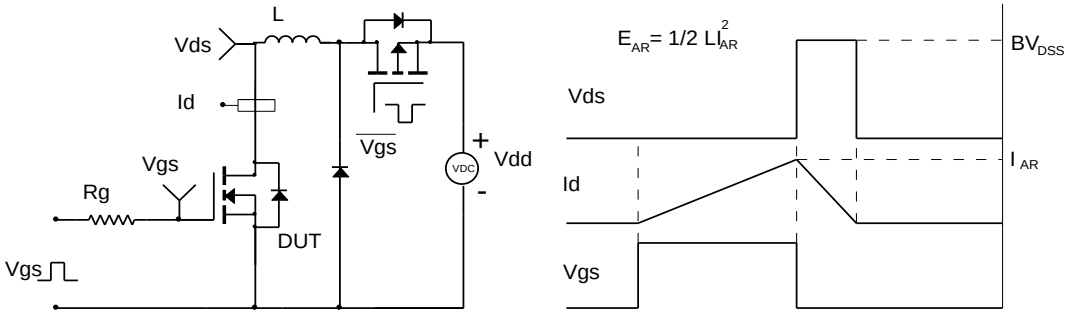


Figure D: Diode Recovery Test Circuit & Waveforms