ALPHA & OMEGA SEMICONDUCTOR

AOZ18102DI

13.8V 21mΩ Over-Voltage Protection eFuse with External Blocking FET Control

General Description

AOZ18102DI is a current-limiting over-voltage protection eFuse targeting applications that require front end protection at the input line. Both VIN and VOUT terminals are rated at 20V absolute maximum. There is a programmable soft-start feature that controls the inrush current for highly capacitive loads. It also has Input Under-Voltage Lock Out (UVLO), Input Over-Voltage Output Clamp (OVC), and Thermal Shut Down Protection (TSD).

AOZ18102DI features an internal current-limiting circuit that protects the supply from large load current. The current limit threshold can be set externally with a resistor.

AOZ18102DI-01 is auto-restart version after fault condition.

AOZ18102DI-02 is latch-off version after fault is detected.

AOZ18102DI is available in small 3mm x 3mm 10-pin DFN package.

Features

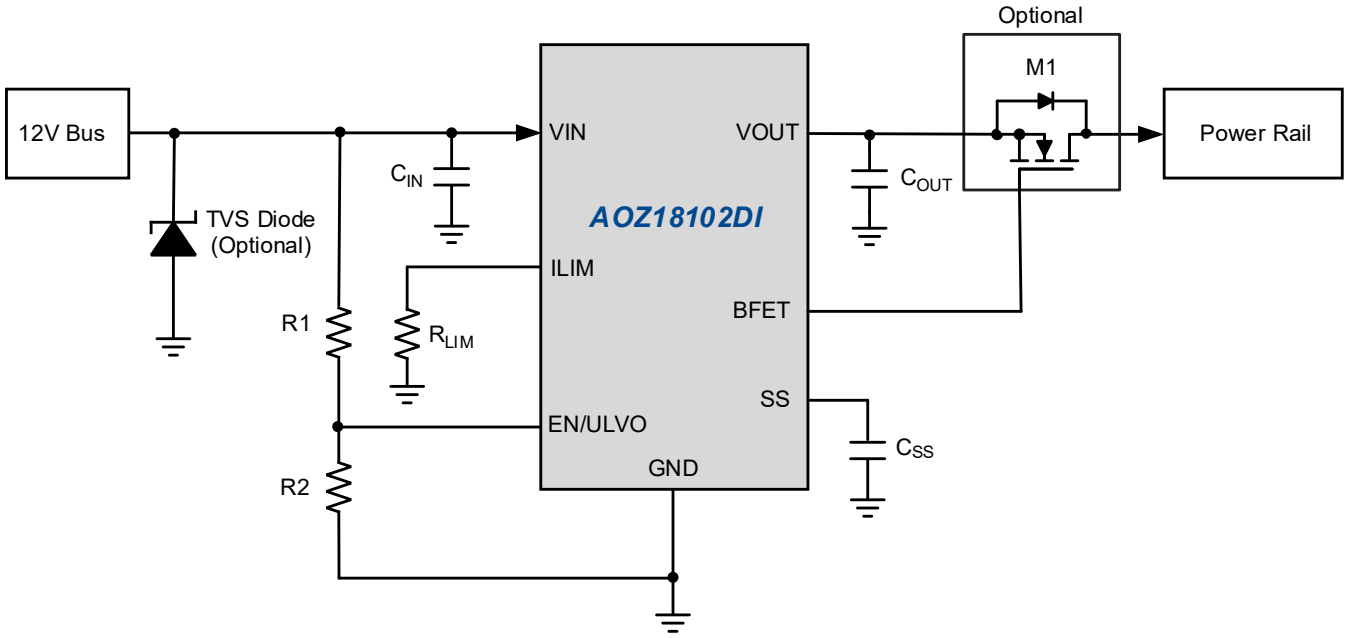
- 3.5V to 13.8V input voltage operating range
- 20V abs max voltage rating on VIN and VOUT pin
- Typical RON: 21mΩ
- 1A to 5A programmable current limit
- Programmable output soft-start time
- Fast Over Current Protection (OCP)
- Input Over-Voltage Output Clamp (OVC)
- Input Under-Voltage Lock Out (UVLO)
- Thermal Shut Down Protection (TSD)
- ±2kV HBM ESD rating
- ±1kV CDM ESD rating
- IEC 61000-4-2: ±8kV on VIN and VOUT
- IEC 61000-4-5: ± 35V on VIN, No cap

Applications

- Servers
- HDD and SSD drives
- PCI cards
- Networking

GREEN Product

Typical Application



Ordering Information

Part Number	Fault Recovery	Operating Voltage Range	Package	Environmental
AOZ18102DI-01	Auto-Restart	3.5V – 13.8V	DFN3x3-10L	RoHS
AOZ18102DI-02	Latch-Off	3.5V – 13.8V	DFN3x3-10L	RoHS

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

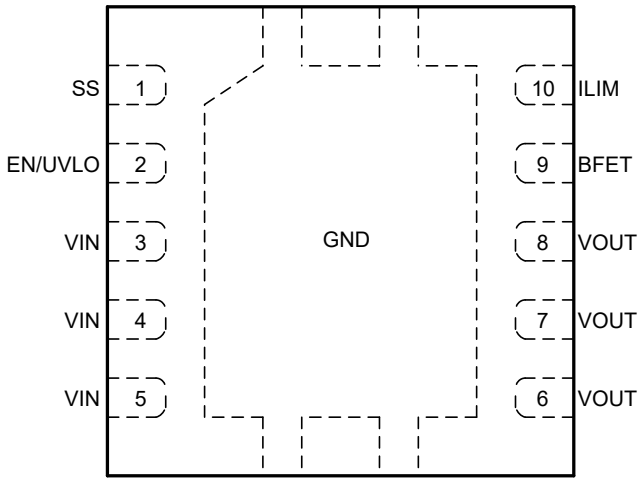


Figure 1. DFN3x3-10L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	SS	Soft-start control. Connect a capacitor C_{SS} from SS to GND to set the soft-start time.
2	EN/UVLO	Enable input. Active high. It can be used as UVLO by connecting resistor divider from VIN. EN/UVLO cannot be left floating.
3, 4, 5	VIN	Supply input. Connected to main power supply. They are internally connected together.
6, 7, 8	VOUT	Power output. They are internally connected together.
9	BFET	External blocking FET gate control. This pin can be left open when it is not used. When external blocking FET is used, connect this pin to the gate of the blocking FET.
10	ILIM	Current limit set pin. Connect a 1% resistor RLIM from ILIM to GND to set the current limit threshold.
EXP	GND	Ground. Connect to GND. For best thermal performance make the ground copper pads as large as possible and connect to EXP to the ground plane through multiple thermal VIAs.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN, VOUT to GND	-0.3V to 20V
VOUT to GND (transient < 1µs)	-1.2V to 22V
EN/UVLO, ILIM, SS to GND	-0.3V to 6V
BFET to GND	-0.3V to 20V
Continuous Output Current	6.25A
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating HBM All Pins	±2kV
IEC 61000-4-2: VOUT and VIN	±8kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
VIN, VOUT to GND	3.5V to 13.8V
BFET to GND	0V to VOUT+6V
EN/UVLO, ILIM, SS to GND	0V to 5.5V
Switch DC Current (I_{SW})	0A to 5A
Junction Temperature (T_J)	-40°C to +125°C
Package Thermal Resistance (R_{JA})	29°C/W
Package Thermal Resistance- Junction to Top case (R_{JC})	11°C/W

Electrical Characteristics

T_A = -40°C to 125°C, VIN = 12V, EN = 5V, R_{LIM} = 100kΩ, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
V_{VIN}	Input Supply Voltage		3.5		13.8	V
V_{UVLO_R}	Under-voltage Lockout Threshold	VIN rising	2.9		3.4	V
V_{UVLO_HYS}	Under-voltage Lockout Hysteresis	VIN falling		250		mV
I_{IN_ON}	Input Quiescent Current	IOUT = 0 A		550		µA
I_{IN_OFF}	Input Shutdown Current	EN/UVLO = 0 V		130		µA
V_{OVC}	Input Over-Voltage Protection Output Clamp Voltage	VIN = 17V, I_{OUT} = 10mA	14.0	15.0	16.5	V
R_{ON}	Switch ON-Resistance	VIN = 12V, I_{OUT} = 1A		21		mΩ
		VIN = 5V, I_{OUT} = 1A		22		
V_{EN_H}	Enable Input Logic High Threshold	EN/UVLO rising	1.3	1.40	1.45	V
V_{EN_L}	Enable Input Logic Low Threshold	EN/UVLO falling	1.2	1.35	1.4	V
I_{EN_BIAS}	Enable Input Bias Current	EN/UVLO = 1.8 V	-100		100	nA

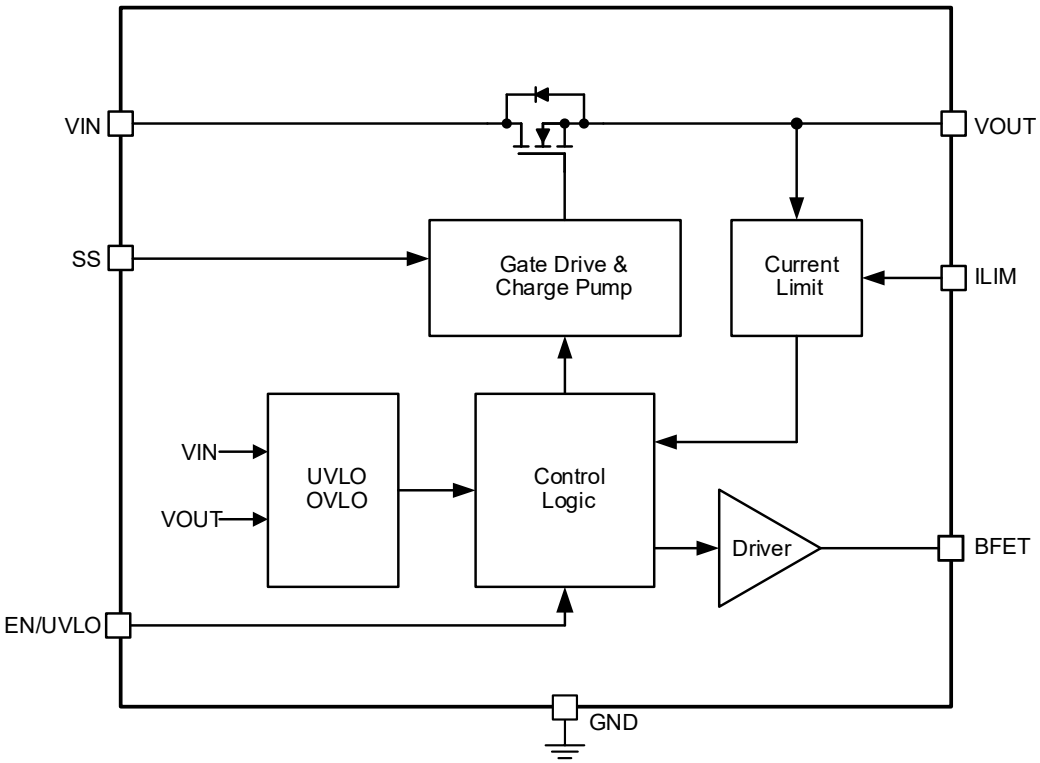
Electrical Characteristics

T_A = -40°C to 125°C, VIN = 12V, EN = 5V, R_{LIM} = 100kΩ, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Dynamic Characteristics						
t_{D_ON}	Turn-on Delay Time	From EN/UVLO > V_{EN_H} to VOUT=0.1V. C_{SS} = open		600		µs
t_{ON}	Turn-on Time (VOUT from 0.1V to 11.7V)	C_{SS} = open		900		µs
		C_{SS} = 1nF		10		ms
t_{D_OFF}	Turn-off Delay Time	From EN/UVLO < V_{EN_L} to V_{BFET} = falling down to 12V, C_{BFET} = 0		0.5		µs
t_{BFET_ON}	BFET Turn-on Time	From EN/UVLO > V_{EN_H} To V_{BFET} = rising above to 12V, C_{BFET} = 1nF		1.3		ms
		From EN/UVLO > V_{EN_H} to V_{BFET} = rising above to 12V, C_{BFET} = 10nF		12		ms
t_{BFET_OFF}	BFET Turn-off Time	From EN/UVLO < V_{EN_L} to V_{BFET} = falling down to 12V, C_{BFET} = 1nF		2		µs
		From EN/UVLO < V_{EN_L} to V_{BFET} = falling down to 12V, C_{BFET} = 10nF		11		µs
Over Current Protection (OCP)						
I_{LIM}	Current Limit Threshold	R_{LIM} = 150kΩ	4.50	5.10	5.70	A
		R_{LIM} = 100kΩ	3.46	3.75	4.03	
		R_{LIM} = 45.3kΩ	1.79	2.10	2.42	
		R_{LIM} = 10kΩ		1.00		
		R_{LIM} = 0 or Open		0.75		
I_{OCP_FAST}	Fast OCP Threshold for Current Spike	Based on I_{LIM} value		160		%
t_{OCP_FAST}	Fast OCP Response Time	From I_{OUT} ≥ (I_{LIM} x 160%)		300		ns
I_{LIM_SS} (1)	Current limit during SS	V_{OUT} = 0V		1.5		A
$T_{timeout\_SS}$ (1)	Current limit time out during SS			250		µs
$T_{timeout\_SS}$ (1)	Current limit time out after SS	After Vout reaches 90% of Vin		512		µs
Blocking FET Driver						
I_{BFET}	BFET Driving Current	BFET = VOUT		10		µA
R_{BFET_DIS}	BFET Discharge Resistance			4		kΩ
Thermal Shutdown (TSD)						
T_{SD}	Thermal Shutdown Threshold	Temperature rising		140		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis	Temperature falling (AOZ18102DI-01 only)		30		°C

Note:
1. Guaranteed by characterization and design.

Functional Block Diagram



Timing Diagrams

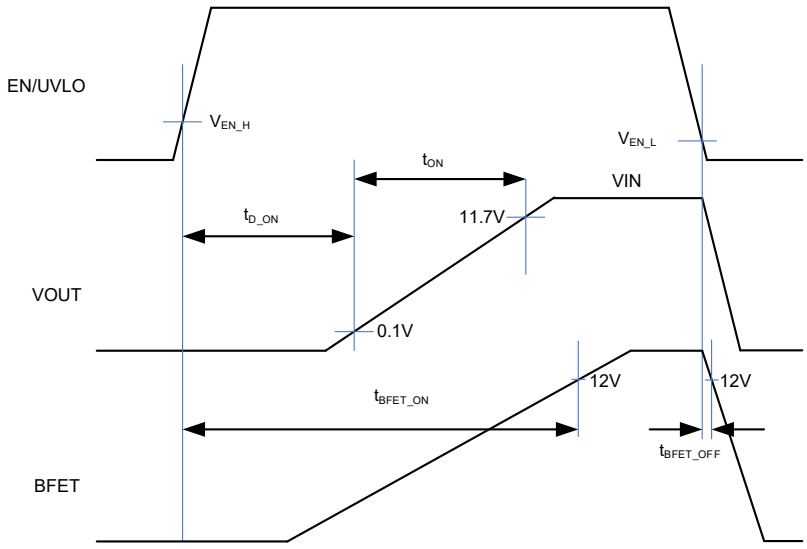


Figure 2. Turn-on Delay, Turn-on and Turn-off time

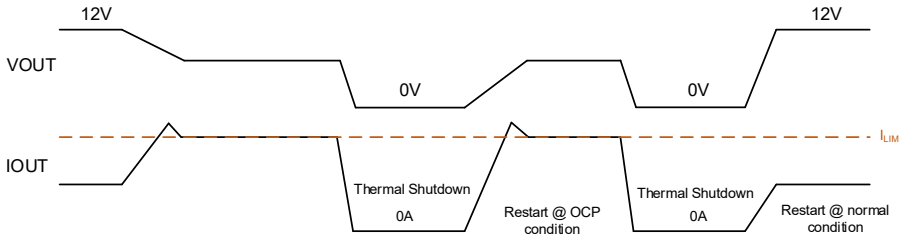


Figure 3. Current Limit Operation (AOZ18102-01 Auto-Restart)

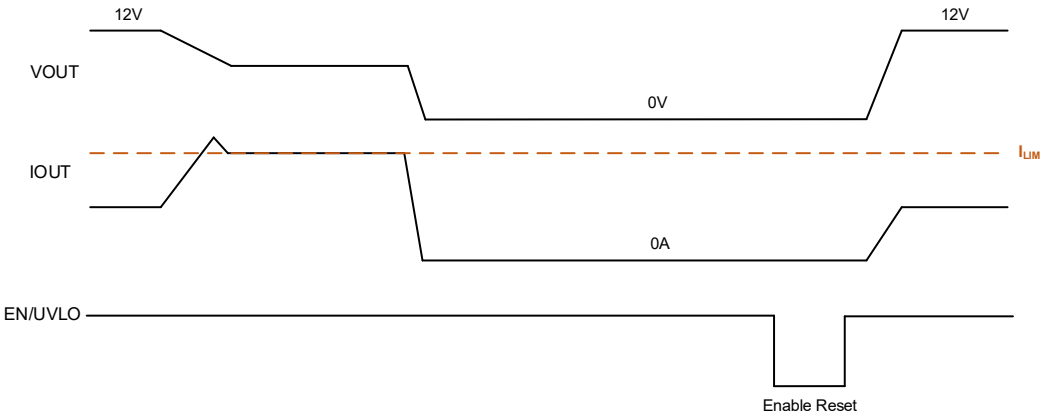


Figure 4. Current Limit Operation (AOZ18102-02 latch-Off)

Typical Characteristics

T_A = 25°C, VIN = 12V, EN = 5V, C_{IN} = 10µF, C_{OUT} = 10µF, C_{SS} = 1nF, R_{LIM} = 150kΩ unless otherwise specified.

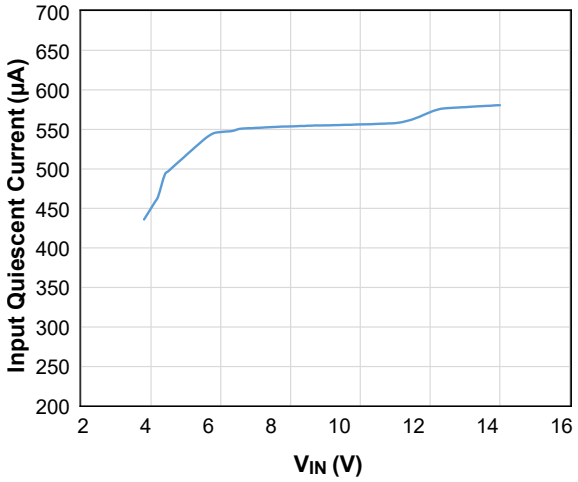


Figure 5. Input Quiescent Current vs VIN

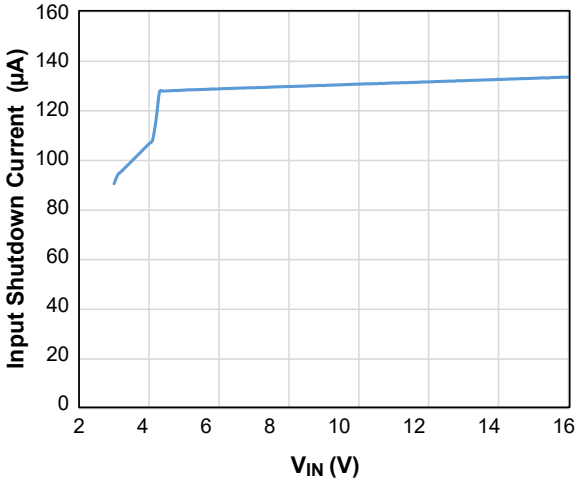


Figure 6. Input Shutdown Current vs VIN

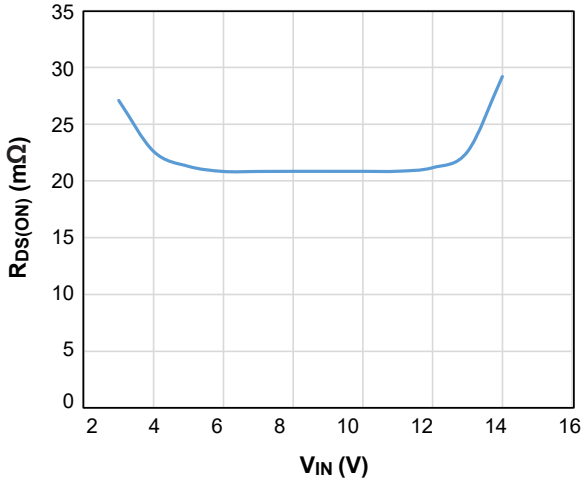


Figure 7. ON Resistance vs VIN

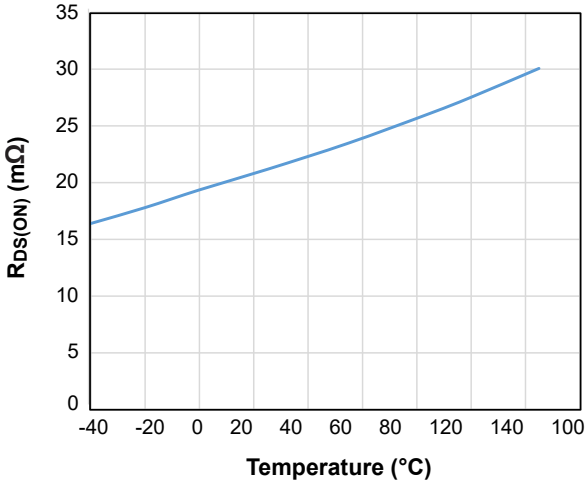


Figure 8. ON Resistance vs Temperature (VIN = 12V)

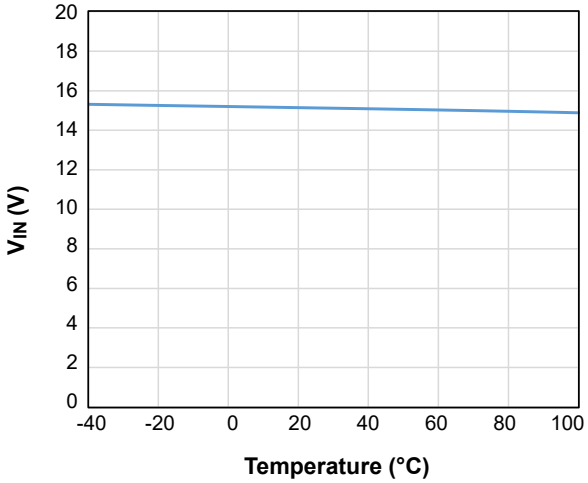


Figure 9. Input Over-Voltage Clamp vs Temperature

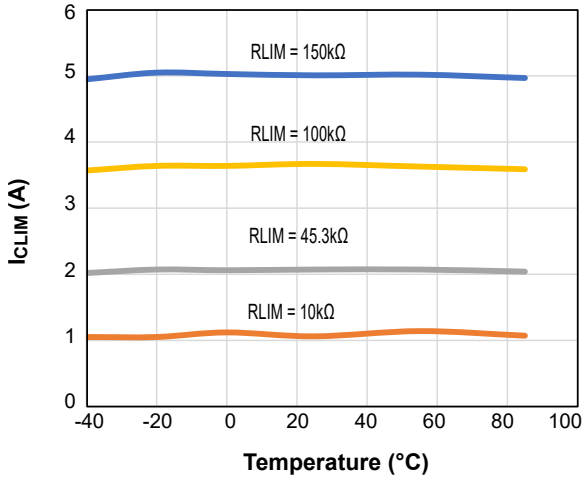
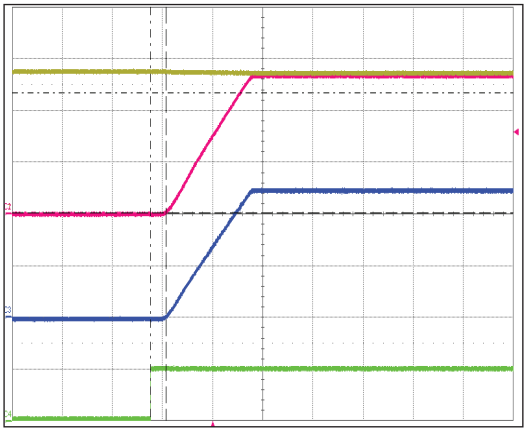


Figure 10. Current Limit vs Temperature

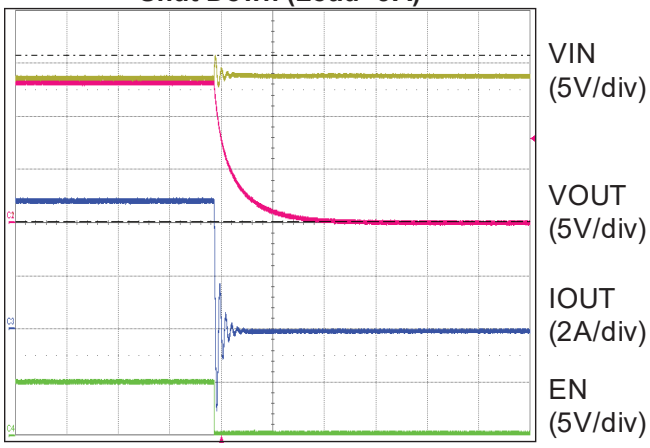
Typical Characteristics

T_A = 25°C, VIN = 12V, EN = 2.5V, C_{IN} = 10µF, C_{OUT} = 10µF, C_{SS} = 1nF, R_{LIM} = 150kΩ unless otherwise specified.

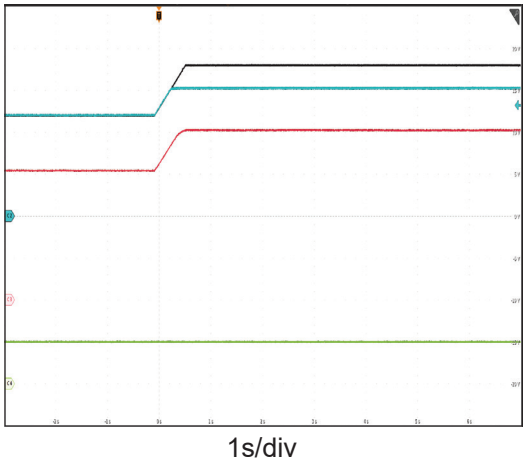
Start Up (Load = 5A)



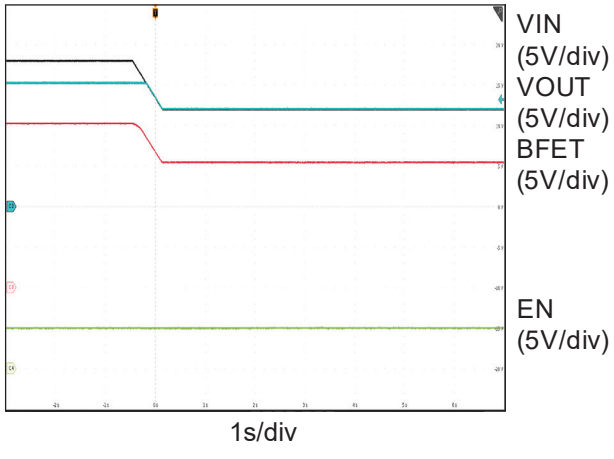
Shut Down (Load=5A)



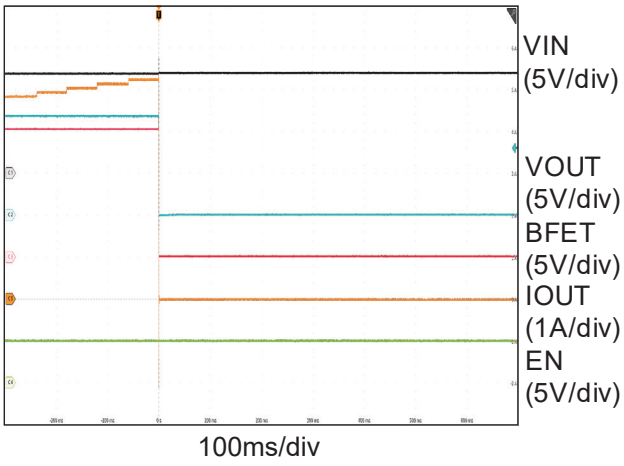
Over Voltage Clamp Entering



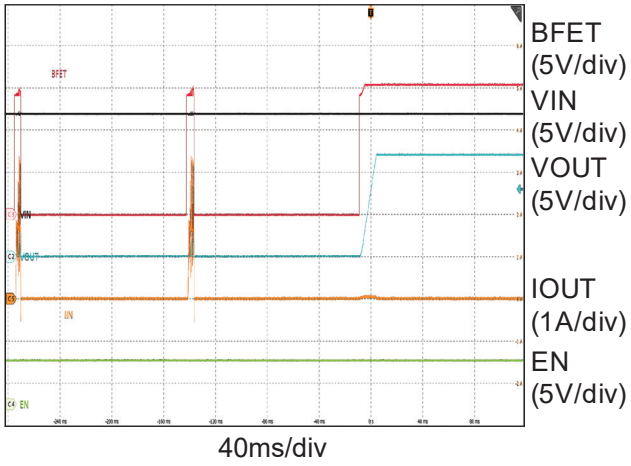
Over Voltage Clamp Leaving



Over Current Protection (AOZ18102DI-02)



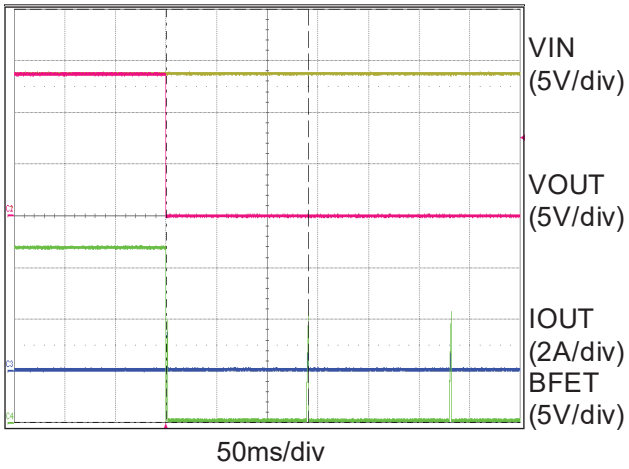
Over Current Protection Recovery (AOZ18102DI-01)



Typical Characteristics

T_A = 25°C, VIN = 12V, EN = 2.5V, C_{IN} = 10µF, C_{OUT} = 10µF, C_{SS} = 1nF, R_{LIM} = 150kΩ unless otherwise specified.

Output Short Protection (AOZ18102DI-01)



Detailed Description

The AOZ18102DI is a current limiting power switch with over-voltage, over-current, and thermal shutdown protections. The VIN and VOUT pins are rated 20V abs max.

Enable and Under-Voltage Lockout

The EN/UVLO pin is the ON/OFF control for the power switch. The device is enabled when the voltage at EN/UVLO pin is higher than V_{EN_H} and the input voltage is higher than the under-voltage lockout threshold, VIN > V_{UVLO_R}.

EN/UVLO pin can be biased with resistor divider network from VIN so that device enable will be tracking the input voltage. While disabled, the AOZ18102DI draws 130µA from supply. EN/UVLO cannot be left floating.

Input Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit monitors the input voltage. The power switch and the BFET for charging the gate of the external FET are only allowed to turn on when input voltage is higher than UVLO threshold (V_{UVLO_R}). Otherwise the switch is off.

Over-Voltage Clamp (OVC)

The voltage at VIN pin is constantly monitored once the device is enabled. In case input voltage exceeds the over-voltage clamp threshold (V_{OVC}), the output voltage will be clamped at the threshold voltage. The voltage clamping is not active when VIN voltage drops below the over voltage clamp threshold V_{OVC}.

Under the over-voltage clamp (OVC) condition, the output voltage is clamped to the V_{OVC} level. The power dissipation in the internal FETs under this condition is P_{FET_OVC} = (VIN – V_{OVC}) x I_{OUT}, which can heat up the device and causes thermal shutdown when the temperature reaches T_{SD}.

Programmable Current Limit and Over-Current Protection (OCP)

The AOZ18102DI implements current limit to ensure that the current through the switch does not exceed current limit threshold set by the external resistor RLIM.

The current limit threshold can be estimated using the equation below:

$$I_{LIM} = (0.7 + 3 \times 10^{-5} \times R_{LIM})$$

where R_{LIM} unit is in ohm and I_{LIM} unit is in Ampere

AOZ18102DI continuously limits the output current when output is overloaded. Under this condition, the part is dissipating excessive power due to higher voltage drop across VIN to VOUT. If over current continues to exist, it will reach thermal shutdown threshold and the switch will be turned off.

The AOZ18102DI integrates a fast comparator which will trigger to turn off the switch at 160% of the current limit threshold set by ILIM pin. After the fast comparator turns off the switch, the switch will be turned on to regulate the current to the set current limit threshold.

For AOZ18102DI-01 Auto-Restart version, the device restarts after the die temperature drops below T_{SD_HYS}.

For AOZ18102DI-02 Latch Off version, when the power switch turns off by TSD, the device enters latch off. The device restarts after toggling the EN/UVLO input logic to reset the device.

Programming Soft-start

The output soft-start time can be programmed externally through SS pin. The output soft-start time can be estimated using the equations below:

$$t_{ON} = \frac{(C_{SS} + 0.07) \times VIN}{1.067}$$

where C_{SS} unit is in nF and t_{ON} unit is in ms.

The SS pin can be left floating (C_{SS} = 0) for the minimum soft-start time.

The device has internal SOA management to protect the internal FETs. Design Tool is available to select the appropriate C_{SS} based on load and input voltage.

Blocking FET Driver (BFET)

When external blocking FET (N-Channel MOSFET) is used, connect this pin to the gate of the blocking FET. The BFET pin charges the gate of the external FET when both the voltage at EN/UVLO pin is higher than V_{EN_H} and the input voltage is higher than the under-voltage lockout threshold, VIN > V_{UVLO_R}. The BFET pin discharges current from the gate of the external FET via a 4kΩ internal discharge resistor, when either the voltage at EN/UVLO pin is lower than V_{EN_L} or the input voltage is lower than the under-voltage lockout threshold with hysteresis.

Thermal Shut Down Protection (TSD)

Thermal shutdown protects device from excessive temperature. The power switch is turned off when the die temperature reaches thermal shutdown threshold of 140°C.

For AOZ18102DI-01 Auto-Restart version, the device restarts after the die temperature drops below T_{SD_HYS}.

For AOZ18102DI-02 Latch Off version, when the power switch turns off by TSD, the device enters latch off. The device restarts after toggling the EN/UVLO input logic to reset the device.

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on to charge output capacitors and to limit input voltage drop. It also prevents high-frequency noise on the power line from passing through to the output. The input capacitor should be located as close to the pin as possible. A minimum of 10µF ceramic capacitor should be used. A higher capacitor value is strongly recommended to further reduce the transient voltage drop at the input.

In some applications, a Transient Voltage Suppressor (TVS) can be added on the input side to ensure that the input voltage transients don't exceed the Absolute Maximum Ratings of the device.

Output Capacitor Selection

The output capacitor acts in a similar way. Also, the output capacitor has to supply enough current for a large load that it may encounter during system transient. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

A Schottky diode can be added between the output and ground to absorb negative voltage spikes.

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$\text{Power Dissipated} = R_{ON} \times (I_{OUT})^2$$

Layout Guidelines

Good PCB layout is important for improving the thermal and overall performance of AOZ18102DI. To optimize the switch response time to output short-circuit conditions, keep all traces as short as possible to reduce the effect of unwanted parasitic inductance. Place the input and output bypass capacitors as close as possible to the VIN and VOUT pins. The input and output PCB traces should be as wide as possible. The input and output traces should be sized to carry at least twice the full-load current.

Place a decoupling capacitor as close as possible to the IN and GND terminals of the device. Minimize the loop area formed by the bypass-capacitor connection, the VIN pins, and the GND pin (EXP) of the IC.

If protective devices such as TVS and Schottky diode are needed, place them physically close to the IC, and route with short traces to reduce inductance.

For the most efficient thermal dissipation, connect the exposed pad to the ground plane with thermal vias as many as possible. Figure 11 shows example for the AOZ18102DI layout.

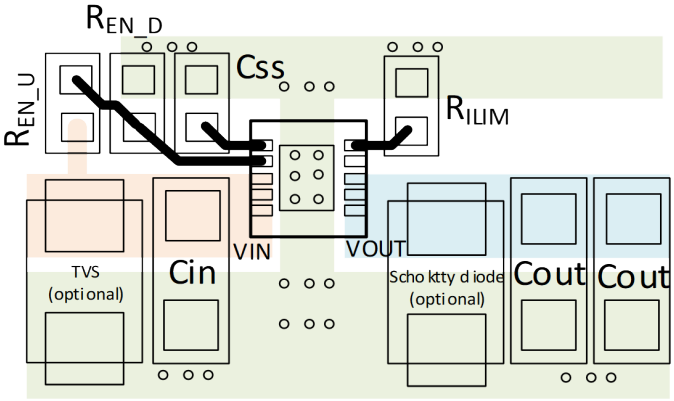
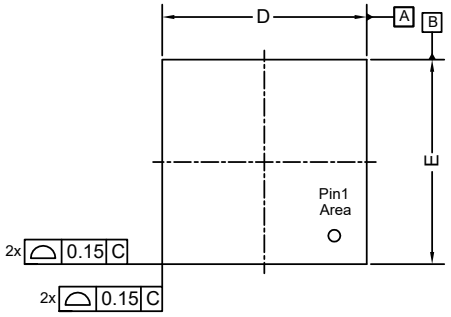
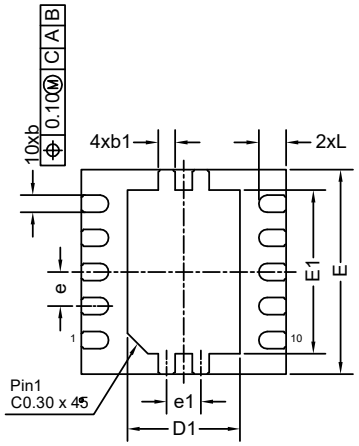


Figure 11. PCB Layout Example

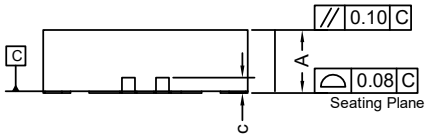
Package Dimensions, DFN3x3-10L



TOP VIEW

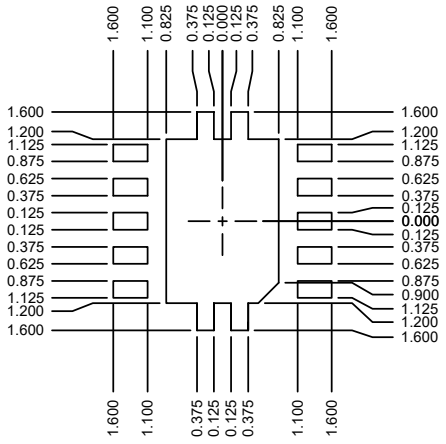


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



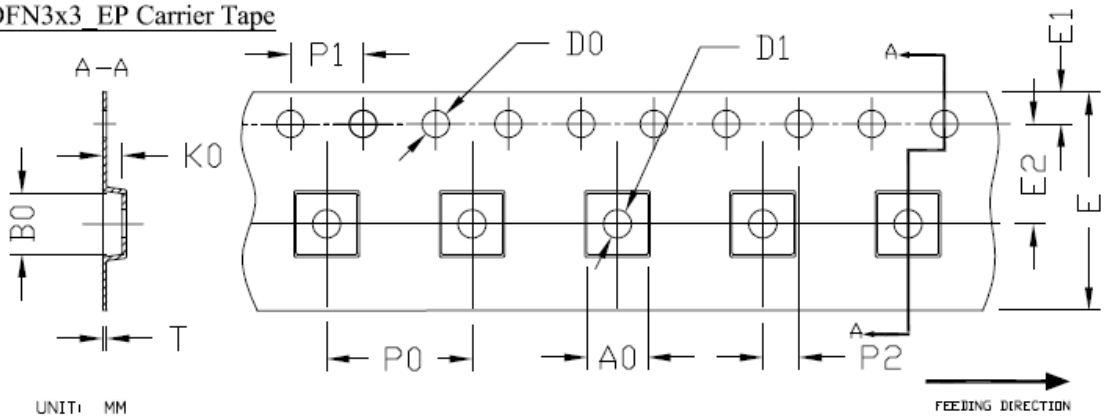
UNIT: mm

SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.800	0.900	1.000	0.031	0.035	0.039
A1	0.000	---	0.050	0.000	---	0.002
D	2.900	3.000	3.100	0.114	0.118	0.122
D1	1.550	1.650	1.750	0.061	0.065	0.069
E	2.900	3.000	3.100	0.114	0.118	0.122
E1	2.300	2.400	2.500	0.091	0.094	0.098
L	0.300	0.400	0.500	0.012	0.016	0.020
b	0.180	0.250	0.300	0.007	0.010	0.012
b1	0.250 REF			0.010 REF		
c	0.200 REF			0.008 REF		
e	0.500 BSC			0.020 BSC		
e1	0.500 REF			0.020 REF		

NOTE:
1. DIMENSIONING AND TOLERANCING COMPLY WITH ASME Y14.5M 1994.
2. CONTROLLED DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD(S) AND ALL TERMINAL LEADS HAVING METALIZATION.

Tape and Reel Dimensions, DFN3x3-10L

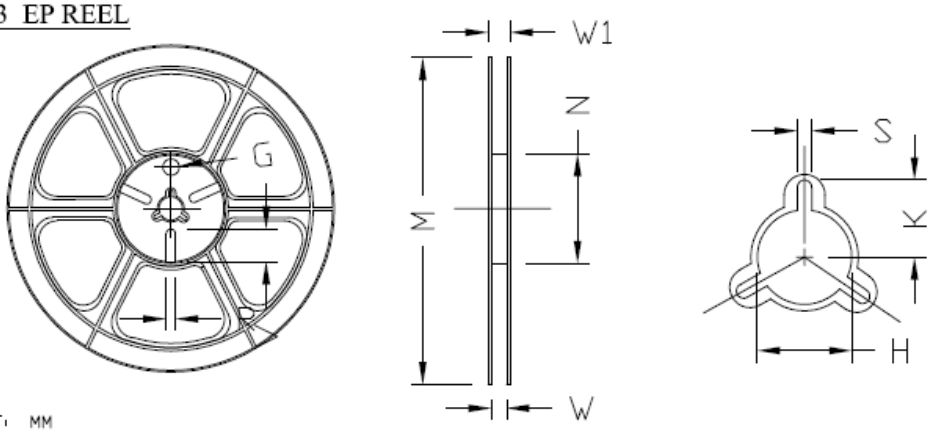
DFN3x3_EP Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3x3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 −0	1.50 +0.10 −0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

DFN3x3_EP REEL

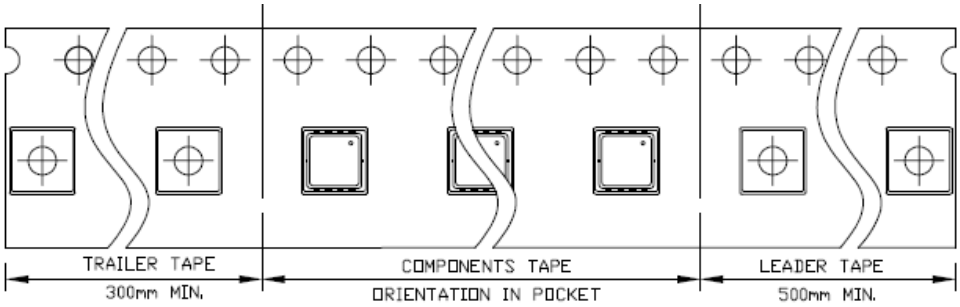


UNIT: MM

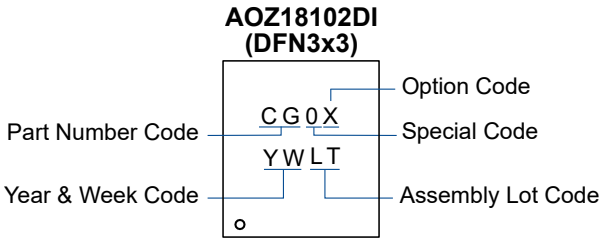
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

PIC

Unit Per Reel: 5000pcs



Part Marking



Part Number	Description	Marking Code
AOZ18102DI-01	Auto-Restart	CG01
AOZ18102DI-02	Latch Off	CG02

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.