AOZ2262NQI-12

28V/10A Synchronous EZBuck™ Regulator

General Description

The AOZ2262NQI-12 is a high-efficiency, easy-to-use DC/DC synchronous buck regulator that operates up to 28V. The device is capable of supplying 10A of continuous output current with an output voltage adjustable down to 0.6V ±1%.

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range. The on time can be externally programmed up to 2.6µs.

The device features multiple protection functions such as V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2262NQI-12 is available in a 4mm×4mm QFN-23L package and is rated over a -40°C to +85°C ambient temperature range.

Features

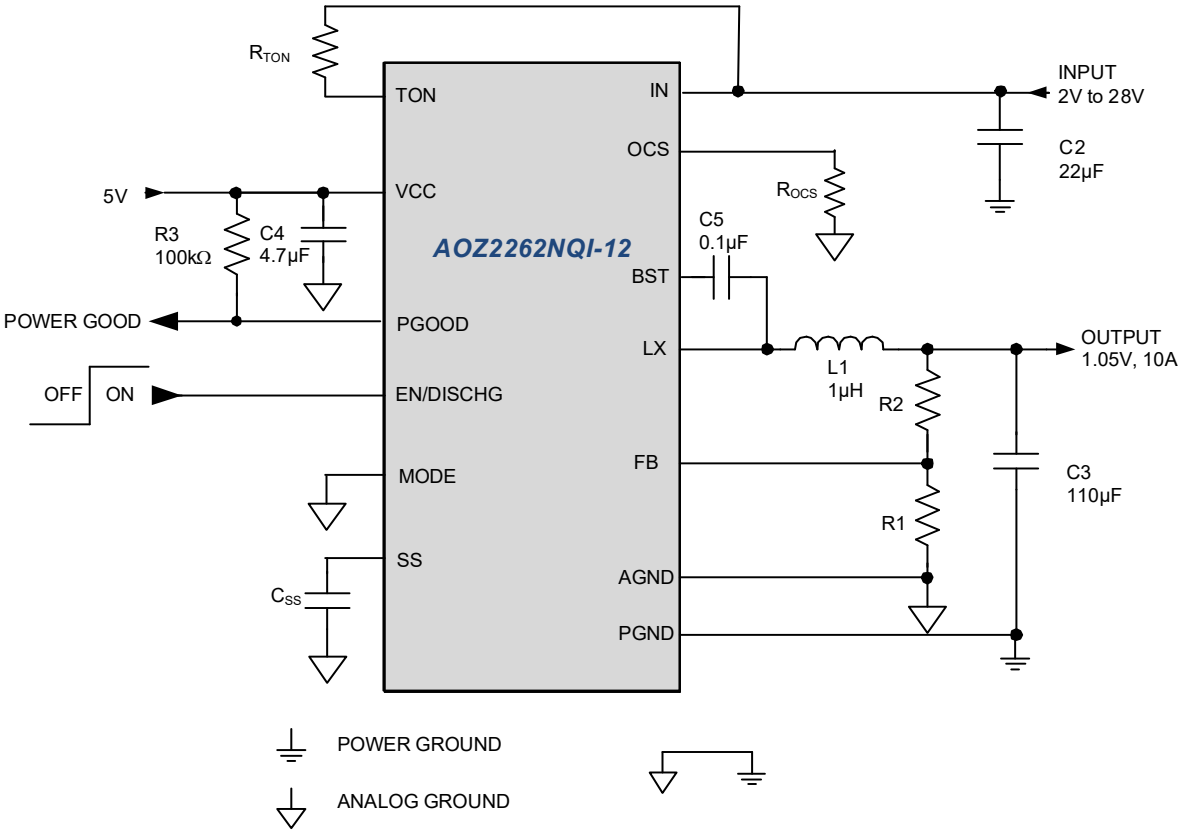
- Wide input voltage range
  - 2V to 28V
- 10A continuous output current
- Output voltage adjustable down to 0.6V (±1.0%)
- Low $R_{DS(ON)}$ internal NFETs
  - 13mΩ high-side
  - 10mΩ low-side
- Constant On-Time with input feed-forward
- Programmable on-time up to 2.6µs
- Selectable PFM light-load operation
- Ceramic capacitor stable
- Adjustable soft start
- Ripple reduction
- Discharge Function
- Power Good output
- Integrated bootstrap diode
- Adjustable cycle-by-cycle current limit
- Short-circuit protection
- Over-voltage protection
- Thermal shutdown
- Thermally enhanced 4mm x 4mm QFN-23L package

Applications

- Portable computers
- Compact desktop PCs
- Servers
- Graphics cards
- Set-top boxes
- LCD TVs
- Cable modems
- Point-of-load DC/DC converters
- Telecom/Networking/Datacom equipment

GREEN Product

Typical Application

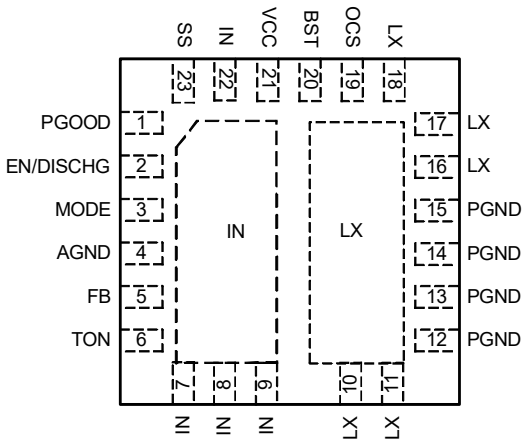


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ2262NQI-12	-40°C to +85°C	23-Pin 4mm x 4mm QFN	Green Product

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



23-Pin 4mm x 4mm QFN
Top View

Pin Description

Pin Number	Pin Name	Pin Function
1	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage or 50% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.
2	EN/DISCHG	Enable Input. The AOZ2262NQI-12 is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after IN and VCC are well supplied. Power-off the device by EN off is suggested. Set voltage level higher/lower than discharge threshold when PGOOD pull high to enable/disable output discharge function.
3	MODE	PFM Selection Input. Connect MODE pin to VCC for forced PWM operation. Connect MODE pin to ground for PFM operation to improve light load efficiency.
4	AGND	Analog Ground.
5	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
6	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on time.
7, 8, 9, 22	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
12, 13, 14, 15	PGND	Power Ground.
10, 11, 16, 17, 18	LX	Switching Node.
19	OCS	Current limitation level setting pin. Connect a resistor between OCS and GND to set over current protection level. No capacitor is allowed between OCS and AGND.
20	BST	Bootstrap Capacitor Connection. The AOZ2262NQI-12 includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in the Typical Application diagram.
21	VCC	Supply Input for analog functions. Bypass VCC to AGND with a 4.7µF~10µF ceramic capacitor. Place the capacitor close to VCC pin.
23	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
IN, TON to AGND	-0.3V to 30V
LX to AGND(1)	-1.0V to 30V
BST to AGND	-0.3V to 36V
SS, OCS, PGOOD, FB to AGND	-0.3V to 6V
EN/DISCH, VCC, MODE to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating(2)	2kV

Notes:

1. LX to PGND Transient (t<20ns) ------ -7V to V_{IN} + 7V.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	2V to 28V
Output Voltage Range	0.6V to 0.85*V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance (θ_{JA})	32°C/W

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

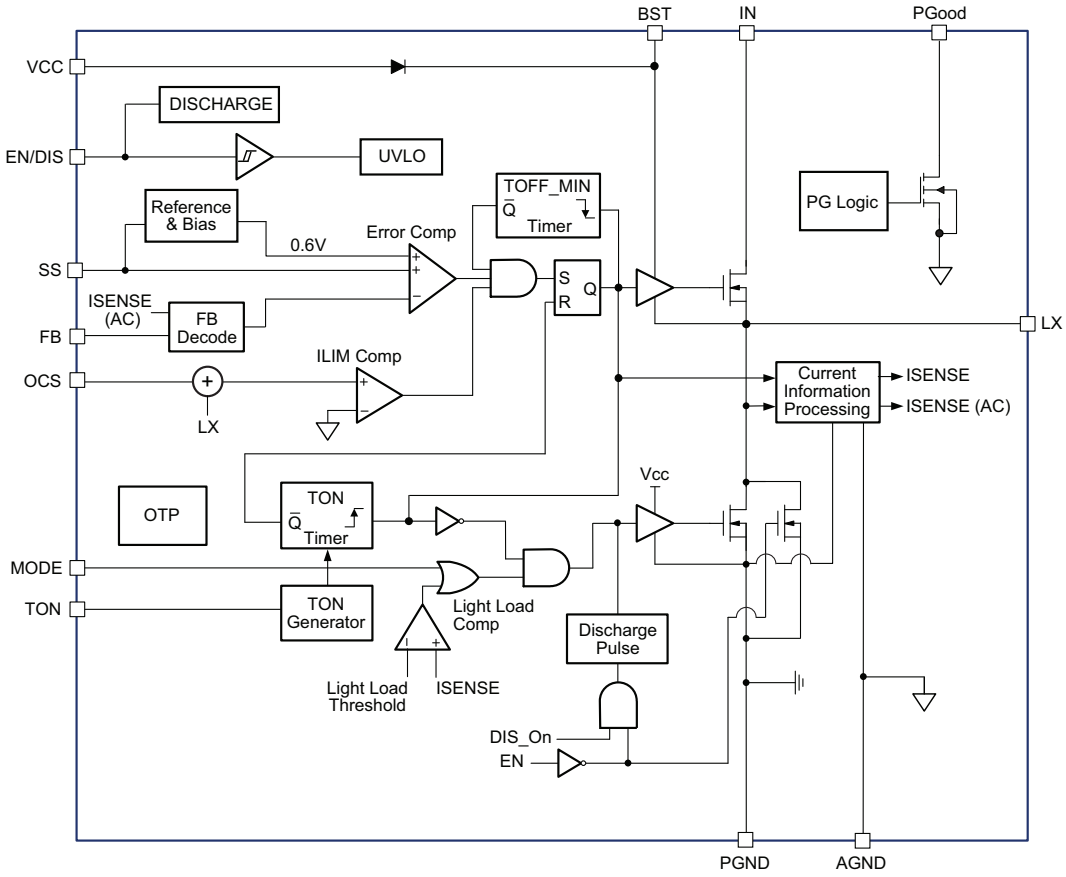
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	IN Supply Voltage		**2**		**28**	V
V_{UVLO}	Under-Voltage Lockout Threshold of V_{CC}	VCC rising VCC falling	 **3.2**	**4.2** **3.9**	**4.5**	V V
I_q	Quiescent Supply Current of V_{CC}	I_{OUT} = 0A, V_{EN} > 2V, PFM mode		**350**		µA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**1**	**20**	µA
V_{FB}	Feedback Voltage	T_A = 25°C	0.594	0.600	0.606	V
	Load Regulation			0.5		%
	Line Regulation			1		%
I_{FB}	FB Input Bias Current				200	nA
Enable/Discharge						
V_{EN}	EN Input Threshold	Off threshold On threshold	 1.2		0.5	V V
V_{EN_HYS}	EN Input Hysteresis		100	250		mV
V_{DIS}	Discharge Threshold	When PGOOD from 0 to 1		1.5		V
MODE Control						
V_{MODE}	MODE Input Threshold	PFM Mode threshold Force PWM threshold	 1.2		0.5	V V
$V_{MODEHYS}$	MODE Input Hysteresis			100		mV
Modulator						
T_{ON}	On Time	R_{TON} = 100kΩ, V_{IN} = 12V		200		ns
T_{ON_MIN}	Minimum On Time			100		ns
T_{ON_MAX}	Maximum On Time			2.6		µs
T_{OFF_MIN}	Minimum Off Time			300		ns

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Soft-Start						
I_{SS_OUT}	SS Source Current	V_{SS} = 0V C_{SS} = 0.001µF to 0.1µF	7	11	15	µA
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			**0.5**	V
	PGOOD Leakage Current				**±1**	µA
V_{PGH}	PGOOD Threshold (Low Level to High Level)	FB rising		90		%
V_{PGL}	PGOOD Threshold (High Level to Low Level)	FB rising FB falling		150 85		% %
	PGOOD Threshold Hysteresis			5		%
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	FB falling		50		%
T_{PL}	Under Voltage Delay Time			32		µs
V_{PH}	Over Voltage Threshold	FB rising		150		%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	V_{IN} = 12V, V_{CC} = 5V		13		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 12V, V_{CC} = 5V		10		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Thermal Protection						
	Thermal Shutdown Threshold	T_J rising T_J falling		150 100		°C °C

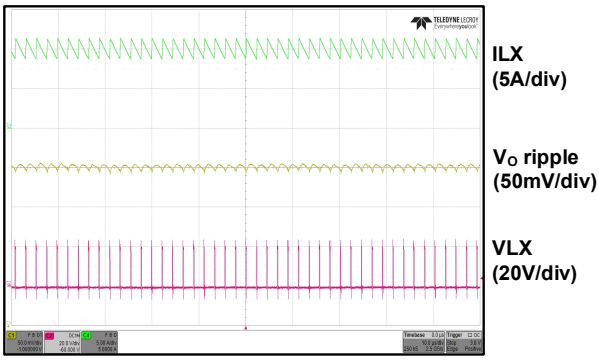
Functional Block Diagram



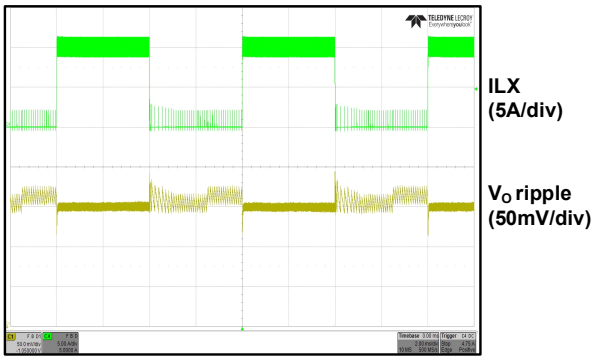
Typical Performance Characteristics

T_A = 25°C, V_{IN} = 19V, V_{OUT} = 1V, f_S = 450kHz, unless otherwise specified.

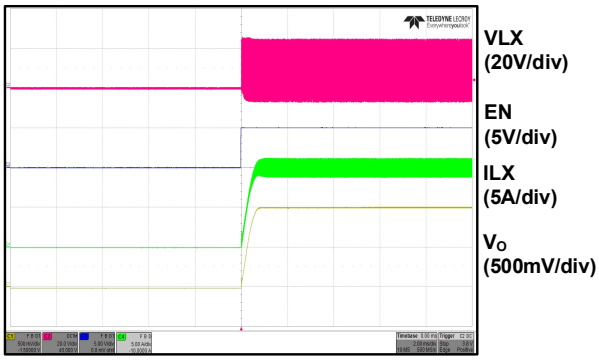
Normal Operation



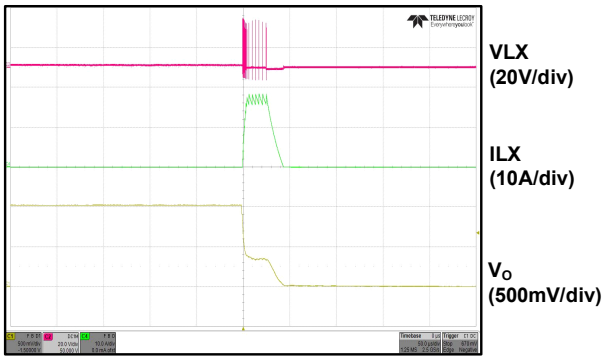
Load Transient 0A to 10A



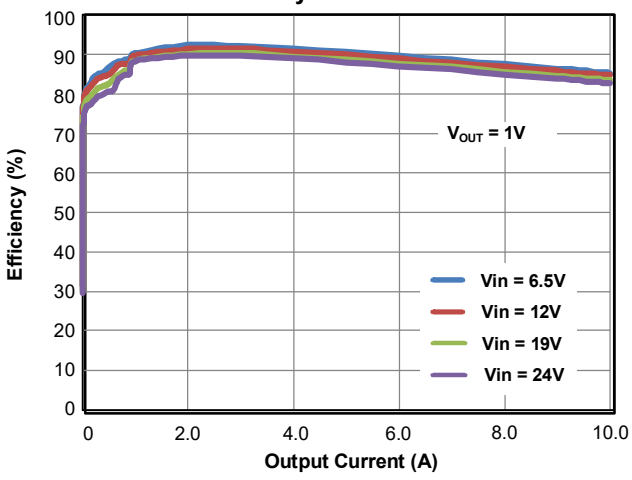
Full Load Start-up



Short Circuit Protection



Efficiency vs. Load Current



Detailed Description

The AOZ2262NQI-12 is a high-efficiency, easy-to-use, synchronous buck regulator optimized for notebook computers. The regulator is capable of supplying 10A of continuous output current with an output voltage adjustable down to 0.6V. The programmable on-time from 100ns to 2.6µs enables optimizing the configuration for PCB area and efficiency.

The input voltage of AOZ2262NQI-12 can be as low as 2V. The highest input voltage of AOZ2262NQI-12 can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with ceramics output capacitor. The switching frequency can be externally programmed. Protection features include V_{CC} under-voltage lockout, current limit, output over voltage and under voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2262NQI-12 is available in 23-pin 4mm×4mm QFN package.

Enable and Soft Start

The AOZ2262NQI-12 has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft start process begins when V_{CC} rises to 4.5V and voltage on EN pin is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of soft-start pin (V_{SS}) when it is lower than 0.6V. When V_{SS} is higher than 0.6V, the FB voltage is regulated by internal precise band-gap voltage (0.6V). When V_{SS} is higher than 1.2V, the PGOOD signal is high. The soft-start time for PGOOD can be calculated by the following formula:

$T_{SS}(\mu s) = 120 \times C_{SS}(nF)$

If C_{SS} is 1nF, the soft-start time will be 120µs; if C_{SS} is 3.6nF, the soft-start time will be 432µs.

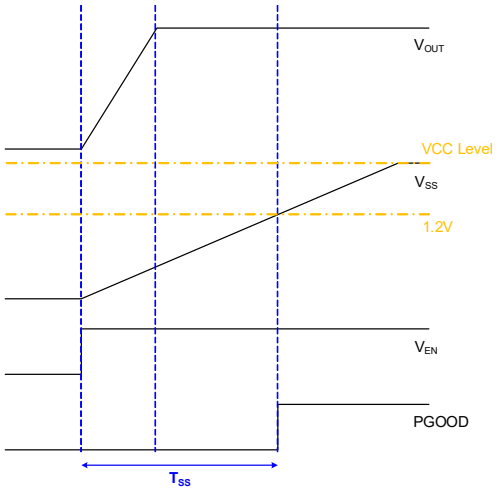


Figure 1. Soft-Start Sequence of AOZ2262NQI-12

Enable and Discharge Function

AOZ2262NQI-12 pin 2 is a multi-function pin, which combines enable and discharge function together. Discharge function on/off is determined by the voltage level on this pin at PGOOD rising edge. Figure 2 illustrates how to activate discharge function. Once PGOOD signal rises up, AOZ2262NQI-12 detects the voltage on EN/DIS pin. Discharge function will be activated (Dis_on set to 1) only if EN/DIS pin voltage is under discharge threshold at that moment. Dis_on keeps high until next PGOOD rising edge and will be overwritten. Discharge function won't be activated (Dis_on set to 0) if EN/DIS pin voltage is over discharge threshold at PGOOD rising edge. Dis_on keeps low until next PGOOD rising edge and will be overwritten.

AOZ2262NQI-12 enters discharge mode if Dis_on signal is high when EN/DIS pin voltage is lower than EN off threshold. Discharge MOSFET is always turn-on during discharge mode. At the mean while, low-side MOSFET turns on and off to quickly discharge output voltage. All protection and COT are disabled during discharge mode. Discharge mode operation ended when FB voltage is under 40mV.

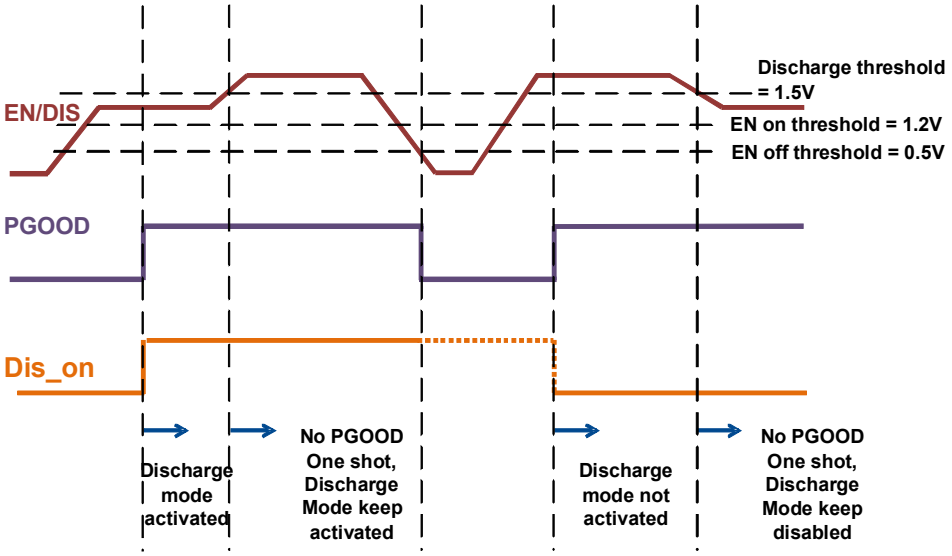


Figure 2. AOZ2262NQI-12 Discharge Function On/Off Setting

Constant-On-Time PWM Control with Input Feed Forward

The control algorithm of AOZ2262NQI-12 is constant-on-time PWM Control with input feed-forward.

The simplified control schematic is shown in Figure. 3. The high-side switch on-time is determined solely by a one-shot whose pulse width can be programmed by one external resistor and is inversely proportional to input voltage (IN). The one-shot is triggered when the internal 0.6V is higher than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed lower-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on time control schemes.

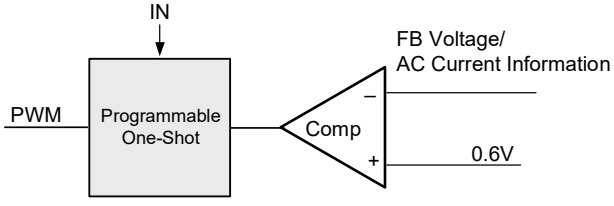


Figure 3. Simplified Control Schematic of AOZ2262NQI-12

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward.

The internal circuit of AOZ2261NQI-12 sets the on-time of high-side switch inversely proportional to the IN.

$$T_{ON} \propto \frac{R_{TON}(k\Omega)}{V_{IN}(V)} \quad (1)$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (2)$$

Once the product of V_{IN} x T_{ON} is constant, the switching frequency keeps constant and is independent with input voltage.

An external resistor between the IN and TON pin sets the switching on-time according to the following equation:

$$T_{ON}(ns) = \frac{R_{TON}(k\Omega)}{V_{IN}(V)} \times 25 \quad (3)$$

Then, the switching frequency can be estimated by:

$$F_{SW}(kHz) = \frac{V_{OUT}}{V_{IN} * T_{ON}(ns)} \times 10^6 = \frac{V_{OUT}}{R_{TON}(k\Omega)} \times 4 \times 10^4 \quad (4)$$

If V_{OUT} is 1.05V, V_{IN} is 19V, and set F_S = 500kHz. According to equation 3, T_{ON} = 110ns is needed. Finally, use the T_{ON} to R_{TON} curve, we can find out R_{TON} is 84kΩ.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually can not be used as output capacitor.

The AOZ2262NQI-11 senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applied. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Current-Limit Protection

The AOZ2262NQI-11 has the current-limit protection by using $R_{DS(ON)}$ of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off (300ns typical) is implemented after a constant on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

Current-Limit Setting

The current-limit threshold mentioned in last paragraph can be set by connecting a resistor between OCS pin and ground. The value of the current limit resistor (R_{OCS}) can be calculated according to the equation below. And the value of R_{OCS} is need higher than 16kΩ. A capacitor from OCS pin to ground would impact the current limit accuracy and is not allowed.

$$I_{L\_LIMIT}(A) = 0.808*R_{OCS}(k\Omega) - 1.616 \quad (5)$$

As shown in Figure 4, once the magnitude of switch node voltage V_{LX} is larger than V_{OCS}, over current signal is triggered. The larger R_{OCS} is, the higher over current threshold will be. Section Current-Limit Protection describes the action when over current condition happens.

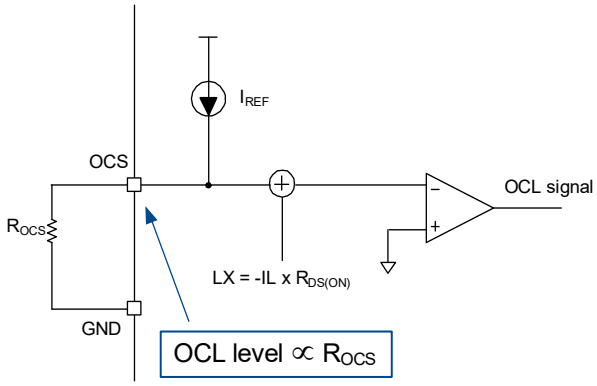


Figure 4. Illustration of Current Limit Setting

Output Voltage Under-Voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, AOZ2262NQI-12 will wait for 32µs (typical) and turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ2262NQI-12 again.

Output Voltage Over-Voltage Protection

The threshold of OVP is set 50% higher than 0.6V. When the V_{FB} voltage exceeds the OVP threshold, high-side MOSFET is turn-off and low-side MOSFETs is turn-on 1µs, then latch-off.

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 15% below the nominal regulation voltage, the PGOOD is pulled low. When the output voltage is 50% higher than the nominal regulation voltage, the PGOOD is also pull low.

When combined with the under-voltage-protection circuit, this current limit method is effective in almost every circumstance.

Ripple Reduction

When switching frequency is down to half of setting during PFM, AOZ2262NQI-12 actively reduces on-time pulse width to reduce inductor current ripple and output voltage ripple. Ripple reduction not only reduces half of voltage ripple but also decreases the chance of acoustic noise under light load.

Application Information

The basic AOZ2262NQI-12 application circuit is shown in page 2. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ2262NQI-12 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7µF, should be connected to the V_{CC} pin and AGND pin for stable operation of the AOZ2262NQI-12. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}} \quad (6)$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

if let *m* equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m \quad (8)$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 5. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

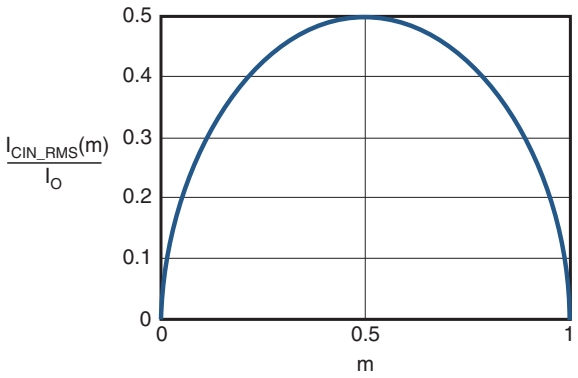


Figure 5. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN\text{-}RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value, and ESR. It can be calculated by the equation below;

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR_{C_o} + \frac{1}{8 \times f \times C_o} \right) \quad (11)$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When a low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times f \times C_o} \quad (12)$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{C_o} \quad (13)$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current.
It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \quad (14)$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, the output capacitor could be overstressed.

Power MOSFET SOA Curve

AOZ2262NQI-12 integrates AOS' state of the art Trench MOSFETs. Robust SOA ensures reliable operation in high performance buck regulator applications.

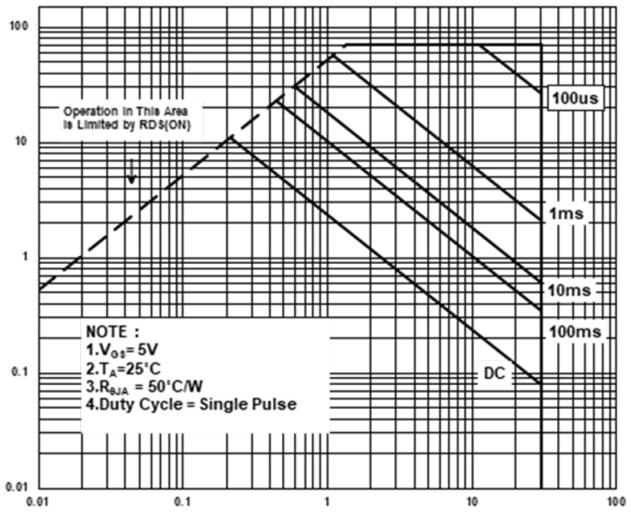


Figure 6. High-side MOSFET SOA Curve

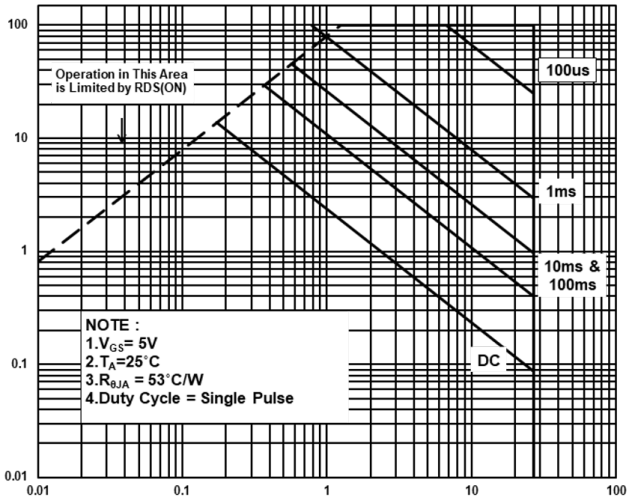


Figure 7. Low-side MOSFET SOA Curve

Power Good Resistor

The selection of the power good resistor involves a trade-off among the following considerations:

1. Hard-switching noise

When the PG high conditions are satisfied, the MOSFET will be turned off, allowing the PG signal to be pulled high. The voltage/current level on the PG MOSFET changes suddenly in a short time, causing switching noise to be generated on the ground of the PG MOSFET, which can influence the Vgs of the PG MOSFET and cause PG glitch problems. To prevent this issue, the PG resistor should not be selected too low. In general condition, a lowest 100kΩ resistance is recommended to reduce the switching noise to be ignorable.

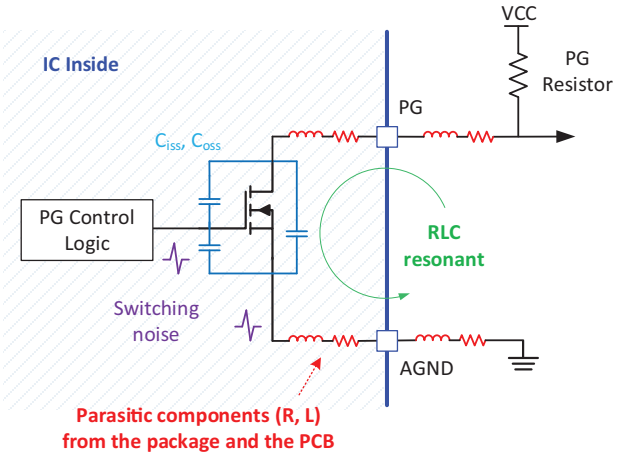


Figure 8. Switching Noise of PG MOSFET

2. Voltage threshold of post device

In most applications, the PG is used to enable post devices. The PG high voltage must be higher than the enable threshold of the post device, and the PG low voltage must be lower than the disable threshold of the post device. The off resistance of the PG MOSFET is guaranteed to be higher than 5MΩ.

3. Driving capability of post devices

The higher PG resistor, the lower driving current from PG to post device. In order to ensure the post device can be properly driven, it is recommended users check the input impedance of post device and include it in the PG resistor calculation.

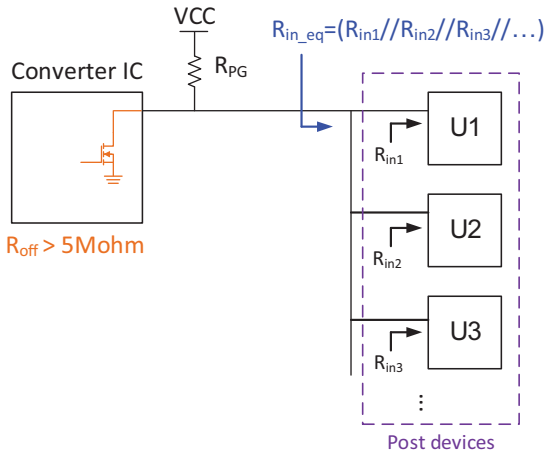


Figure 9. Input Impedances of Post Devices for Power Good

Considering the above factors, AOS recommends a lowest PG resistor value of 100kΩ. This value can be used for the vast majority of application designs; however, users may adjust it based on the aforementioned considerations and specific application requirements. A PG resistor calculation formula is shown as below:

$$100k\Omega < R_{PG} < \frac{V_{CC} - V_{th\_H}}{V_{th\_H}} \times (5M\Omega \,//\, R_{in\_eq}) \quad (15)$$

Where the V_{th_H} is the highest enable threshold of post devices.

Thermal Management and Layout Consideration

In the AOZ2262NQI-12 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ2262NQI-12.

In the AOZ2262NQI-12 buck regulator circuit, the major power dissipating components are the AOZ2262NQI-12 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} \quad (16)$$

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{inductor\_loss} = I_{OUT}^2 \times R_{inductor} \times 1.1 \quad (17)$$

The actual junction temperature can be calculated with power dissipation in the AOZ2262NQI-12 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{total\_loss}) \times \theta_{JA} + T_A \quad (18)$$

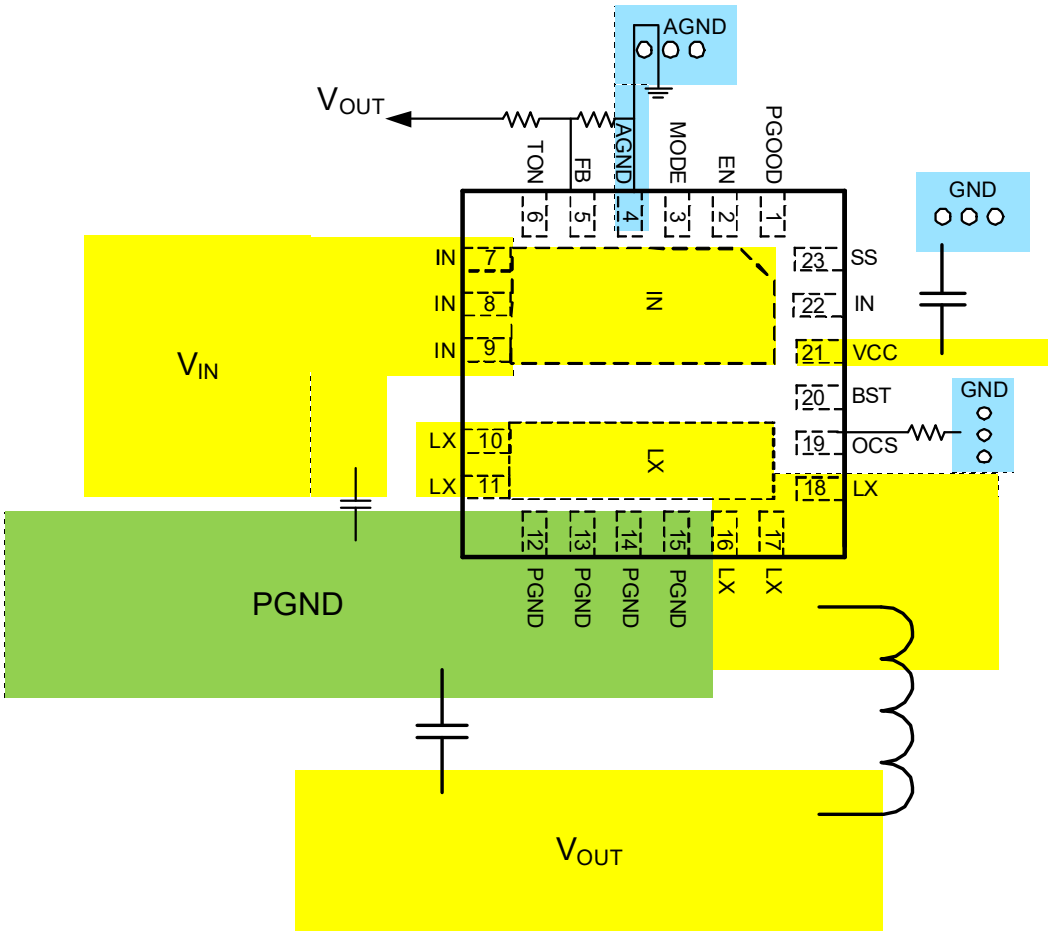
The maximum junction temperature of AOZ2262NQI-12 is 150ºC, which limits the maximum load current capability.

The thermal performance of the AOZ2262NQI-12 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

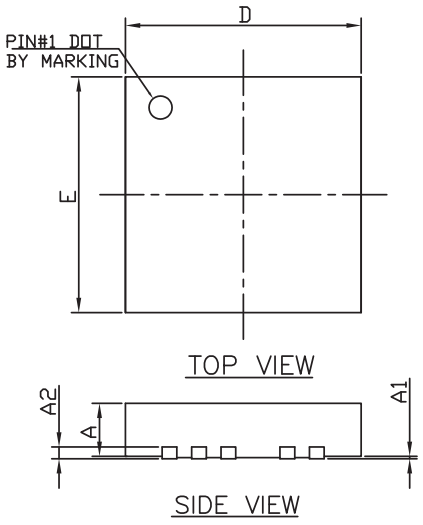
Layout Considerations

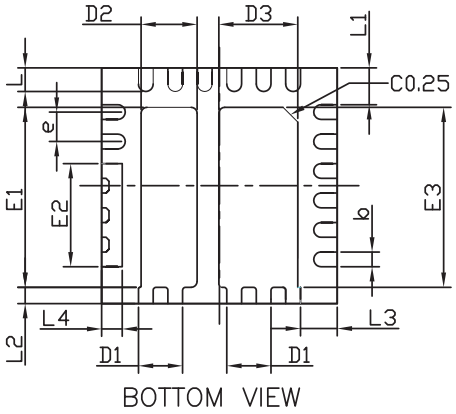
Several layout tips are listed below for the best electric and thermal performance.

1. The LX pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connect a large copper plane to LX pin to help thermal dissipation.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connect a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor C_{VCC} should be connected to VCC and AGND as close as possible.
5. Voltage divider R1 and R2 should be placed as close as possible to FB and AGND.
6. R_{TON} should be connected as close as possible to Pin 6 (TON pin).
7. A ground plane is preferred.
8. Keep sensitive signal traces such as feedback trace far away from the LX pins.
9. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
10. The current limit resistor (R_{OCS}) should be connected as close as possible to Pin 19 (OCS). Place three GND vias to connect to inner ground layer. Keep distance between Rocs and Lx plane.



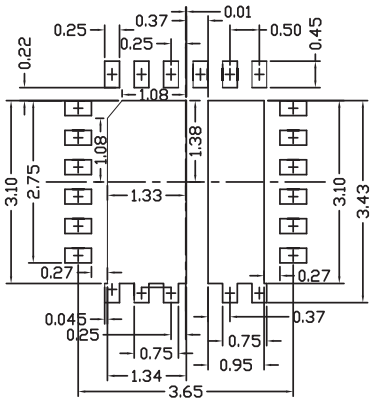
Package Dimensions, QFN4x4B-23L



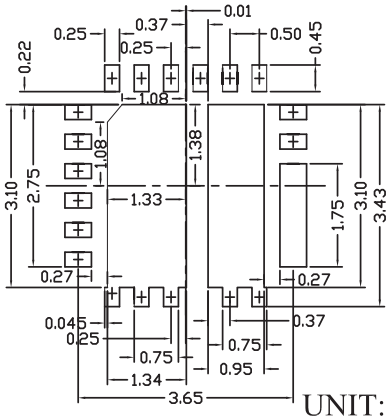


RECOMMENDED LAND PATTERN

Option 1



Option 2



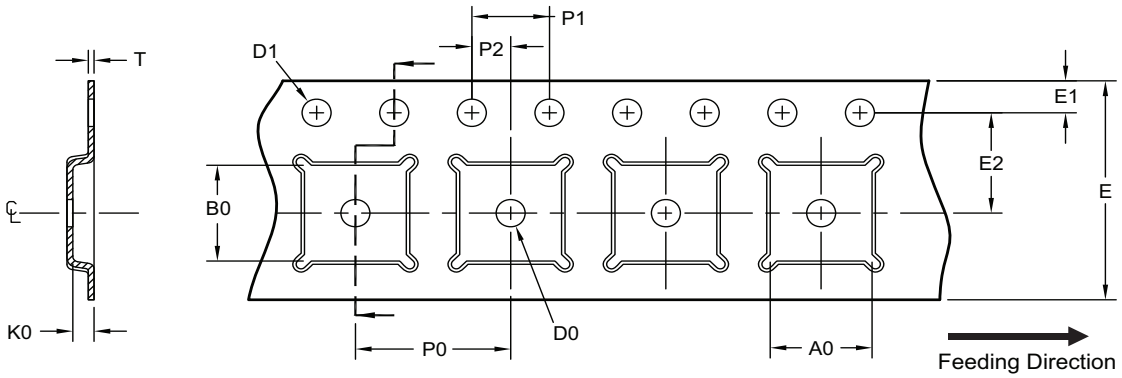
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	—	0.05	0.000	—	0.002
A2		0.2 REF			0.008 REF	
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.65	1.75	1.85	0.065	0.069	0.073
E3	2.95	3.05	3.15	0.116	0.120	0.124
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.034
D2	0.85	0.95	1.05	0.033	0.037	0.041
D3	1.24	1.34	1.44	0.049	0.053	0.057
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
L3	0.57	0.62	0.67	0.022	0.024	0.026
L4	0.30	0.35	0.40	0.012	0.014	0.016
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020 BSC	

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: ±0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

Tape and Reel Dimensions, QFN4x4B-23L

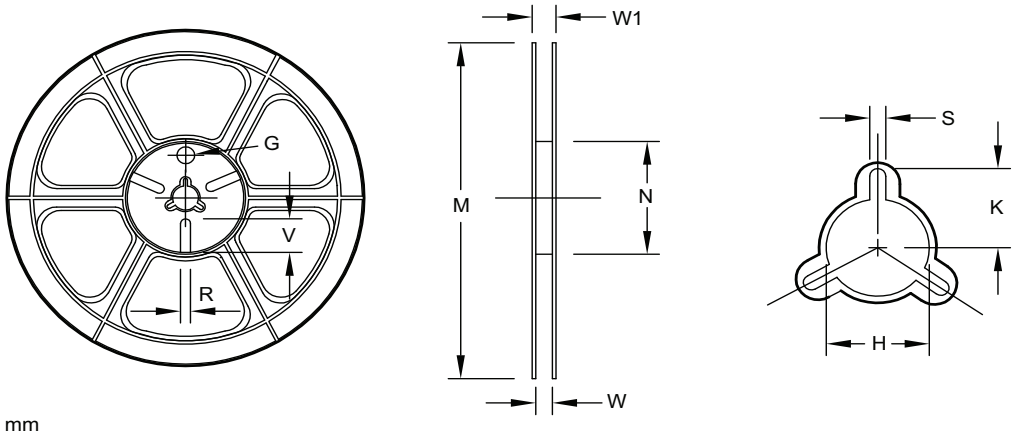
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN 4x4 (12mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.10/-0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

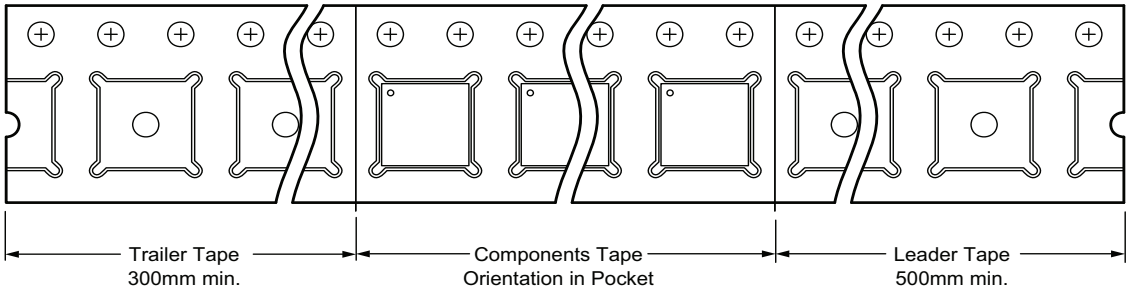
Reel



UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0.0	17.0 +2.6/-1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation



Part Marking