AOZ22701QI

I^2C Controllable 28 V/4 A Synchronous EZBuck™ Regulator

General Description

The AOZ22701QI is an I^2C controllable, high efficiency, easy-to-use DC-DC synchronous buck regulator capable of operation from a 6.5 V to 28 V input bus. Ability to control the output voltage using the I^2C bus simplifies converter design for microprocessors or SoCs that require dynamic voltage scaling or voltage margining. The device is capable of supplying 4 A of continuous output current with an output voltage adjustable from 0.7 V to 1.15927 V (±1.0%).

The AOZ22701QI integrates an internal linear regulator to generate 5.3 V V_{CC} from input. If input voltage is lower than 5.3 V, the linear regulator operates at low drop output mode, which allows the V_{CC} voltage is equal to input voltage minus the drop-output voltage of the internal linear regulator.

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range.

The devices feature multiple protection functions such as V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ22701QI is available in a 4 mm×4 mm QFN-22L package and is rated over a -40°C to +85°C ambient temperature range.

Features

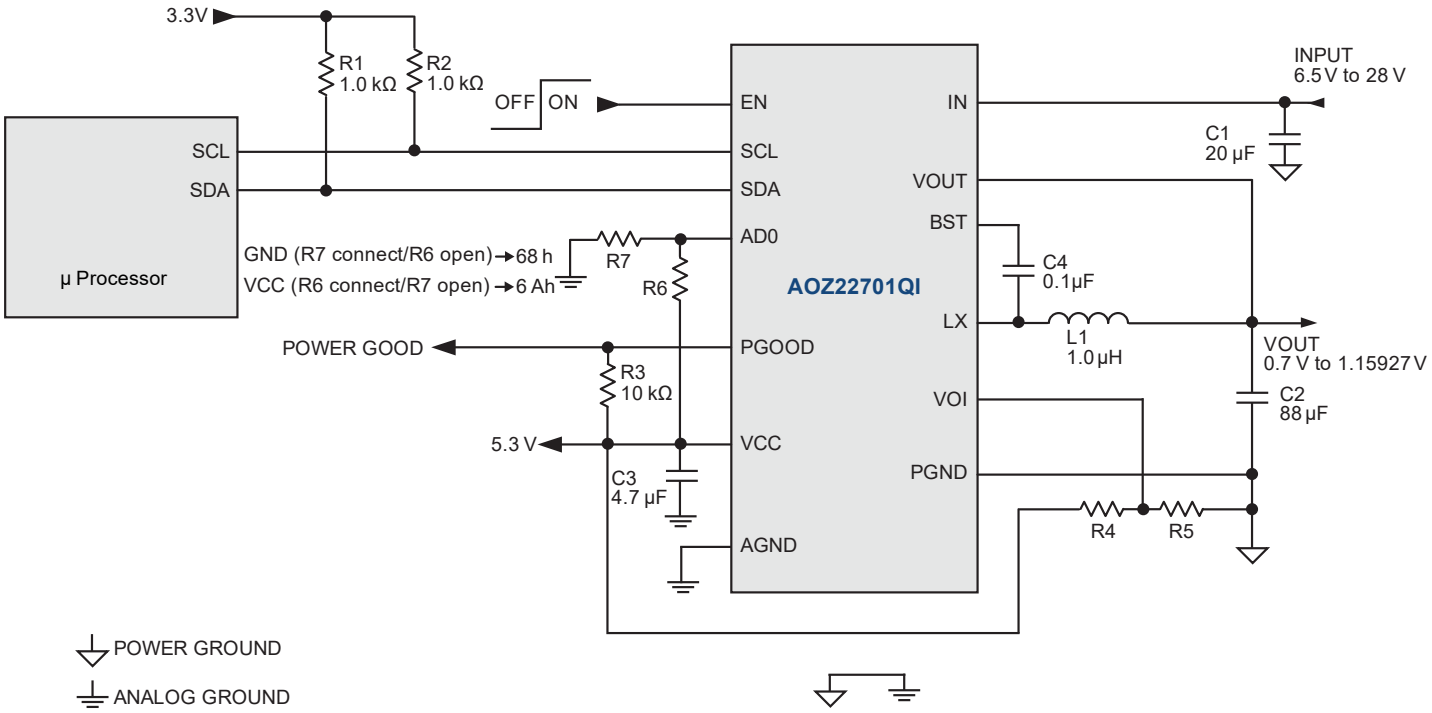
- Wide input voltage range
  - 6.5 V to 28 V
- 4 A continuous output current
- Output voltage adjustable down to 0.7 V to 1.15927 V in 7.29 mV
- ±1.0% output voltage accuracy for I^2C control
- Low $R_{DS(ON)}$ internal NFETs
  - 28 mΩ high-side
  - 28 mΩ low-side
- Constant on-time with input feed-forward
- Selectable PFM light-load operation
- Ceramic capacitor stable
- Power Good output
- I^2C address programming
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Over voltage protection
- Thermal shutdown
- Thermally enhanced 4 mm x 4 mm QFN-22L package

Applications

- Portable computers
- Compact desktop PCs
- Servers
- Graphics cards
- Set-top boxes
- LCD TVs
- Cable modems
- Point-of-load DC/DC converters
- Telecom/Networking/Datacom equipment

Green Product

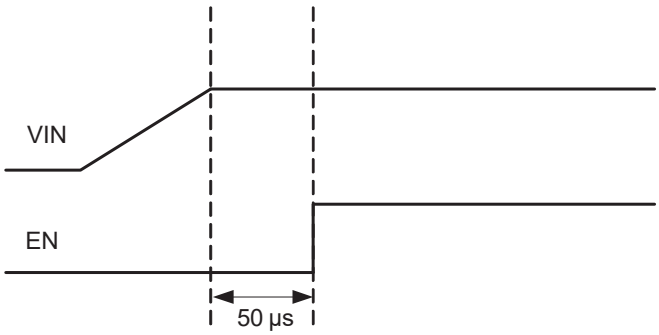
Typical Application



Option Table

Item / Code	AD0	Address (Binary)	Address (Hex)
AOZ22701QI	Ground (0)	01101000	68h
	VCC(1)	01101010	6Ah
AOZ22702QI	Ground (0)	01101100	6Ch
	VCC (1)	01101110	6Eh

Recommended Start-up Sequence

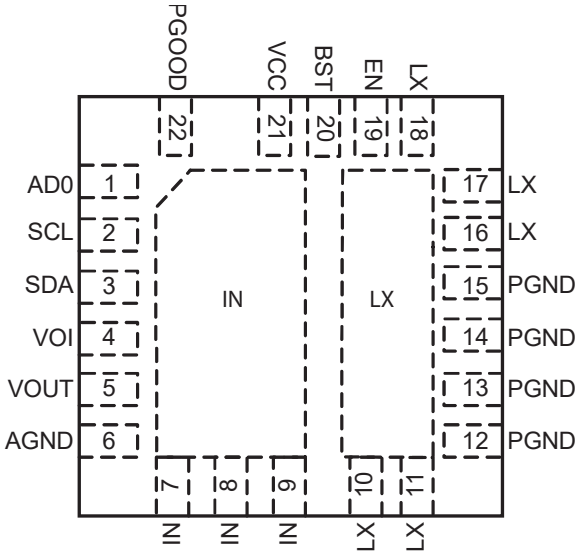


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ22701QI	-40 °C to +85 °C	22-Pin 4 mm x 4 mm QFN	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



22-Pin 4 mm x 4 mm QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	AD0	Chip Address. The AD0 pin just connects to AOZ22701QI VCC pin or GND.
2	SCL	Clock I/O Terminal.
3	SDA	Data I/O Terminal.
4	VOI	Initial Output Voltage Feedback Input. Adjust the output voltage with a resistive voltage-divider between VCC and AGND.
5	VOUT	Output Voltage Feedback Input. Connection to output voltage.
6	AGND	Analog Ground.
7, 8, 9	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
10, 11, 16, 17, 18	LX	Switching Node.
12, 13, 14, 15	PGND	Power Ground.
19	EN	Enable Input. The AOZ22701QI is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after IN is supplied.
20	BST	Bootstrap Capacitor Connection. The AOZ22701QI includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in Typical Application diagram.
21	VCC	Supply Input for Analog Functions. Bypass VCC to AGND with a 1µF~4.7µF ceramic capacitor. Place the capacitor close to VCC pin.
22	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
IN to AGND	-0.3 V to 30 V
LX to AGND(1)	-0.7 V to 30 V
BST to AGND	-0.3 V to 36 V
PGOOD, EN, VCC, SCL, SDA, VOUT, VOI, AD0 to AGND	-0.3 V to 6 V
PGND to AGND	-0.3 V to +0.3 V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating-HBM(2)	2 kV
ESD Rating-CDM	1 kV

Notes:

1. LX to PGND Transient (t<20 ns) ---------- -7 V to V_{IN}+7 V.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	6.5 V to 28 V
Output Voltage Range	0.7 V to 1.15927 V
Ambient Temperature (T_A)	-40°C to +85°C
Operating Junction Temperature (T_J)	-40°C to +145°C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	 32°C/W 6°C/W

Electrical Characteristics

T_A = 25 °C, V_{IN} = 12 V, EN = 5 V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

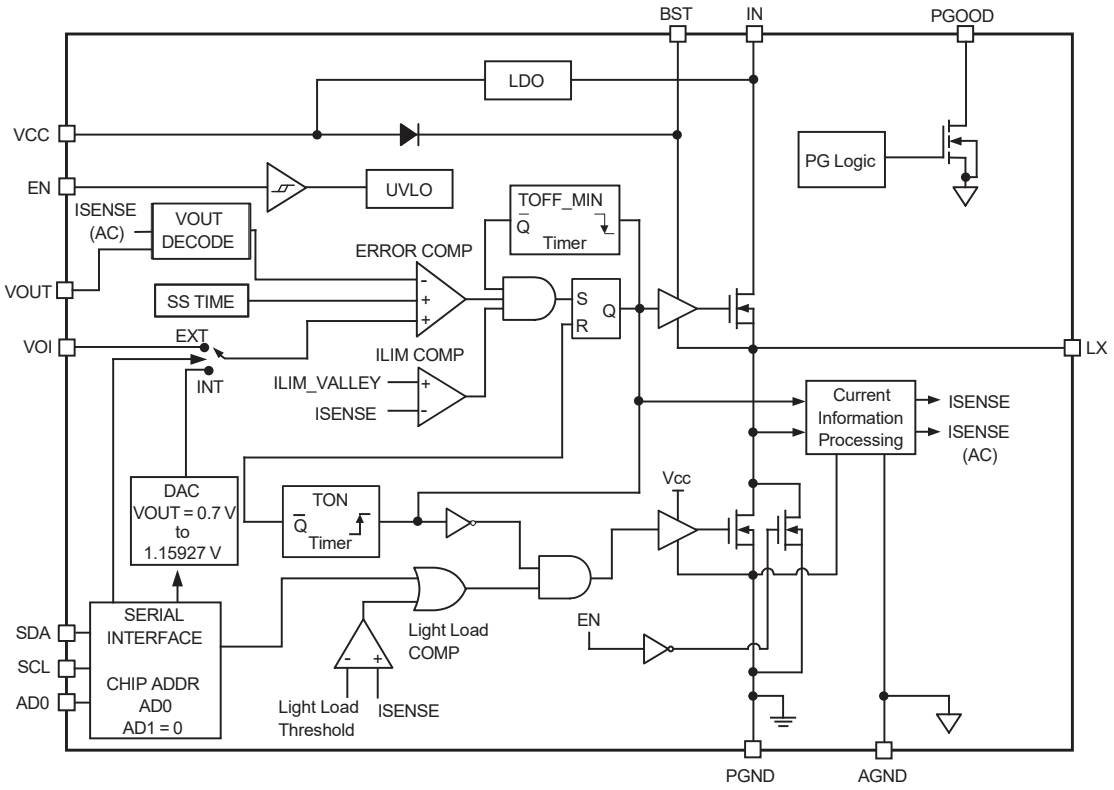
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	IN Supply Voltage		**6.5**		**28**	V
V_{UVLO}	Under-Voltage Lockout Threshold of V_{CC}	V_{CC} rising		**4.2**	**4.6**	V
		V_{CC} falling	**3.64**	**3.9**		
I_q	Quiescent Supply Current of V_{CC}	I_{OUT} = 0, V_{EN} > 2 V, PFM		**0.5**		mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0 V		**1**	**20**	µA
V_{OUT}	Output Voltage	T_A = 25°C, V_{IN} = 12 V V_{OUT} = 0.7 V to1.15927 V, L = 1 µH	-1%	0	1%	V_{OUT}
T_{r_OUT}	Output Voltage Rising Time	V_{OUT} = 0.7 V to 1.15927 V, C_{OUT} = 88 µF, PWM mode	2.5		25	µs
T_{f_OUT}	Output Voltage Falling Time	V_{OUT} = 0.7 V to 1.15927 V, C_{OUT} = 88 µF, PWM mode	2.5		25	µs
Enable						
V_{EN}	EN Input Threshold	Off threshold			0.5	V
		On threshold	1.4			
V_{EN_HYS}	EN Input Hysteresis			100		mV

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AD0						
V_{AD0}	AD0 Input Threshold	Off threshold			0.5	V
		On threshold	4.2			
Modulator						
f_{SW}	Operating Frequency			400		kHz
T_{ON_MIN}	Minimum On Time			100		ns
T_{ON_MAX}	Maximum On Time			2.6		µs
T_{OFF_MAX}	Maximum Off Time			300		ns
Soft-Start						
T_{SS_OUT}	SS Source Current	for PGOOD pulled High		4		ms
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			0.5	V
	PGOOD Leakage Current				±1	µA
V_{PGH}	PGOOD Threshold (Low level to High level)	V_{OUT} rising		90		%
V_{PGL}	PGOOD Threshold (High level to Low level)	V_{OUT} rising		120		%
		V_{OUT} falling		85		%
	PGOOD Threshold Hysteresis			5		%
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	V_{OUT} falling		50		%
V_{PH}	Over Voltage Threshold	V_{OUT} rising		120		%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	V_{IN} = 12V		28		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 12V		28		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
V_{CC} Output						
V_{CC}	V_{CC} Output Voltage	V_{IN} ≥ 6.5V, ICC= 0mA	4.97	5.3	5.6	V
I_{CC}	V_{CC} Current Limit	V_{IN} ≥ 6.5V	50			mA
Over-current and Thermal Protection						
I_{LIM}	Current Limit		6			A
	Thermal Shutdown Threshold	T_J rising		100		°C
		T_J falling		100		

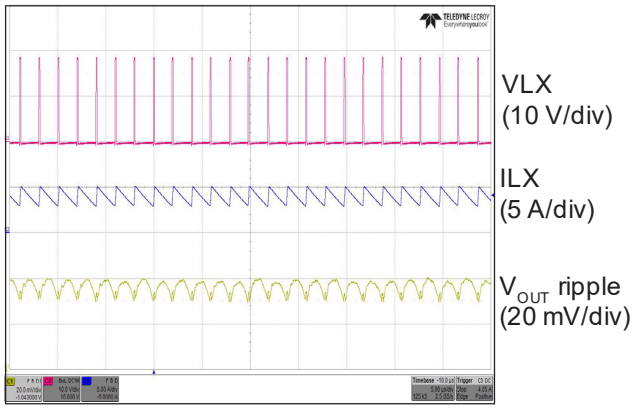
Functional Block Diagram



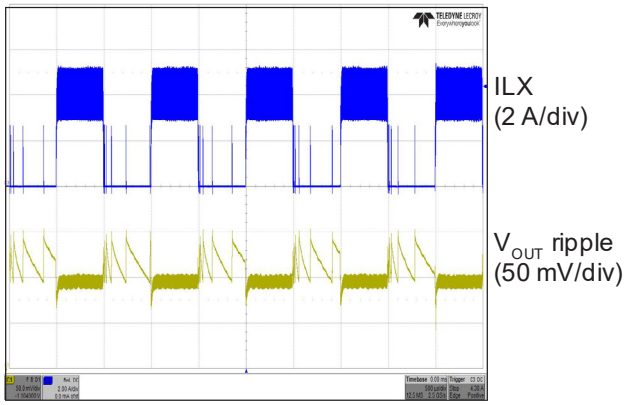
Typical Characteristics

T_A = 25 °C, V_{IN} = 19 V, V_{OUT} = 0.9 V, fs = 400 kHz, unless otherwise specified.

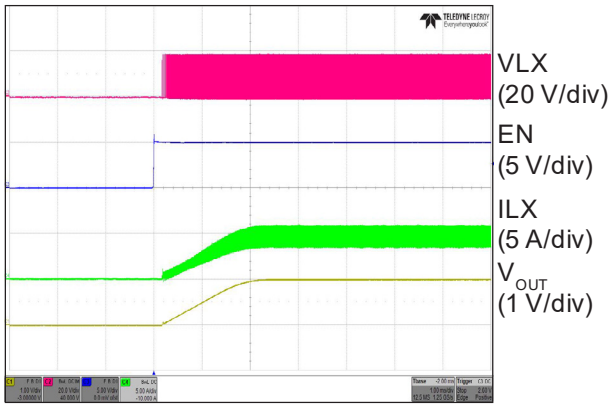
Normal Operation



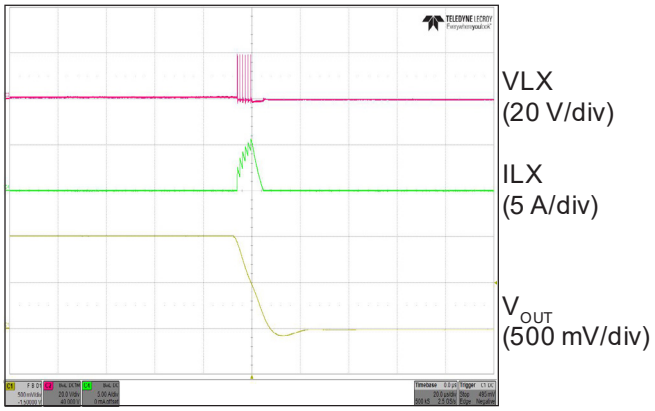
Load Transient 0 A to 4 A



Full Load Start-up



Short Circuit Protection



Efficiency vs. Load Current

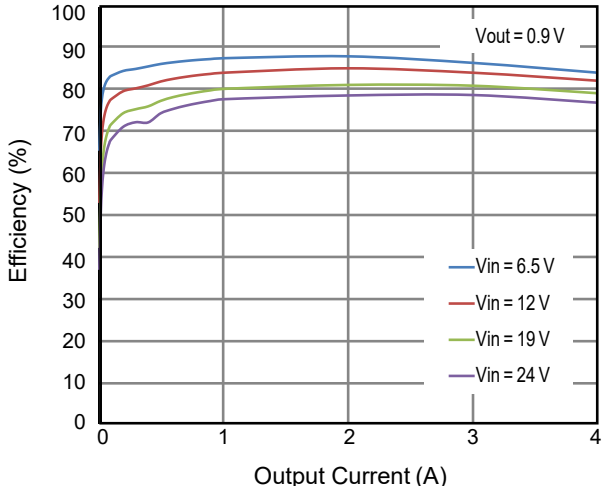


Table 1. I²C Control Specification(3)(4)(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage				0.6	V
V_{IH}	High Level Input Voltage		2.9			V
V_{hys}	Hysteresis of Schmitt Trigger Inputs		0.11			V
V_{OL}	Low Level Output Voltage (Open Drain, 3 mA Sink Current)				0.4	V
T_{SP}	Pulse Width of Spikes Suppressed by Input Filter		32			ns
f_{SCL}	SCL Clock Frequency				400	kHz
$t_{HD;STA}$	Hold Time (Repeated), START Condition		0.6			µs
t_{LOW}	Low Period of SCL Clock		1.3			µs
t_{HIGH}	High Period of SCL Clock		0.6			µs
$t_{SU;STA}$	Set-up Time for a Repeated START Condition		0.6			µs
$t_{HD;DAT}$	Data Hold Time		50		900	ns
$t_{SU;DAT}$	Data Set-up Time		100			ns
t_r	Rise Time (SDA or SCL)		$20+0.1C_b$		300	ns
t_f	Fall Time (SDA or SCL)		$5+0.1C_b$		300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition		0.6			µs
t_{BUF}	Bus Free Time Between STOP and START Conditions		1.3			µs
C_b	Capacitive Load for each Bus Line				400	pF
I_D	SDA Driver Capability		25		100	mA

Notes:

3. Ensured by design. Not production tested.
4. Refer to Figure 1 for I²C timing definitions.
5. C_b = capacitance of bus line in pF.

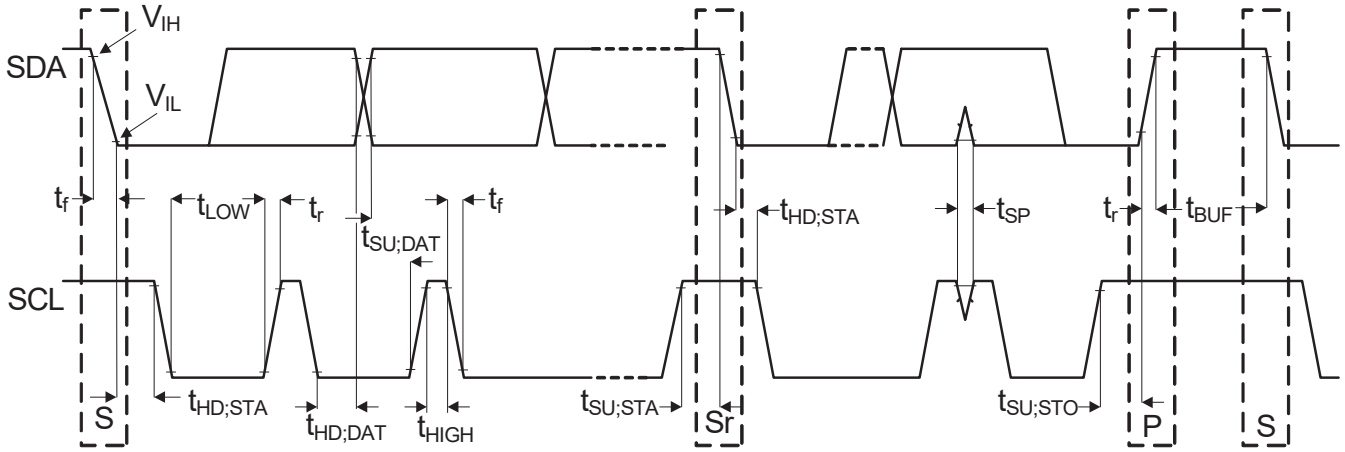


Figure 1. I²C Timing Definitions

Table 2. I²C Register Maps

Register Name	Register Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Output Voltage	00	Odd Parity	Output Voltage [6:0]						
Control A	01	Internal Mode			Output Voltage Change	PFMb			Protection Mode

Table 3. Summary of Default Control Bits

Control Bit(s)	Default	Function
VOUT [6:0]	0110010	VOUT code, 7 bits VOUT [6:0]. Part default to 0.83122V.
Internal Mode	0 (External Mode)	0 case: External Mode 1 case: Internal Mode (1) If set to 1, the part switches to internal mode and VOUT register value controls output voltage. (2) The part can be set back to external control mode at any time by wiring this bit to 0.
Output Voltage Change	0	0 case: Internal protection on 1 case: Internal protection off (1) If set to 0, when VOUT code change, the internal protection isn't turned off. (2) If set to 1, when VOUT code change, the internal protection is turned off to avoid triggering internal protection.
PFMb	1	Select PFM or PWM at light load. 0 case: PFM 1 case: PWM Part defaults to PWM.
Protection Mode	1	Select Latch-off or Auto-recovery for protection. 0 case: Auto-recovery mode 1 case: Latch-off mode Part defaults to Latch-off mode.

Odd Parity Bit

The odd parity bit is set by the Master controller to be the exclusive-NOR of the output voltage [6:0] bits. It will be used by the AOZ22701QI to check that a valid data byte has been received. If odd parity is not equal to the exclusive-NOR of the output voltage [6:0] bits, the AOZ22701QI assumes that an error has been occurred during the data transmission, and it will not send an ACK bit, nor will it reset the VOUT to the received code (or, if the Control register will not reset the register contents as requested). The Master should try again to re-send the data. When reading back the VOUT register, the parity bit is sent back.

I²C Serial Interface Description

The AOZ22701QI serial data interface works as an I²C slave device. It supports most standard data transfer mode (100kbps) and fast transfer mode (400kbps). The serial interface provides the mean to program a precision resistor DAC to set up a VID output voltage control for the 4A DC/DC converter. A one-byte data is written by the I²C Master to the AOZ22701QI and stored in a data buffer for the VID. The content of the data buffer can also be read back by the Master. After I²C is enabled, the AOZ22701QI starts to check the address code sent by the Master every time a START condition is detected. If a valid address code, AD[6:0], is recognized, it will send out an ACK bit by pulling down on the SDA bus during the clock pulse 9 of the SCL bus. The ACK time of the clock pulse 9 of the SCL bus can be written as below:

$$T_{ACK} = 9 \times \frac{1}{f_{SCL}}$$

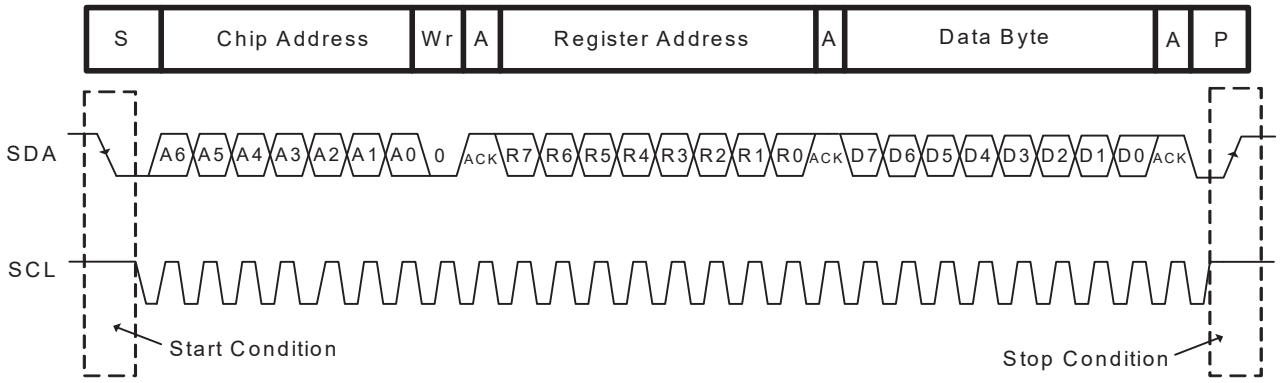


Figure 2. A Complete Write Byte Transfer

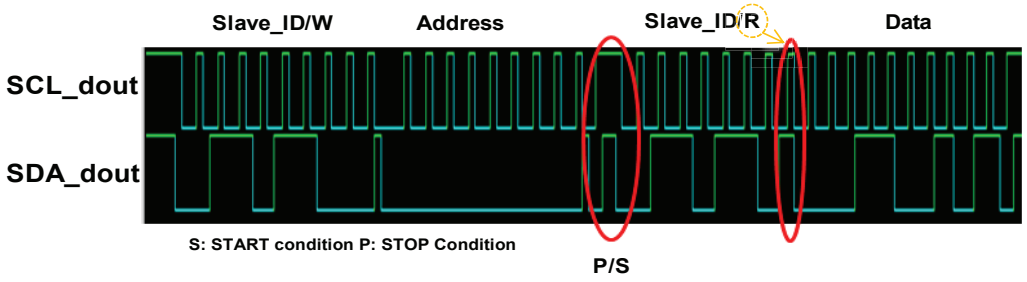


Figure 3. Single Read

Figure 4. Single Write

If no valid address is detected, no action will be taken and no ACK will be sent. The I^2C controller assumes the address is for other I^2C device and it will ignore the data bits and resume the search for the next valid address transfer. Finally, the response time from entering command to changing internal function is shown as below:

$$T_R = 27 \times \frac{1}{f_{SCL}}$$

After a valid address code is confirmed, the next bit (Wr) is checked for Write (“0”) or Read (“1”) mode. If the requested operation is Write mode, the AOZ22701QI will evaluate the data code, D[7:0], received after the address ACK.

Once the Write data is validated, AOZ22701QI will send ACK on the SDA bus. The data code will also be transferred to the data holding buffer of the VID and the output voltage will move to the new, or ideal, value. If the data is not valid, no ACK will be sent. It will be up to the I^2C Master to repeat the operation.

If the requested operation is Read mode, the AOZ22701QI will transmit the content of the VID data buffer register, or D[7:0], on the SDA bus. After the 8 data bits are transmitted and STOP detected, the AOZ22701QI will return to the normal operation regardless of ACK is received or not. It will be up to the I^2C Master to re-send a Read request if the last Read operation is deemed invalid.

Table 4. Output Voltage Setting vs. Register Code

Code	Binary	VOUT	Code	Binary	VOUT	Code	Binary	VOUT	Code	Binary	VOUT
0	0000000	0.7	32	0100000	0.7	64	1000000	0.93328	96	1100000	0.93328
1	0000001	0.70729	33	0100001	0.70729	65	1000001	0.94057	97	1100001	0.94057
2	0000010	0.71458	34	0100010	0.71458	66	1000010	0.94786	98	1100010	0.94786
3	0000011	0.72187	35	0100011	0.72187	67	1000011	0.95515	99	1100011	0.95515
4	0000100	0.72916	36	0100100	0.72916	68	1000100	0.96244	100	1100100	0.96244
5	0000101	0.73645	37	0100101	0.73645	69	1000101	0.96973	101	1100101	0.96973
6	0000110	0.74374	38	0100110	0.74374	70	1000110	0.97702	102	1100110	0.97702
7	0000111	0.75103	39	0100111	0.75103	71	1000111	0.98431	103	1100111	0.98431
8	0001000	0.75832	40	0101000	0.75832	72	1001000	0.9916	104	1101000	0.9916
9	0001001	0.76561	41	0101001	0.76561	73	1001001	0.99889	105	1101001	0.99889
10	0001010	0.7729	42	0101010	0.7729	74	1001010	1.00618	106	1101010	1.00618
11	0001011	0.78019	43	0101011	0.78019	75	1001011	1.01347	107	1101011	1.01347
12	0001100	0.78748	44	0101100	0.78748	76	1001100	1.02076	108	1101100	1.02076
13	0001101	0.79477	45	0101101	0.79477	77	1001101	1.02805	109	1101101	1.02805
14	0001110	0.80206	46	0101110	0.80206	78	1001110	1.03534	110	1101110	1.03534
15	0001111	0.80935	47	0101111	0.80935	79	1001111	1.04263	111	1101111	1.04263
16	0010000	0.81664	48	0110000	0.81664	80	1010000	1.04992	112	1110000	1.04992
17	0010001	0.82393	49	0110001	0.82393	81	1010001	1.05721	113	1110001	1.05721
18	0010010	0.83122	50	0110010	0.83122	82	1010010	1.0645	114	1110010	1.0645
19	0010011	0.83851	51	0110011	0.83851	83	1010011	1.07179	115	1110011	1.07179
20	0010100	0.8458	52	0110100	0.8458	84	1010100	1.07908	116	1110100	1.07908
21	0010101	0.85309	53	0110101	0.85309	85	1010101	1.08637	117	1110101	1.08637
22	0010110	0.86038	54	0110110	0.86038	86	1010110	1.09366	118	1110110	1.09366
23	0010111	0.86767	55	0110111	0.86767	87	1010111	1.10095	119	1110111	1.10095
24	0011000	0.87496	56	0111000	0.87496	88	1011000	1.10824	120	1111000	1.10824
25	0011001	0.88225	57	0111001	0.88225	89	1011001	1.11553	121	1111001	1.11553
26	0011010	0.88954	58	0111010	0.88954	90	1011010	1.12282	122	1111010	1.12282
27	0011011	0.89683	59	0111011	0.89683	91	1011011	1.13011	123	1111011	1.13011
28	0011100	0.90412	60	0111100	0.90412	92	1011100	1.1374	124	1111100	1.1374
29	0011101	0.91141	61	0111101	0.91141	93	1011101	1.14469	125	1111101	1.14469
30	0011110	0.9187	62	0111110	0.9187	94	1011110	1.15198	126	1111110	1.15198
31	0011111	0.92599	63	0111111	0.92599	95	1011111	1.15927	127	1111111	1.15927

Detailed Description

The AOZ22701QI is a high-efficiency, easy-to-use, synchronous buck regulator with a voltage scaling control to power up MCUs requiring core voltage tune-ups. After the initial power up, the output voltage can be programmed/scaled by VID codes sent over an I^2C compatible bus. The regulator is capable of supplying 4A of continuous output current with an output voltage adjustable from 0.7V to 1.15927V.

The input voltage of AOZ22701QI can be as low as 6.5V. The highest input voltage of AOZ22701QI can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with ceramics output capacitor. Protection features include V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over voltage and under voltage protection, short circuit protection, and thermal shutdown.

The AOZ22701QI is available in 22-pin 4mm×4mm QFN package.

Input Power Architecture

The AOZ22701QI integrates an internal linear regulator to generate 5.3V (±5%) V_{CC} from input. If input voltage is lower than 5.3V, the linear regulator operates at low drop-output mode; the V_{CC} voltage is equal to input voltage minus the drop-output voltage of internal linear regulator.

Enable and Soft Start

The AOZ22701QI has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft start process begins when V_{CC} rises to 4.2V and voltage on EN pin is HIGH. The output voltage follows the internal voltage of soft-start (V_{SS}) when it is lower than initial output voltage. When V_{SS} is higher than initial output voltage, the voltage of VOUT pin is regulated by internal precise band-gap voltage. Moreover, the soft start period between EN and PGOOD is 4ms. The soft start sequence of AOZ22701QI is shown in Figure 5.

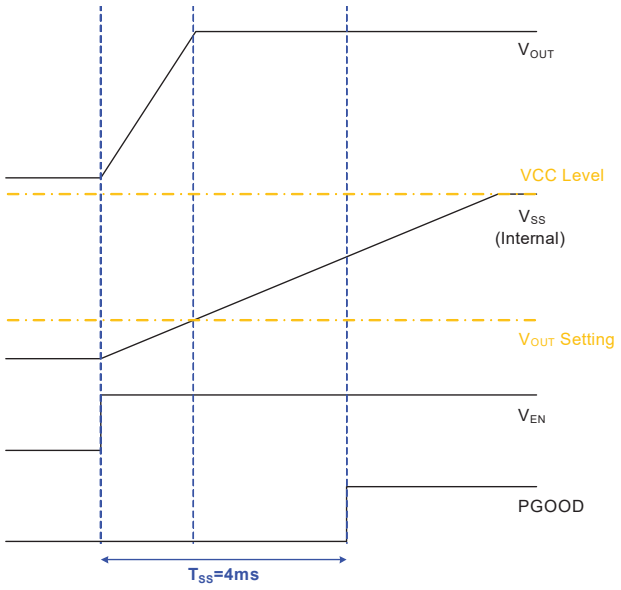


Figure 5. Soft Start Sequence of AOZ22701QI

Enable

The AOZ22701QI has an embedded discharge path, including a 100kΩ resistor and an M1 NMOS device. This discharge path is activated when V_{IN}(Input Voltage) is high and V_{EN}(Enable Voltage) is low. The internal circuit of EN pin is shown in Figure 6.

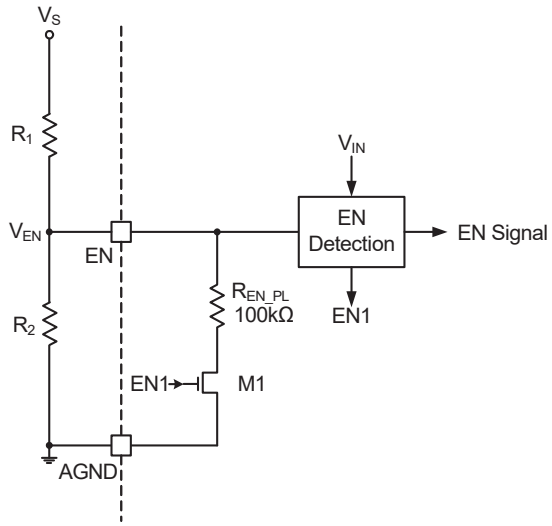


Figure 6. Enable Internal Circuit

There are two different enable control methods:

1. Connection to EN pin by an external resistive voltage divider.
2. Direct connection to EN pin by an external power source, V_S.

In the first condition, we must consider the internal pull down resistance by using a divider circuit with an external power source V_S to get V_{EN}. The V_{EN} can be calculated by the following formula:

$$V_{EN} = \frac{R_2 // R_{EN\_PL}}{R_1 + (R_2 // R_{EN\_PL})} \times V_s$$

When the V_{IN} is high and the V_{EN} is high, the EN internal M1 is turned off, and then the pull down resistance is removed for V_{EN}, the V_{EN} can be re-calculated by:

$$V_{EN} = \frac{R_2}{R_1 + R_2} \times V_s$$

In the second condition, the AOZ22701QI will be turned on when the V_{EN} is higher than 1.4 V, and will be turned off when the V_{EN} is lower than 0.5 V. The simplified schematic and timing sequence are shown in Figure 7.

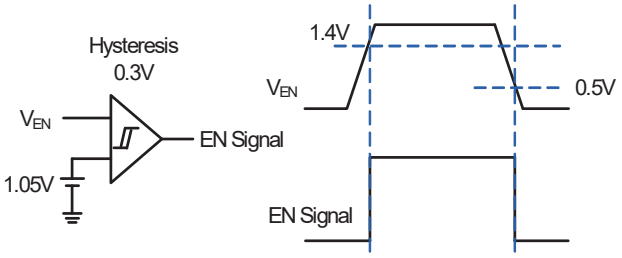


Figure 7. Enable Threshold Schematic and Timing Sequence

I²C Chip Address Byte (AD0)

The AOZ22701QI can select addresses between 68h(01101000) and 6Ah(01101010) by AD0 terminal. Moreover, the internal AD1 terminal is pulled to low, allowing up to 2 AOZ22701QI to be controlled on the same I²C bus. The internal AD0 circuit is a hysteresis comparator. The input terminal (AD0) of the hysteresis comparator doesn't have pull down or pull up resistor, therefore, the AD0 pin needs to avoid the floating condition. The simplified schematic and timing sequence are shown in Figure 8.

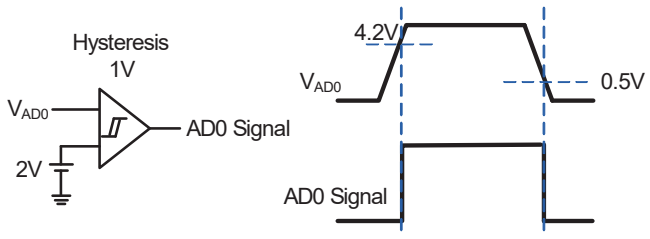


Figure 8. AD0 Schematic and Timing Sequence

Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of AOZ22701QI is constant-on time PWM control with input feed-forward. The simplified control schematic is shown in Figure 9. The high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage (IN). The one-shot is triggered when the internal VOI/DAC voltage is higher than the combined information of output voltage and the AC current information of inductor, which is processed and obtained through the sensed low-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant on-time control schemes.

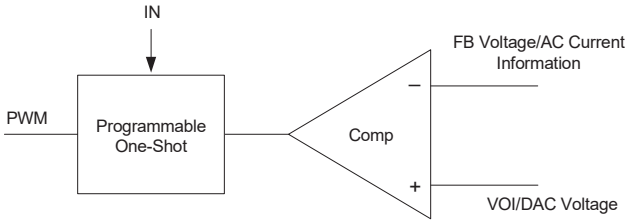


Figure 9. Simplified Control Schematic

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The AOZ22701QI senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the VOUT pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus, the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Current-Limit Protection

The AOZ22701QI has the current-limit protection by using $R_{DS(ON)}$ of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant-off time (300 ns typical) is implemented after a constant-on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual

peak is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 16 switching cycles, the AOZ22701QI considers this is a true failed condition and thus, turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ22701QI again.

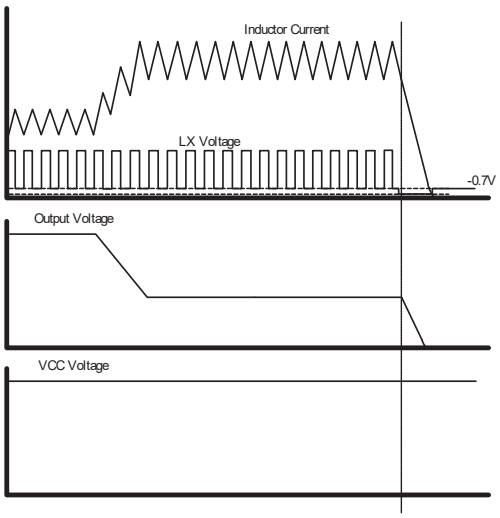


Figure 10. OCP Timing Chart

Output Voltage Under-Voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, AOZ22701QI turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ22701QI again.

Output Voltage Over-Voltage Protection

The threshold of OVP is set 20% higher than VOI/DAC voltage. When the voltage of VOUT pin exceeds the OVP threshold, high-side MOSFET is turned-off and low-side MOSFETs is turned-on until the voltage of VOUT pin is lower than VOI/DAC voltage.

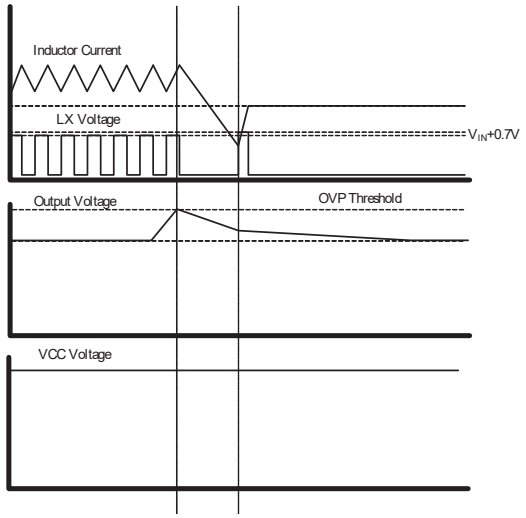


Figure 11. OVP Timing Chart

Output Voltage Registers

The AOZ22701QI has 7 bits of output voltage register control for output voltage adjusting from 0.7 V to1.15927 V. Output Voltage Setting vs Register Code shows the output voltage setting for DAC voltage and register codes. When the AOZ22701QI powers up, the startup and output voltage regulation conditions are set by the external resistor divider feedback to the VOI pin from VCC voltage. Therefore, the initial output voltage can be calculated by:

$$VOI = \frac{R_5}{R_4 + R_5} \times V_{CC}$$

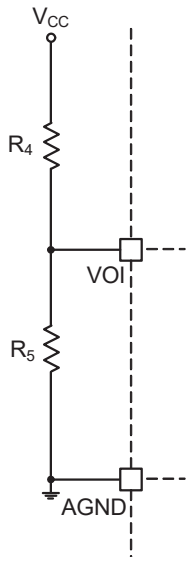


Figure 12. VOI Divided Circuit

Output Voltage Rising and Falling Time

We can adjust AOZ22701QI's output voltage level by the I^2C interface. The output voltage rising time and falling time is determined by our internal slew-rate control circuit. Resulted from various output voltage change points, it makes different rising and falling time. If the output voltage starts to change at the peak of output voltage, it takes less time to achieve new output voltage level than from the valley. The difference of their rising time in the same sample is approximately 1/2 of switching cycle time.

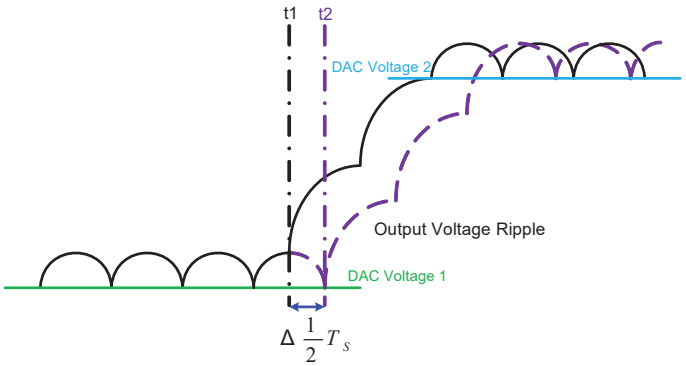


Figure 13. Variations of Output Voltage Rising Time

Application Information

The basic AOZ22701QI application circuit is shown in Typical Application section. The component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ22701QI to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7 µF, should be connected to the V_{CC} pin and AGND pin for stable operation of the AOZ22701QI. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

if let m equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 14. It can be seen that when V_{OUT} is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_{OUT}$.

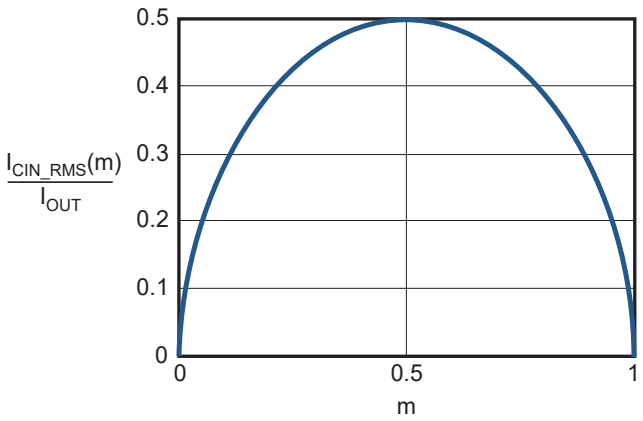


Figure 14. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are referred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR_{COUT} + \frac{1}{8 \times f \times C_{OUT}}\right)$$

where, C_{OUT} is output capacitor value and ESR_{COUT} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times f \times C_{OUT}}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{COUT}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Thermal Management and Layout Consideration

In the AOZ22701QI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the IN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ22701QI.

In the AOZ22701QI buck regulator circuit, the major power dissipating components are the AOZ22701QI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT}$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor and output current.

$$P_{inductor\_loss} = I_{OUT}^{2} \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ22701QI and thermal impedance from junction to ambient.

$$T_{junction} = \left(P_{total\_loss} - P_{inductor\_loss} \right) * \Theta_{JA} + T_{A}$$

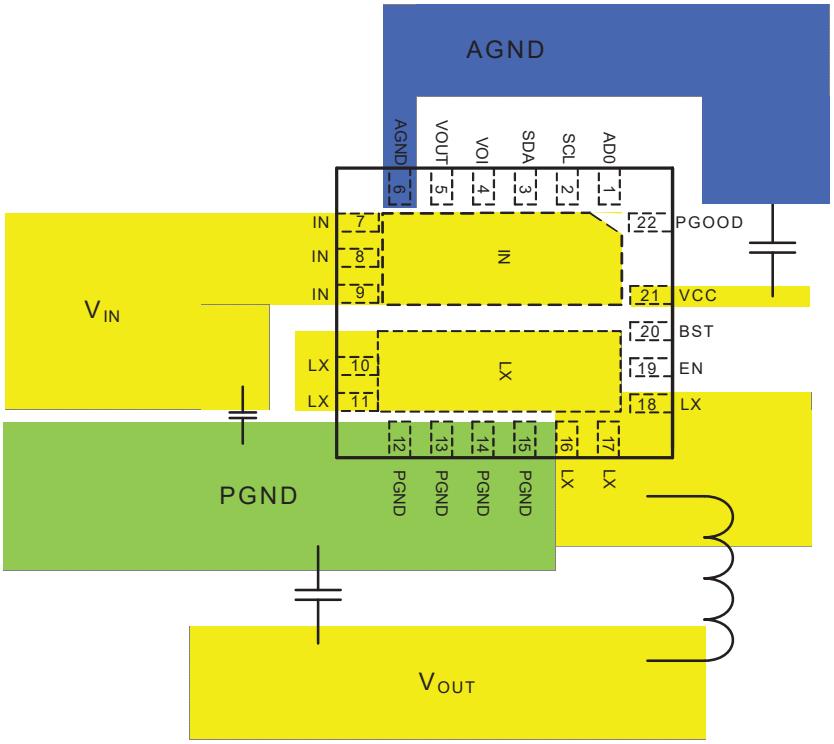
The maximum junction temperature of AOZ22701QI is 150ºC, which limits the maximum load current capability.

The thermal performance of the AOZ22701QI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

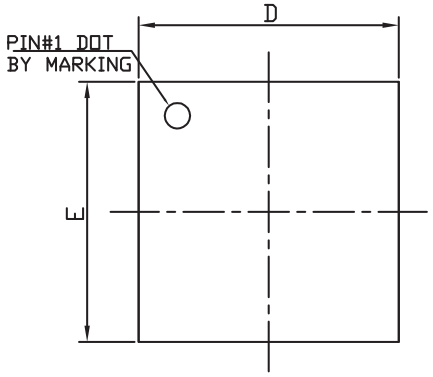
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

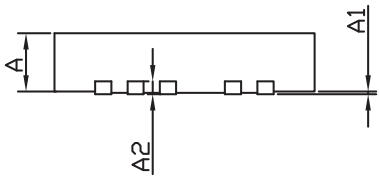
1. Connected a small copper plane to LX pin to have lower noise interference area.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor C_{VCC} should be connected to V_{CC} and AGND as close as possible.
5. Keep sensitive signal traces such as output trace faraway from the LX pins.
6. Let digital pins such as AD0, SCL and SDA, to use AGND.
7. Let VOI pin to use AGND.
8. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.



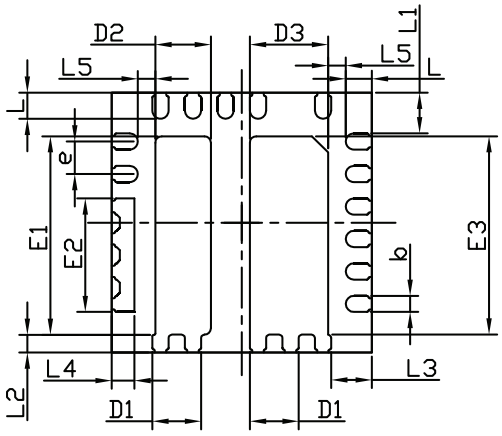
Package Dimensions, QFN 4x4-22L



TOP VIEW

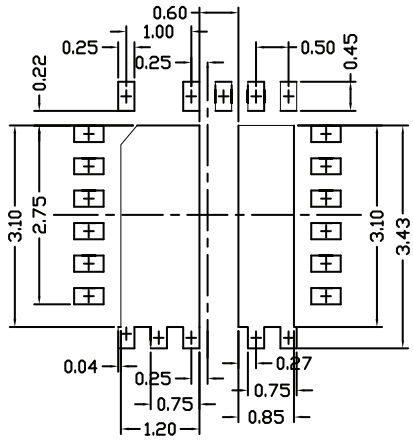


SIDE VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN



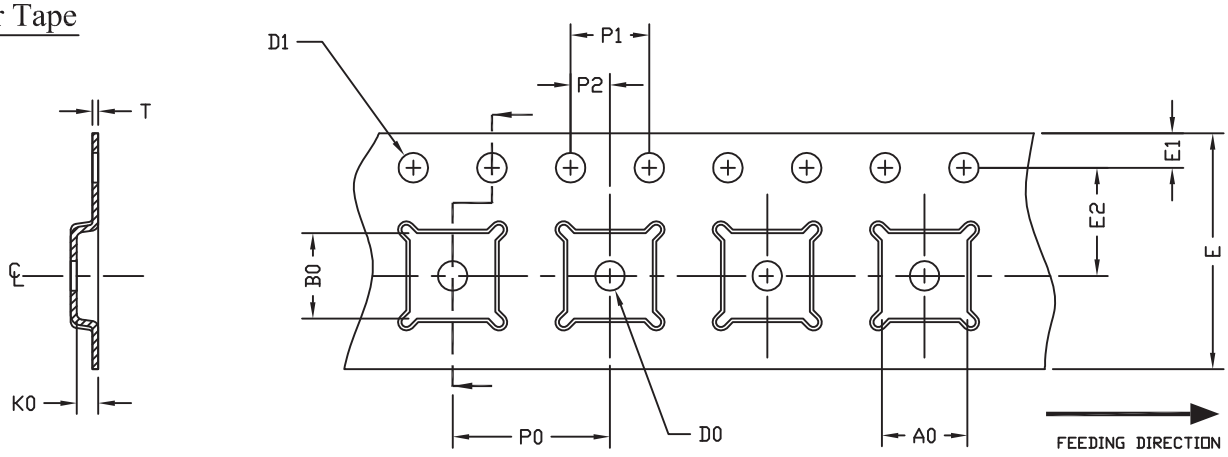
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	---	0.002
A2		0.2 REF			0.008 REF	
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.65	1.75	1.85	0.065	0.069	0.073
E3	2.95	3.05	3.15	0.116	0.120	0.124
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.034
D2	0.75	0.85	0.95	0.029	0.033	0.037
D3	1.10	1.20	1.30	0.043	0.047	0.051
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
L3	0.57	0.62	0.67	0.022	0.024	0.026
L4	0.30	0.35	0.40	0.012	0.014	0.016
L5	0.17	0.27	0.37	0.007	0.011	0.015
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020 BSC	

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE : 0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: 0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

Tape and Reel Dimensions, QFN 4x4-22L

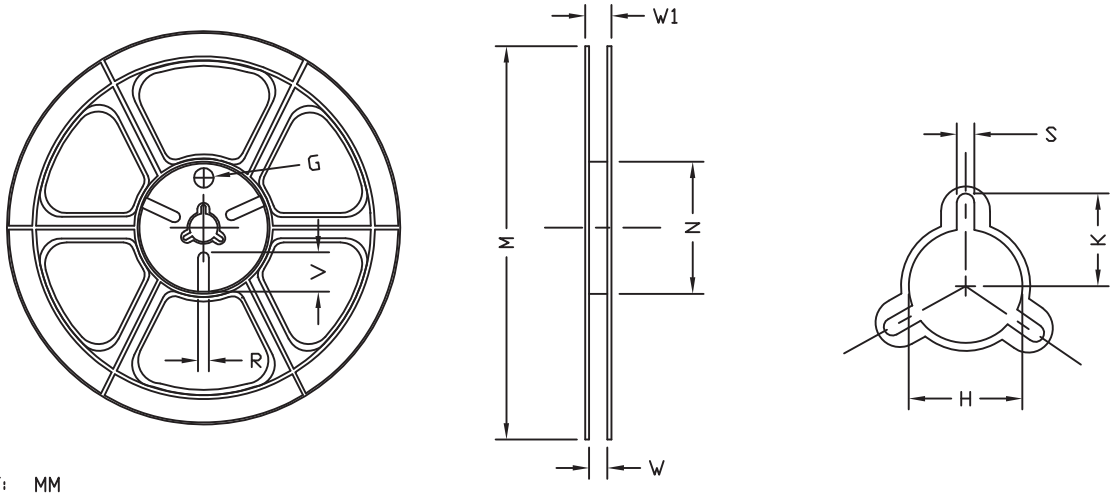
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

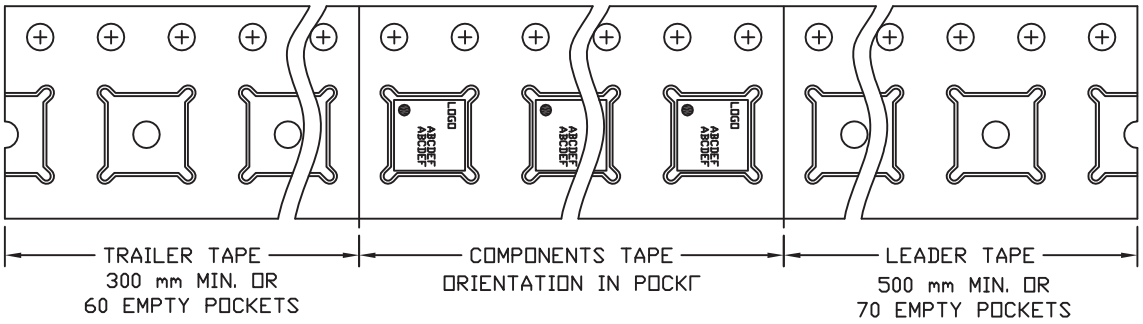


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

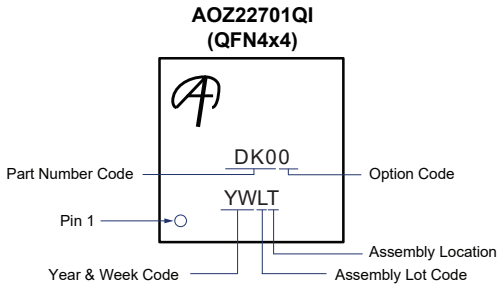
Tape

Leader / Trailer & Orientation



Unit Per Reel: 3000pcs

Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.