AOZ23567QI

28V/22A Synchronous EZBuck™ Regulator

General Description

The AOZ23567QI is a high-efficiency, easy-to-use DC/DC synchronous buck regulator that operates up to 28V. The device is capable of supplying 22A of continuous output current with an output voltage adjustable down to 0.6V (±1.0%).

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range. A low 70ns minimum on-time enables very low output voltages at ultra-high operating frequencies.

Integrated AC ripple injection enables all-ceramic low ESR output filter capacitors and smaller PCB footprint with no external components needed.

Selectable PFM mode optimizes light load efficiency while forced PWM mode maintains constant frequency for lower harmonic noise.

The device features multiple protection functions such as V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ23567QI is available in a 5mm×5mm QFN-36L package and is rated over a -40°C to +85°C ambient temperature range.

Features

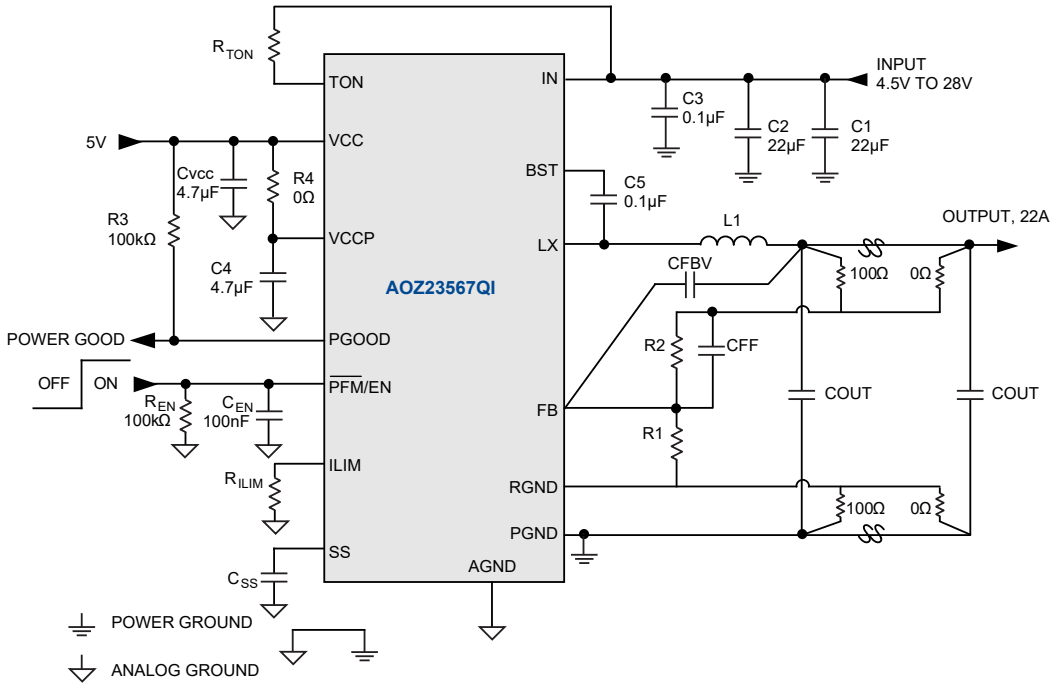
- Wide input voltage range
  - 4.5V to 28V
- Support Intel I_{TDC} up to 22A
- Support Intel I_{CCMAX} up to 45A
- Output voltage adjustable down to 0.6V (±1.0%)
- Low $R_{DS(ON)}$ internal NFETs
  - 5mΩ high-side
  - 1.8mΩ low-side
- Constant on-time with input feed-forward
- Programmable on-time up to 3.5µs and down to 70ns
- Programmable Switching Frequency Range up to 1MHz (For 12 V_{IN} to 1 V_{OUT})
- Selectable PFM or forced PWM light load operation
- Ceramic capacitor stable
- Remote sense
- Adjustable current limit setting
- Adjustable soft-start
- Power Good output
- Integrated bootstrap diode
- Under-voltage protection and over-voltage protection
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Thermally enhanced 36-pin 5mm×5mm QFN

Applications

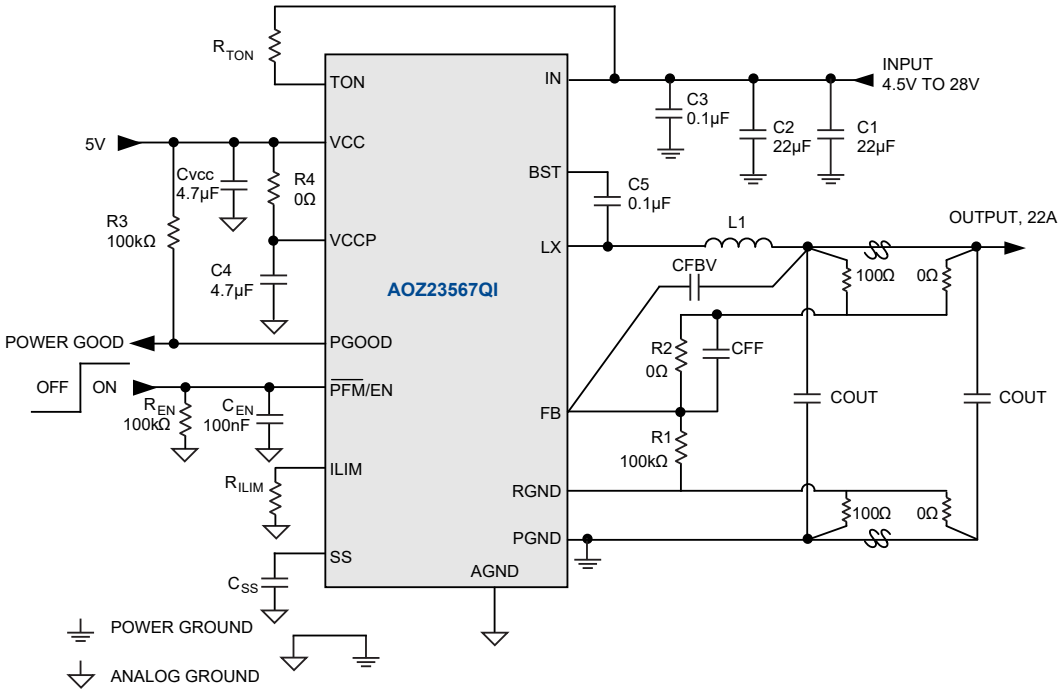
- Compact PCs and gaming systems
- Set-top boxes and LCD TVs
- Server & Storage systems
- Datacom and networking
- Embedded Computing
- Point-of-load DC/DC Converters

GREEN Product

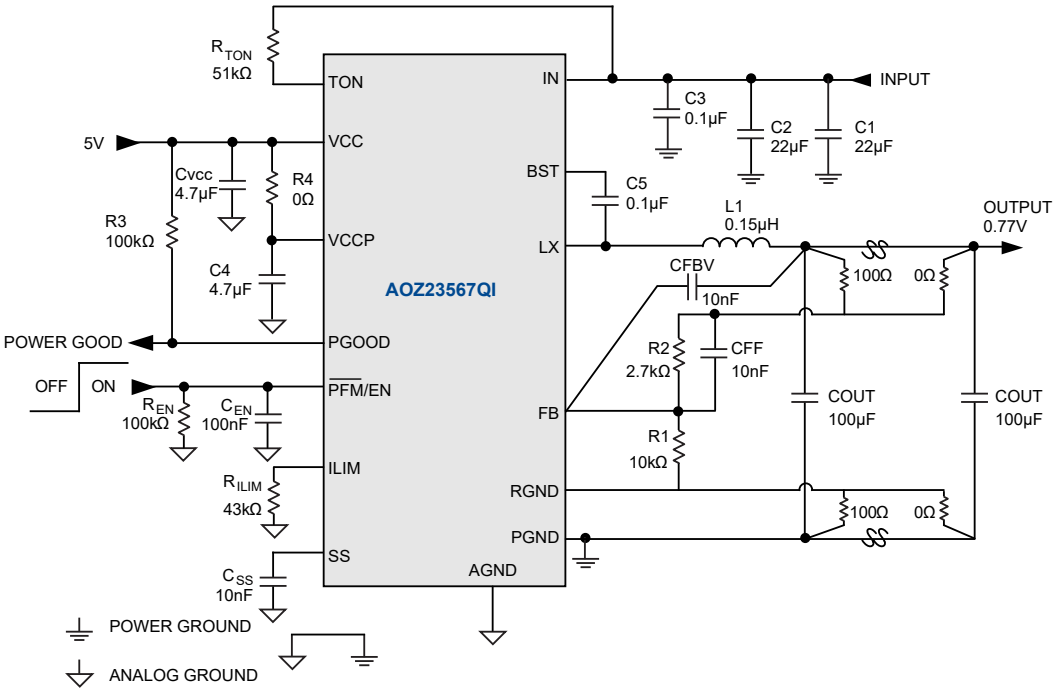
Typical Application



Output Voltage 0.6V Recommended Circuit



Intel VNNAON Application Circuit Output Voltage 0.77V



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ23567QI	-40°C to +85°C	QFN5x5-36L	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

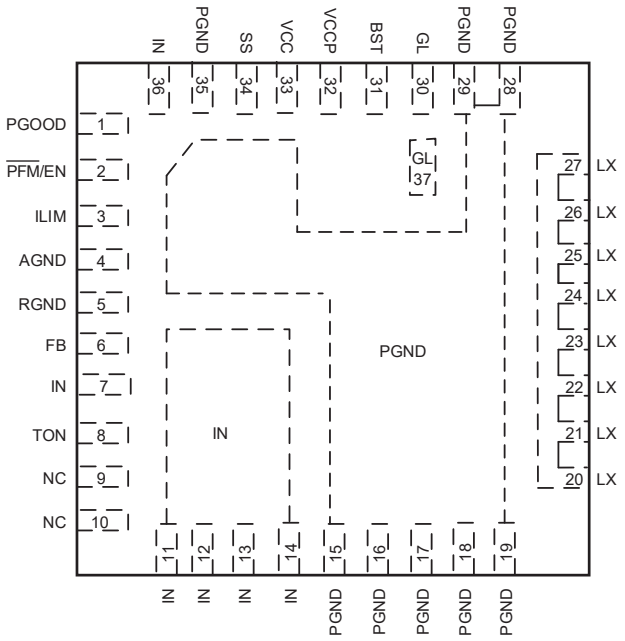


Figure 1. AOZ23567QI
36-Pin 5mmx5mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage for or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.
2	$\overline{\text{PFM}}$/EN	Multi-function pin. Enable Input and PFM Selection Input. AOZ23567QI is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after IN are well supplied. Power-off the device by EN off is suggested. Set this pin higher than PFM threshold for PFM operation to improve light load efficiency. Set this pin lower than PFM threshold for forced PWM operation.
3	ILIM	Current limitation level setting pin. Connect a resister between ILIM and GND to set over current protection level. No capacitor is allowed between ILIM and AGND.
4	AGND	Analog Ground.
5	RGND	Differential remote sense negative input.
6	FB	Feedback (Differential remote sense positive Input). Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
8	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on-time.
7, 11, 12, 13, 14, 36	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
15, 16, 17, 18, 19, 28, 29, 35	PGND	Power Ground.
20, 21, 22, 23, 24, 25, 26, 27	LX	Switching Node.
30, 37	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
31	BST	Bootstrap Capacitor Connection. The AOZ23567QI includes an internal bootstrap diode. Connect an external capacitor between BST and LX.
32	VCCP	Supply for MOSFETs drive stage. Bypass VCCP to AGND with a 4.7µF~10µF ceramic capacitor. Place the capacitor close to VCCP pin.
33	VCC	Supply for analog functions. Bypass VCC to AGND with a 4.7µF~10µF ceramic capacitor. Place the capacitor close to VCC pin.
34	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.
9,10	NC	No Connect.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
IN, TON to AGND	-0.3 V to +30 V
IN to LX[1]	-1.0 V to +30 V
LX to AGND[2]	-1.0 V to +30 V
BST to AGND	-0.3 V to +36 V
PGND to AGND	-0.3 V to +0.3 V
Other Pins to AGND	-0.3 V to 6 V
Junction Temperature (T_J)	+150 °C
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating-HBM[3]	2 kV
ESD Rating-CBM	1 kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	4.5 V to 28 V
Output Voltage Range	0.6 V to 0.85 V*V_{IN}
Ambient Temperature (T_A)	-40 °C to +85 °C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	 32 °C/W 4 °C/W

Notes:
1. IN to LX Transient (t<20 ns) ------- -7 V to Vin+7 V.
2. LX to PGND Transient (t<20 ns) ------- -7 V to Vin+7 V.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 kΩ in series with 100 pF.

Electrical Characteristics

T_A = 25 °C, V_{IN} = 12 V, V_{CC} = 5 V, EN = 5 V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40 °C to +85 °C

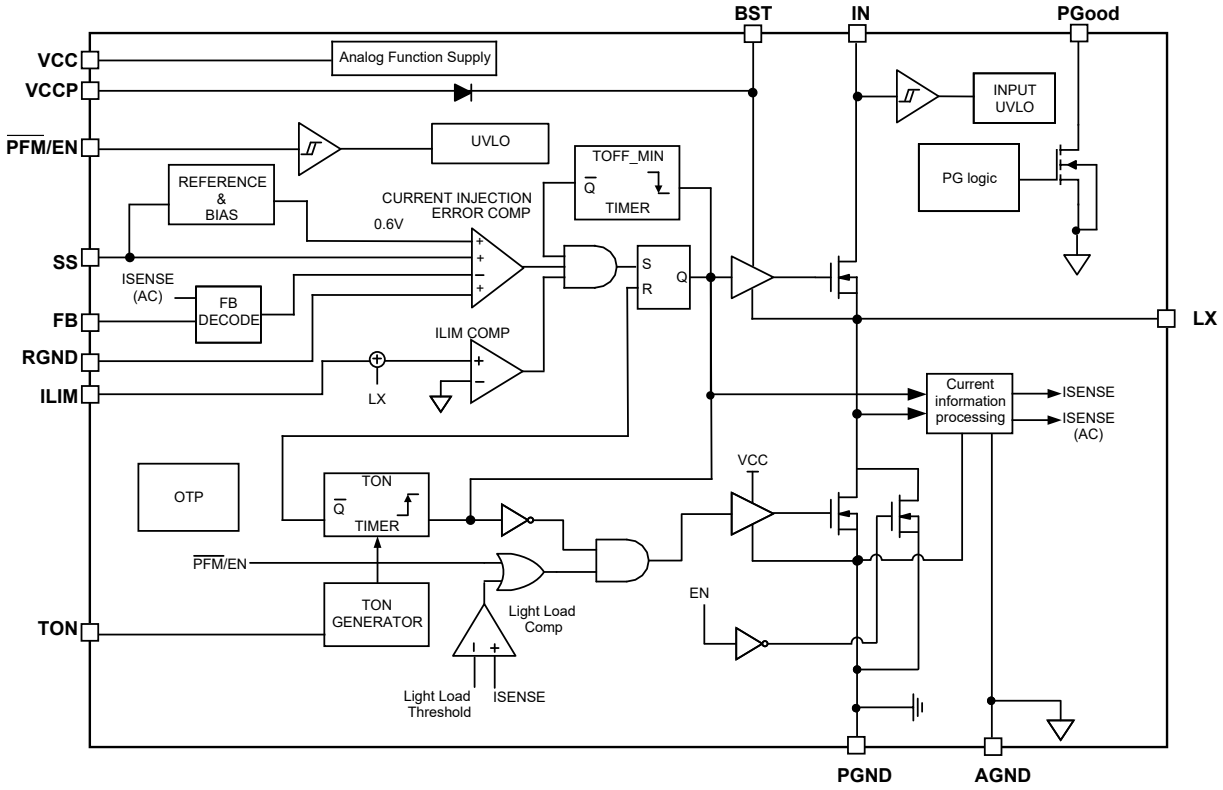
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	IN Supply Voltage		4.5		28	V
V_{IN_UVLO}	Under-Voltage Lockout Threshold of V_{IN}	V_{IN} rising V_{IN} falling	 2.9	3.5 3.2	3.8	V V
V_{VCC_UVLO}	Under-Voltage Lockout Threshold of V_{CC}	V_{CC} rising V_{CC} falling	 3.9	4.5 4.1	4.7	V V
I_q	Quiescent Supply Current of V_{CC}	I_{OUT} = 0 A, V_{EN}> 2 V, PFM mode		400		µA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0 V		15		µA
V_{REF}	Reference Voltage	T_A = 25 °C	594	600	606	mV
I_{FB}	FB Input Bias Current				200	nA
Enable/PFM						
V_{EN}	EN Input Threshold	Off threshold On threshold	 1.2		0.5	V V
V_{EN_HYS}	EN Input Hysteresis		100	250		mV
$V_{\overline{PFM}}$	PFM / PWM threshold	PFM Mode threshold Force PWM threshold	1.7 1.2		5 1.4	V
R_{DIS}	Enable-off Discharge Resistor	V_{EN} = 0 V, V_{CC} = 5 V	52	64	76	Ω

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, V_{CC} = 5V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Modulator						
T_{ON}	On-time	R_{TON} = 100kΩ, V_{IN} = 12V		200		ns
T_{ON_MIN}	Minimum On-time			70		ns
T_{ON_MAX}	Maximum On-time			3.5		µs
T_{OFF_MIN}	Minimum Off-time			350		ns
Soft-start						
I_{SS_OUT}	SS Source Current	V_{SS} = 0V C_{SS} = 0.001µF to 0.1µF	7	11	15	µA
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 1mA			**0.5**	V
	PGOOD Leakage Current				±1	µA
Current						
V_{PGH}	PGOOD Threshold (Low level to High level)	FB rising	82	90	98	%
V_{PGL}	PGOOD Threshold (High level to Low level)	FB rising FB falling	110 77	120 85	130 93	%
	PGOOD Threshold Hysteresis			5		%
Under-voltage and Over-voltage Protection						
V_{PL}	Under-voltage threshold	FB falling	40	50	60	%
V_{PH}	Over-voltage Threshold	FB rising	110	120	130	%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-resistance	V_{IN} = 12V		5		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
$R_{DS(ON)}$	Low-Side NFET On-resistance	V_{LX} = 12V		1.8		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Thermal Protection						
	Thermal Shutdown	T_J rising		150		°C

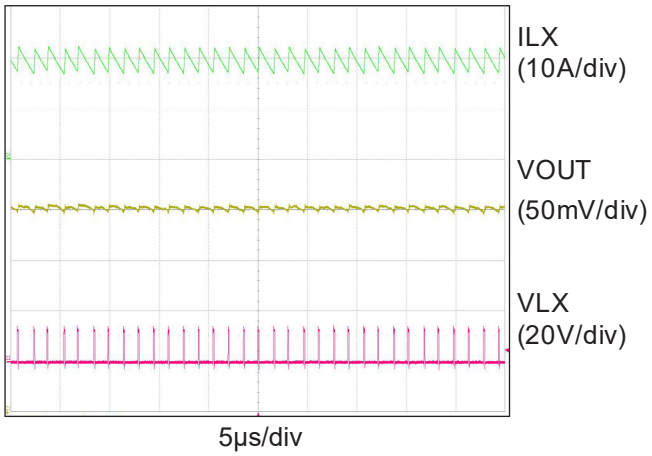
Functional Block Diagram



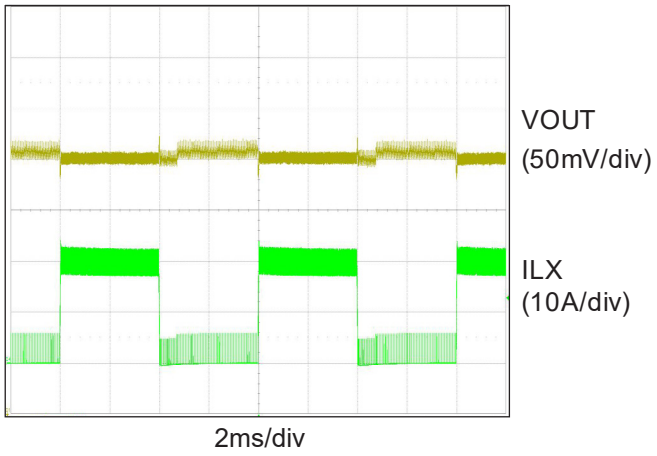
Typical Characteristics

T_A = 25°C, V_{IN} = 12V, V_{OUT} = 0.77V, fs = 600kHz, unless otherwise specified.

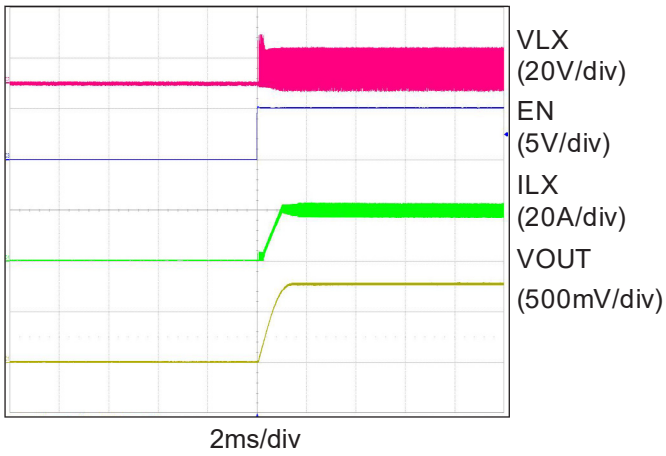
Normal Operation



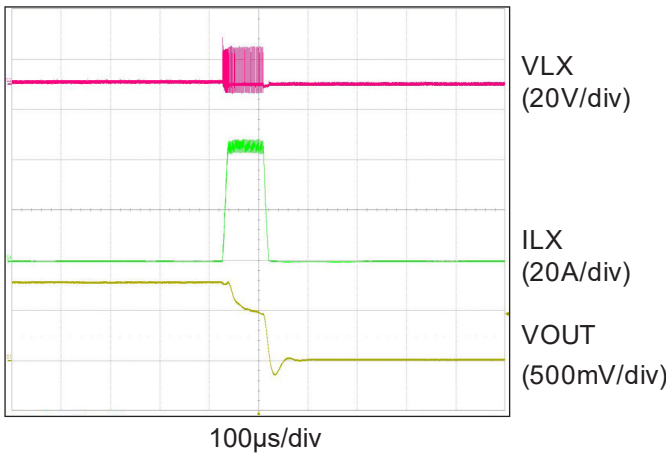
Load Transient 0A to 22A



Full Load Start-up



Short Circuit Protection



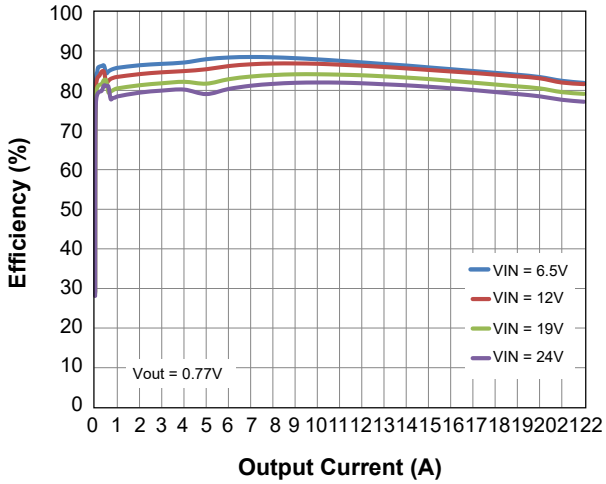


Figure 2. Efficiency vs. Load Current

Detailed Description

The AOZ23567QI is a high-efficiency, easy-to-use, synchronous buck regulator. The regulator is capable of supplying 22A of continuous output current with an output voltage adjustable down to 0.6V. The programmable on-time from 70ns to 3.5µs enables optimizing the configuration for PCB area and efficiency.

The input voltage of AOZ23567QI can be as low as 4.5V. The highest input voltage of AOZ23567QI can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with the ceramics output capacitor. The switching frequency can be externally programmed. Protection features include V_{CC} under-voltage lockout, current limit, output over-voltage and under-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ23567QI is available in a 36-pin 5mm×5mm QFN package.

Enable and Soft-start

The AOZ23567QI has external soft-start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft-start process begins when V_{CC} rises to 4.5V and voltage on EN pin is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of the soft-start pin (V_{SS}) when it is lower than 0.6V. When V_{SS} is higher than 0.6V, the FB voltage is regulated by internal precise band-gap voltage (0.6V). When V_{SS} is higher than 3.3V, the PGOOD signal is high. The soft-start time for PGOOD can be calculated by the following formula:

$$T_{ss}(\mu s) = 330 * C_{ss}(nF) \quad (1)$$

If C_{SS} is 1nF, the soft-start time will be 330µ seconds; if C_{SS} is 10nF, the soft-start time will be 3.3m seconds.

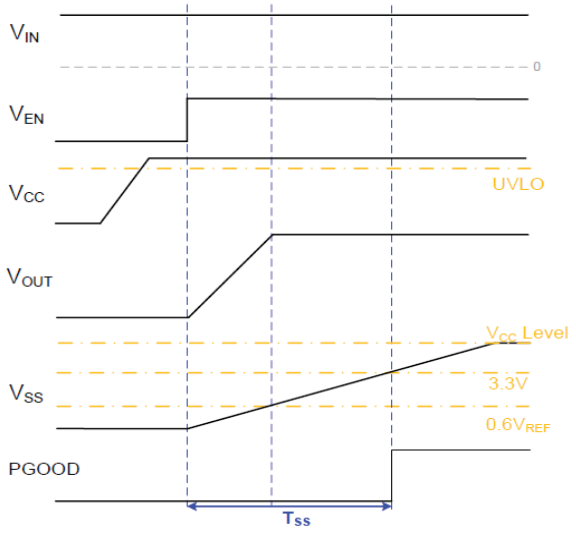


Figure 3. Soft-start Sequence of AOZ23567QI

Enable-off Discharge Resistor

AOZ23567QI has an enable-off discharge resistor function that allows the output voltage to quickly discharge to zero voltage when enabled turn-off. When VCC remains at 5V and the EN pin voltage is low, the discharge resistor loop is opened and the output voltage discharges the internal discharge resistor.

Constant-on-time PWM Control with Input Feed-forward

The control algorithm of AOZ23567QI is constant-on-time PWM control with input feed-forward. The simplified control schematic is shown in Figure 4. The high-side switch on-time is determined solely by a one-shot whose pulse width can be programmed by one external resistor and is inversely proportional to input voltage (IN). The one-shot is triggered when the internal 0.6V is higher than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed lower-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on-time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on-time control schemes.

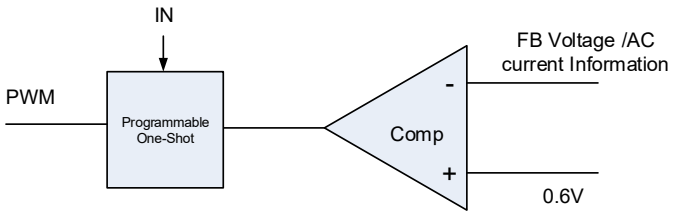


Figure 4. Simplified Control Schematic of AOZ23567QI

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of AOZ23567QI sets the on-time of the high-side switch inversely proportional to the IN.

$$T_{ON} \propto \frac{R_{TON}(k\Omega)}{V_{IN}(V)} \quad (2)$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (3)$$

Once the product of Vin*Ton is constant, the switching frequency keeps constant and is independent of input voltage.

An external resistor between the IN and TON pins sets the switching on-time according to the following equation:

$$T_{ON}(ns) = \frac{R_{TON}(k\Omega)}{V_{IN}(V)} \times 25 \quad (4)$$

Then, the switching frequency can be estimated by:

$$F_{SW}(kHz) = \frac{V_{OUT}(V)}{V_{IN}(V) * T_{ON}(ns)} \times 10^6 = \frac{V_{OUT}}{R_{TON}(k\Omega)} \times 4 \times 10^4 \quad (5)$$

If V_{OUT} is 0.77V, and set F_{SW} = 600kHz. According to the above equation, we can find out R_{TON} is 51kΩ. Notice that the frequency would be slightly increased due to the voltage dropping at the resistance of power trace.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

True Current Mode Control

AOS's COT control scheme uses a patented current-injection technique to provide stable performance using all-ceramic output capacitors. The constant-on-time control scheme is intrinsically unstable if the output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The AOZ23567QI senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Current Limit Setting

The AOZ23567QI has the current limit function by using R_{dson} of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off (350ns typical) is implemented after a constant-on-time. If the current exceeds the current limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 64 switching cycles, the AOZ23567QI considers this is a true failed condition and thus turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ23567QI again.

The current limit threshold mentioned in last paragraph can be set by connecting a resistor between ILIM pin and ground. The value of the current limit resistor (R_{ILIM}) can be calculated according to the equation below. A capacitor from ILIM pin to ground would impact the current limit accuracy and is not allowed.

$$I_{L\_LIMIT}(A) = 1.25 * R_{ILIM}(k\Omega) \quad (6)$$

As shown in Figure 5, once the magnitude of switch node voltage V_{LX} is larger than V_{ILIM}, over current signal is triggered. The larger R_{ILIM} is, the higher over current threshold will be. Section Current Limit Protection describes the action when over current condition happens.

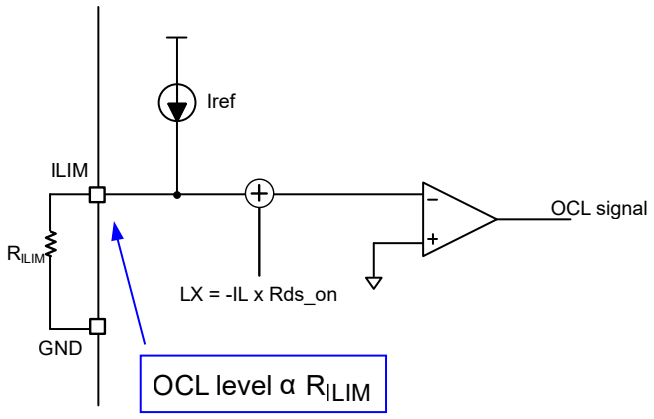


Figure 5. Illustration of Current Limit Setting

The value of current limit resistor (R_{ILIM}) must be higher than 15kΩ. The current limit calculation formula is not guaranteed if the resistor is lower than 15kΩ.

Output Voltage Under-voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, AOZ23567QI will turn off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ23567QI again.

Output Voltage Over-voltage Protection

The threshold of OVP is set 20% higher than 0.6V. When the VFB voltage exceeds the OVP threshold, high-side MOSFET is turn-off and low-side MOSFETs is turn-on 1μs, then latch-off.

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 15% below than the nominal regulation voltage for, the PGOOD is pulled low. When the output voltage is 20% higher than the nominal regulation voltage, the PGOOD is also pull low.

When combined with the under-voltage protection circuit, this current limit method is effective in almost every circumstance.

Application Information

The basic AOZ23567QI application circuit is shown in the previous page. The component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ23567QI to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7μF, should be connected to the V_{CC} pin and AGND pin for stable operation of the AOZ23567QI. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}} \quad (7)$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (8)$$

if let *m* equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m \quad (9)$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure. 6. It can be seen that when V_{OUT} is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_{OUT}$.

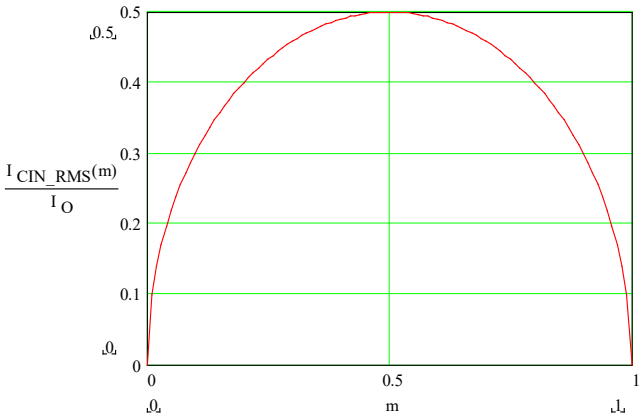


Figure 6. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic

capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2} \quad (11)$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR_{C_o} + \frac{1}{8 \times f \times C_o}\right) \quad (12)$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times f \times C_o} \quad (13)$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{C_o} \quad (14)$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}} \quad (15)$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Thermal Management and Layout Consideration

In the AOZ23567QI buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ23567QI.

In the AOZ23567QI buck regulator circuit, the major power dissipating components are the AOZ23567QI and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} \quad (16)$$

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{inductor\_loss} = I_{OUT}^2 \times R_{inductor} \times 1.1 \quad (17)$$

The actual junction temperature can be calculated with power dissipation in the AOZ23567QI and thermal impedance from junction to ambient.

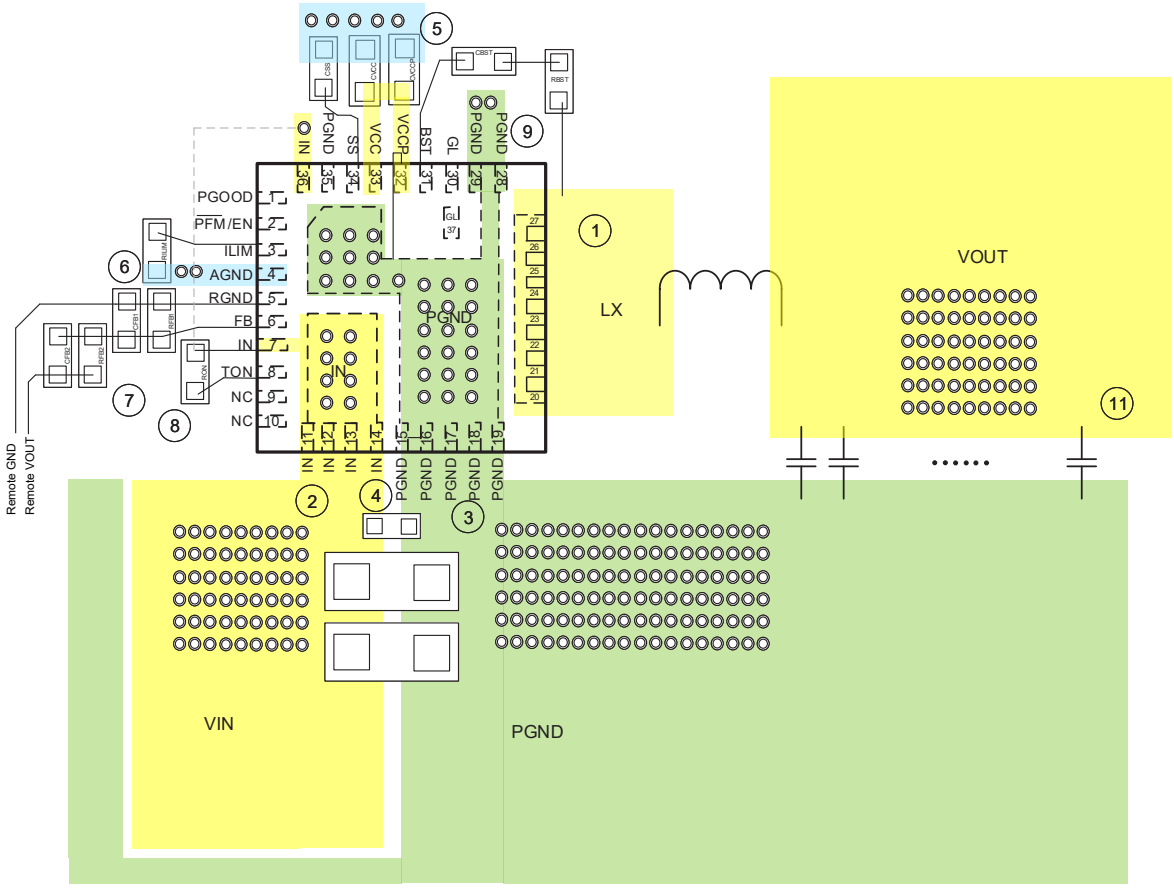
$$T_{junction} = (P_{total\_loss} - P_{total\_loss}) \times \theta_{JA} + T_A \quad (18)$$

The maximum junction temperature of AOZ23567QI is 150ºC, which limits the maximum load current capability. The thermal performance of the AOZ23567QI is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

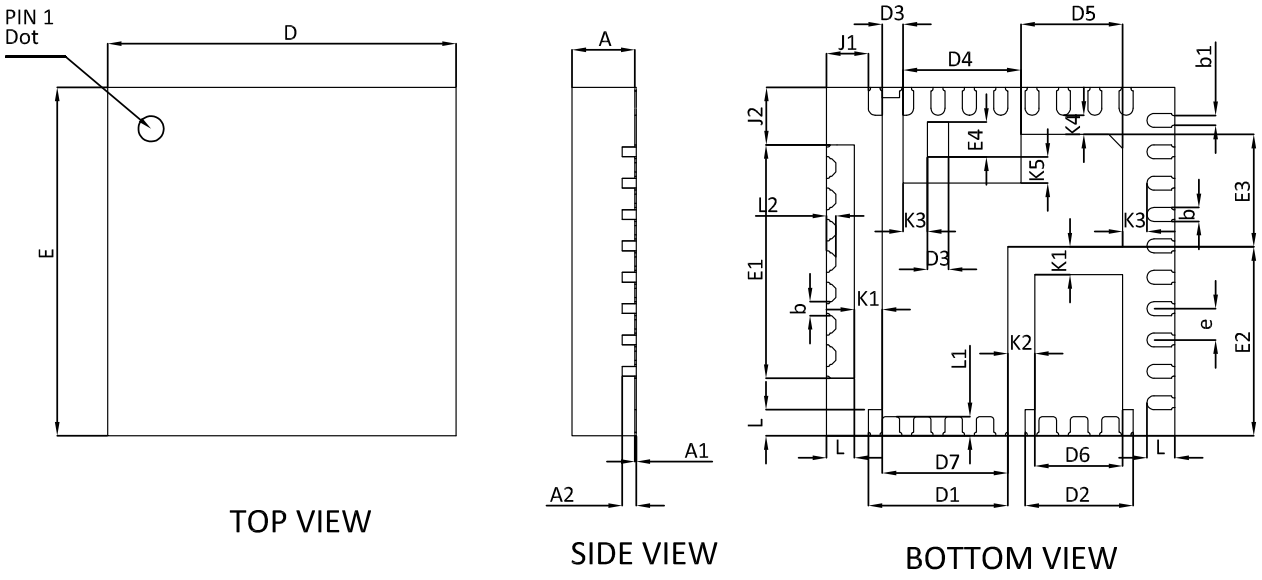
Layout Considerations

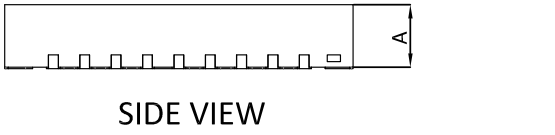
Several layout tips are listed below for the best electric and thermal performance.

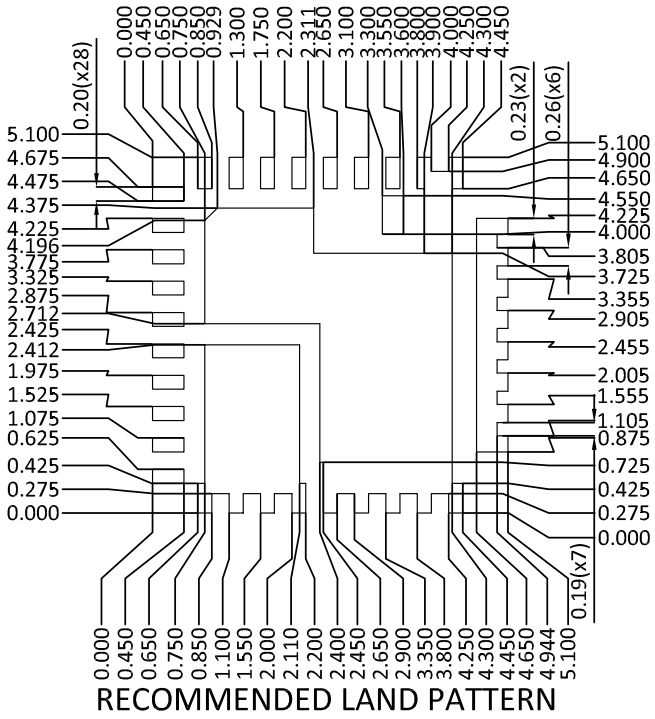
1. The LX pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a copper plane to LX pin to help thermal dissipation. The inductor needs to be placed as close to LX pin as possible.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
3. Connect a large PGND copper plane to PGND pin. Thick and short PGND trace could keep power path impedance low.
4. Input decoupling capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
5. Decoupling capacitor C_{VCC} should be connected to V_{CC} and GND as close as possible. Connect this GND to GND layer with vias as shown in below figure. Place C_{VCC} on the same layer with IC.
6. Connect AGND to GND layer with vias right close to AGND pin as shown in below figure.
7. Voltage divider R1 and R2 should be placed as closes possible to FB and RGND. Place R1 and R2 on the same layer with IC.
8. RTON should be connected as close as possible to Pin 7 (TON pin). Place RTON on the same layer with IC.
9. A ground plane is preferred; Pin 28, 29 (PGND) must be connected to the ground plane through vias as shown in figure below.
10. Sensitive signal traces such as feedback trace must be shielded from all noise sources, especially the LX node.
11. The feedback trace should be taken directly from output capacitor pad and use thin trace. FB trace goes through the other layer and shielded by GND layer is acceptable.
12. No signal should run on nearby layer under the Lx trace or under the inductor.
13. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
14. Insert at least two inner layers (or planes) connected to the power ground, in order to shield and isolate the small signal traces from noisy power lines.



Package Dimensions, QFN5x5-36L





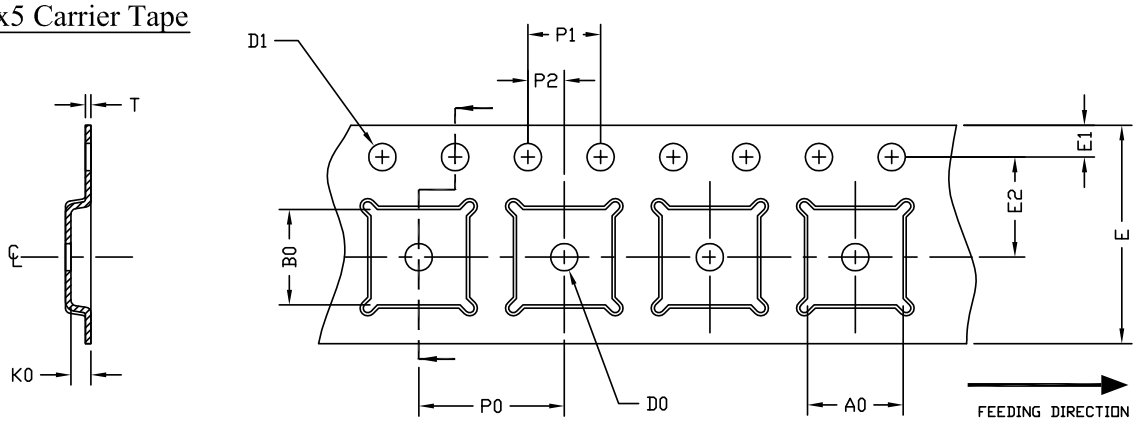


SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	---	0.002
A2		0.20 REF			0.008 REF	
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.95	2.00	2.05	0.077	0.079	0.081
D2	1.50	1.55	1.60	0.059	0.061	0.063
D3	0.25	0.30	0.35	0.010	0.012	0.014
D4	1.64	1.69	1.74	0.065	0.067	0.069
D5	1.41	1.46	1.51	0.056	0.057	0.059
D6	1.21	1.26	1.31	0.048	0.050	0.052
D7	1.75	1.80	1.85	0.069	0.071	0.073
E	4.95	5.00	5.05	0.195	0.197	0.199
E1	3.25	3.35	3.45	0.128	0.132	0.136
E2	2.61	2.71	2.81	0.103	0.107	0.111
E3	1.51	1.61	1.71	0.059	0.063	0.067
E4	0.40	0.50	0.60	0.016	0.020	0.024
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.23	0.28	0.33	0.009	0.011	0.013
L2	0.09	0.14	0.19	0.004	0.006	0.007
J1	0.55	0.60	0.65	0.022	0.024	0.026
J2	0.78	0.83	0.88	0.031	0.033	0.035
K1	0.35	0.40	0.45	0.014	0.016	0.018
K2	0.34	0.39	0.44	0.013	0.015	0.017
K3	0.30	0.35	0.40	0.012	0.014	0.016
K4	0.23	0.28	0.33	0.009	0.011	0.013
K5	0.33	0.38	0.43	0.013	0.015	0.017
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.09	0.14	0.19	0.004	0.006	0.007
e		0.45 BSC			0.018 BSC	

NOTE:
1. CONTROLLED DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS IN INCHES ARE CONVERTED AS REFERENCE ONLY.

Tape and Reel Dimensions, QFN5x5-36L

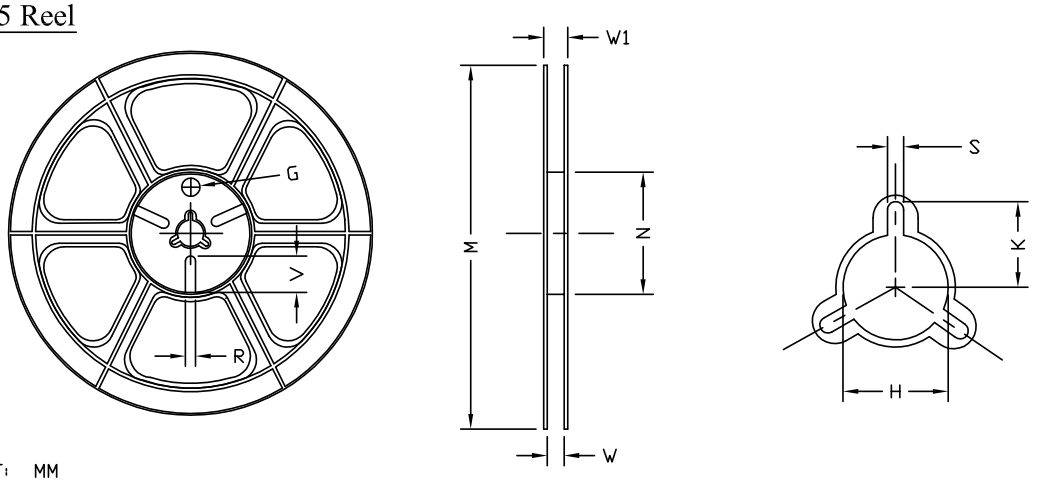
QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN5x5 Reel

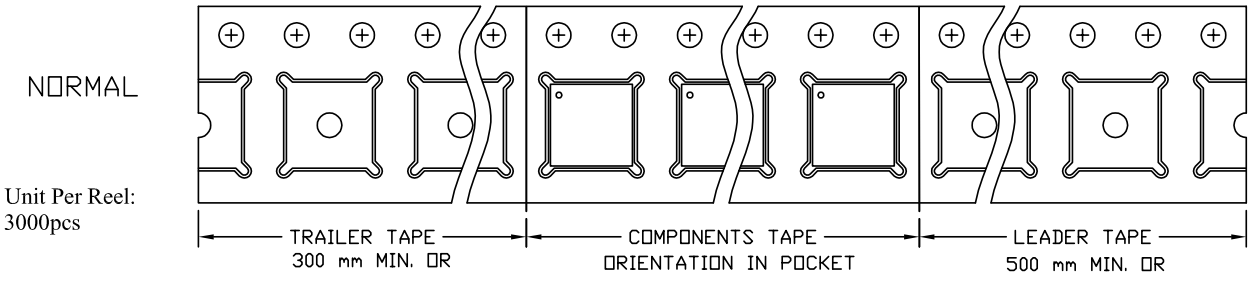


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø100.0 ±1.0	12.4 $^{+2.0}_{-0.0}$	17.0 $^{+2.6}_{-1.2}$	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

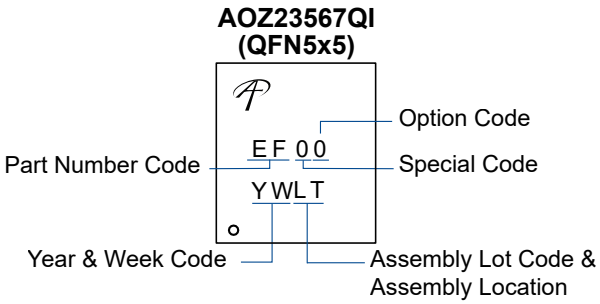
QFN5x5 Tape

Leader / Trailer & Orientation



Unit Per Reel: 3000pcs

Part Marking



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