AOZ32101ADV

100V, 2.5A Half-bridge Gate Driver

General Description

The AOZ32101ADV is a 100V half-bridge gate driver, used to drive high side and low side N-channel MOSFETs, with sufficient drive capability and fast rise/fall times to operate at high frequencies or multiple MOSFETs in parallel. Integrated bootstrap diode, saving external components. With shoot-through protection to protect the MOSFET from damage.

Under voltage lock-out protection pulls the high/low side output low when the supply voltage is insufficient.

The AOZ32101ADV is available in a 3mm x 3mm DFN-10L package and is rated over a -40°C to +125°C ambient temperature range.

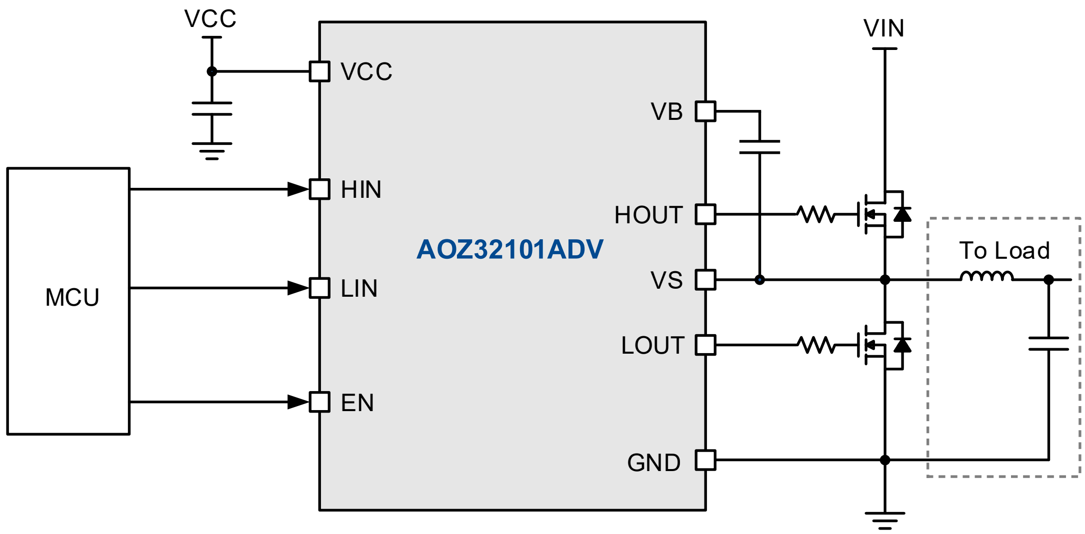
Features

- Drives half-bridge, dual N-channel MOSFET
- 110V bootstrap voltage range
- Input signal overlap protection
- Integrated bootstrap diode
- Typical 20ns propagation delay time
- Less than 5ns gate drive mismatch
- Less than 150μA quiescent current
- Less than 5μA shutdown current
- UVLO for both high side and low side
- DFN 3mm x 3mm 10 pin packages

Applications

- Three-phase, brushless, DC motors
- Permanent magnet synchronous motors
- Power tools
- E-bikes
- DC-DC converters
- Switch power supplies

Typical Application



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32101ADV	-40 °C to +125 °C	DFN3x3-10L	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

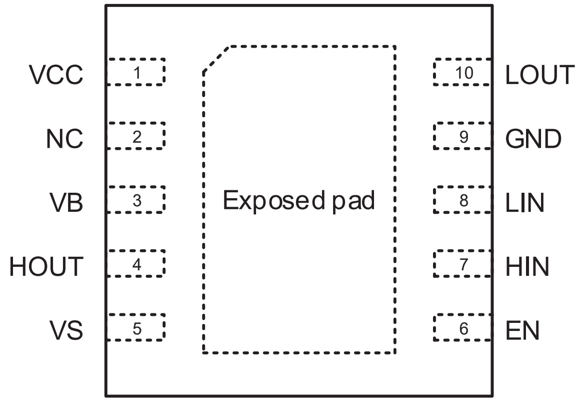


Figure 1. DFN3x3-10L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Gate driver power supply input.
2	NC	No connection.
3	VB	Bootstrap capacitor connection. Connect a ceramic capacitor between VB and VS for supplying high side MOSFET.
4	HOUT	High side gate driver output.
5	VS	High side source connection. Connect to source of high side power MOSFET.
6	EN	Enable / Disable control.
7	HIN	Signal input for the high side driver.
8	LIN	Signal input for the low side driver.
9	GND	Ground.
10	LOUT	Low side gate driver output.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VCC)	-0.3V to 20V
SW Voltage (VS)	-5V to 105V
Bootstrap Voltage (VB)	-0.3V to 110V
VB to VS	-0.3V to 18V
HOUT	-0.3V to (VB - VS) +0.3V
LOUT to GND	-0.3V to (VCC +0.3V)
All Other Pins	-0.3V to 20V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to + 150°C
ESD Rating	2KV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VCC)	+5.5V to 18V
SW Voltage (VS)	-1.0V to 100V
Voltage slew rate (VS)	50V/ns
Ambient Temperature (TA)	-40°C to +125°C
Package Thermal Resistance Θ_{JA} Θ_{JC}	 40 °C/W 0.6 °C/W

Electrical Characteristics

V_{CC} = VB - VS = 12V, V_{GND} = VS = 0V, V_{EN} = 5V, No load at HOUT and LOUT, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current						
I_{SHDN}	VCC shutdown current	V_{EN} = 0		1.6		µA
I_{VCC_Q}	VCC quiescent current	HIN = LIN = 0		80	150	µA
I_{VCC_O}	VCC operating current	fsw = 500kHz		1	1.5	mA
I_{VB_Q}	Floating driver quiescent current	HIN = LIN = 0		70	120	µA
I_{VB_O}	Floating driver operating current	fsw = 500kHz		1.5	2	mA
I_{LK}	Leakage current	VB = VS = 110V		2	5	µA
Inputs						
V_{IN_H}	Input logic high voltage threshold		2.3			V
V_{IN_L}	Input logic low voltage threshold				1	V
V_{IN_HYS}	Input voltage hysteresis			0.7		V
R_{IN}	Internal pull-down resistance			285		kΩ
Enable						
V_{EN_H}	EN pin input logic high voltage threshold to enable the driver			1.5		V
V_{EN_L}	EN pin input logic low voltage threshold to disable the driver			1.2		V
V_{EN_HYS}	EN pin input Hysteresis			300		mV
I_{EN}	EN Input Current	V_{EN} = 2V		10		µA
		V_{EN} = 5V		20		µA
R_{EN}	EN pin internal pull-down resistance			285		kΩ

Electrical Characteristics *(Continued)*

V_{CC} = VB - VS = 12V, V_{GND} = VS = 0V, V_{EN} = 5V, No load at HOUT and LOUT, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Under Voltage Protection						
V_{CC_R}	VCC rising threshold		4.8	5	5.2	V
V_{CC_F}	VCC falling threshold		4.3	4.5	4.8	V
V_{CC_HYS}	VCC threshold hysteresis			0.5		V
V_{B_R}	(VB-VS) rising threshold		3.4	3.7	4.1	V
V_{B_F}	(VB-VS) falling threshold		3.1	3.4	3.8	V
V_{B_HYS}	(VB-VS) threshold hysteresis			0.4		V
Bootstrap Diode						
V_{F1}	Bootstrap diode VF @ 100µA			0.16		V
V_{F2}	Bootstrap diode VF @ 100mA			0.5		V
R_D	Bootstrap diode dynamic resistance	@ 100mA		1.8		Ω
Low Side Gate Driver						
V_{LOUT_L}	Low level output voltage	I_{LOUT} = 100mA		64		mV
V_{LOUT_H}	High level output voltage	I_{LOUT} = -100mA, V_{LOUT_H} = V_{CC} - V_{LOUT}		65		mV
I_{LOUT_SOURCE} (1)	Peak pull-up current	V_{LOUT} = 0V, V_{CC} = 12V		2.85		A
I_{LOUT_SINK} (1)	Peak pull-down current	V_{LOUT} = V_{CC} = 12V		3.9		A
High Side Gate Driver						
V_{HOUT_L}	Low level output voltage	I_{HOUT} = 100mA		170		mV
V_{HOUT_H}	High level output voltage	I_{HOUT} = -100mA, V_{HOUT_H} = V_B – V_{HOUT}		160		mV
I_{HOUT_SOURCE} (1)	Peak pull-up current	V_{HOUT} = 0V, V_{CC} = 12V		2.6		A
I_{HOUT_SINK} (1)	Peak pull-down current	V_{HOUT} = V_{CC} = 12V		3.7		A

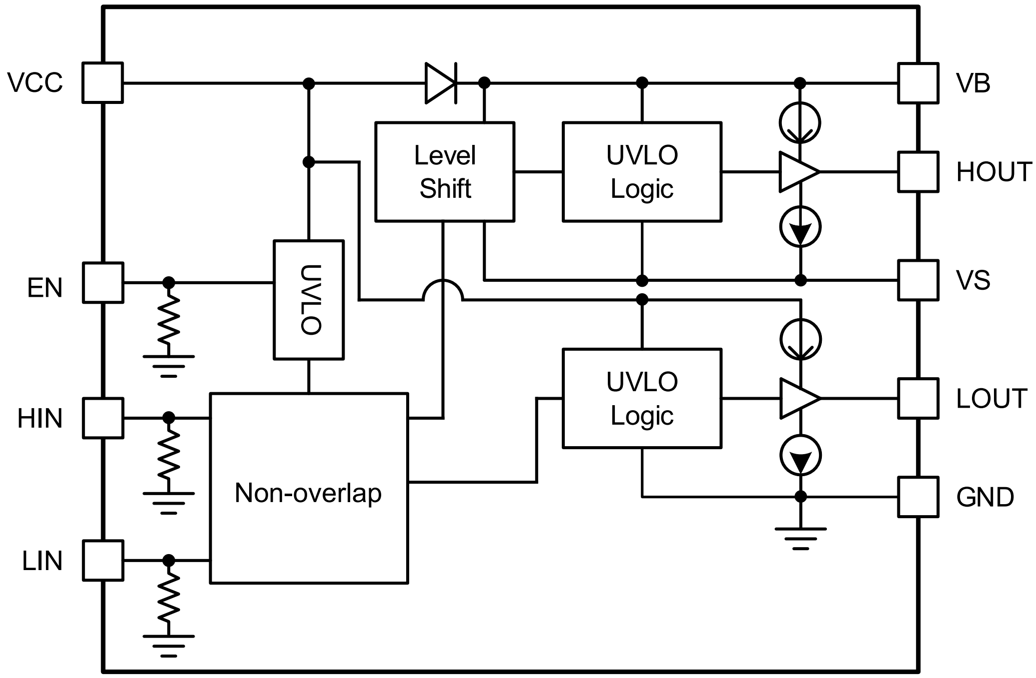
Electrical Characteristics *(Continued)*

V_{CC} = VB - VS = 12V, V_{GND} = VS = 0V, V_{EN} = 5V, No load at HOUT and LOUT, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Switching Characteristics						
Low Side Gate Driver						
t_{PDF_L}	Turn-off propagation delay LIN falling to LOUT falling			20		ns
t_{PDR_L}	Turn-on propagation delay LIN rising to LOUT rising			20		ns
t_{R_L}	LOUT rise time	C_L = 1nF		10		ns
t_{F_L}	LOUT fall time	C_L = 1nF		10		ns
High Side Gate Driver						
t_{PDF_H}	Turn-off propagation delay HIN falling to HOUT falling			20		ns
t_{PDR_H}	Turn-on propagation delay HIN rising to HOUT rising			18		ns
t_{R_H}	HOUT rise time	C_L = 1nF		10		ns
t_{F_H}	HOUT fall time	C_L = 1nF		10		ns
Matching						
T_{MOFF}	Form Lout turn-off to Hout turn-on			1		ns
T_{MON}	Form Hout turn-off to Lout turn-on			1		ns
T_{PW}	Minimum input pulse width that changes the output				40	ns

Note:
1. Guaranteed by design.

Functional Block Diagram



Timing Diagrams

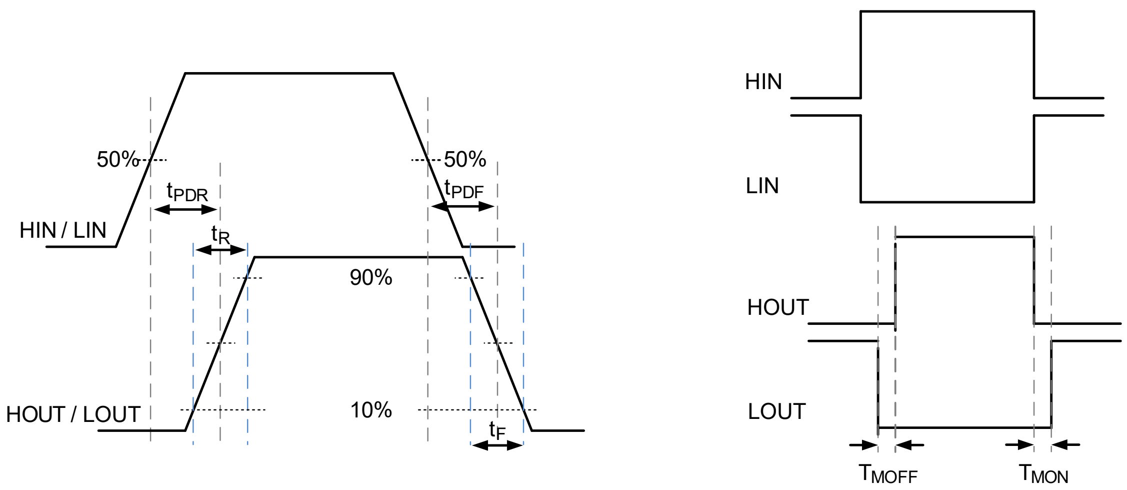
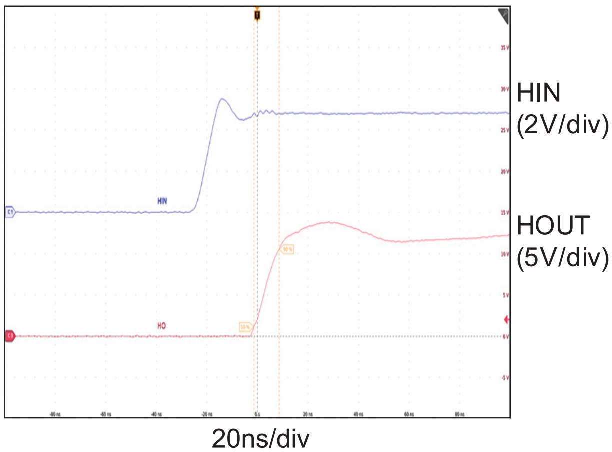


Figure 2. Timing Diagrams

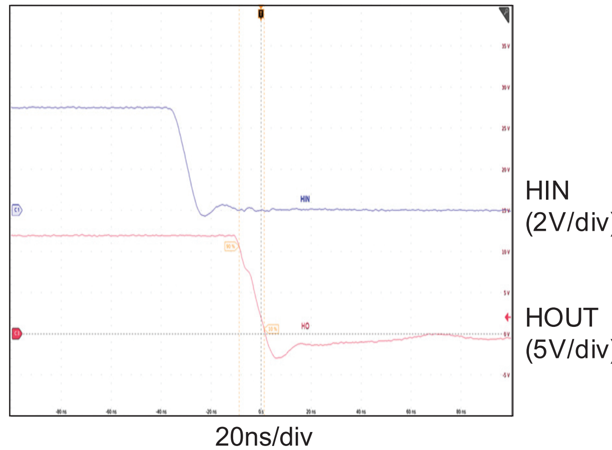
Typical Characteristics

VCC = VB - VS = 12V, V_{GND} = VS = 0V, V_{EN} = 5V, T_A = +25°C, unless otherwise specified.

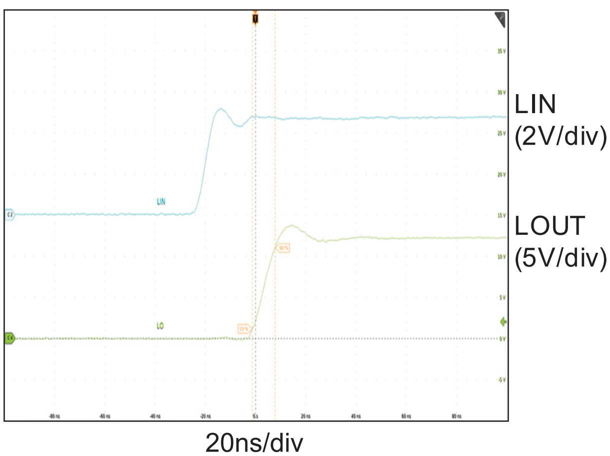
HOUT Rise Time = 10ns



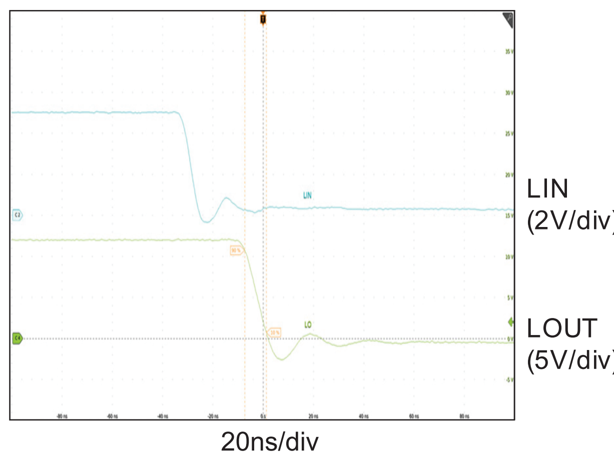
HOUT Fall Time = 10ns



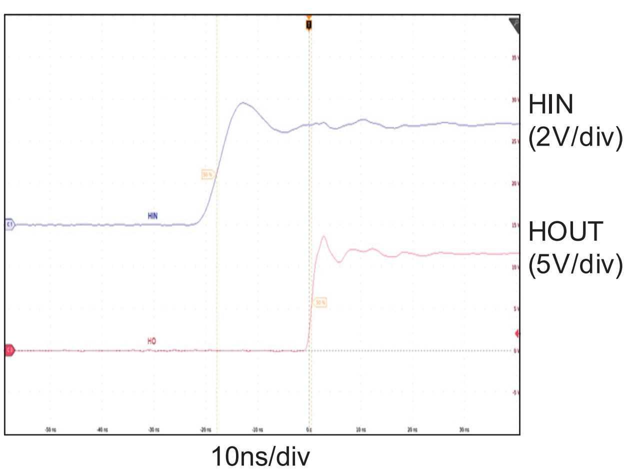
LOUT Rise Time = 9ns



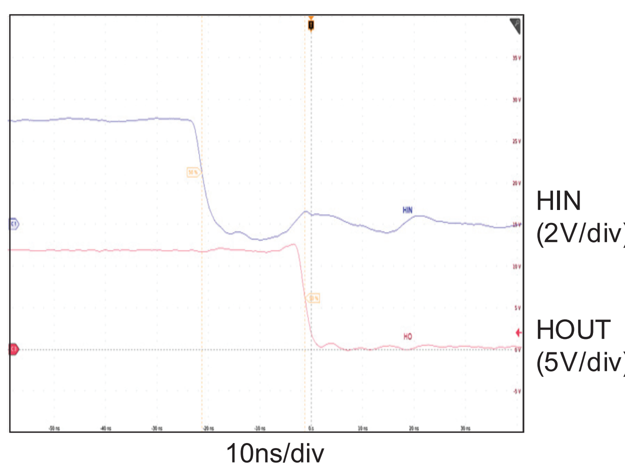
LOUT Fall Time = 8.63ns



High Side Turn-on Propagation Delay = 18.4ns



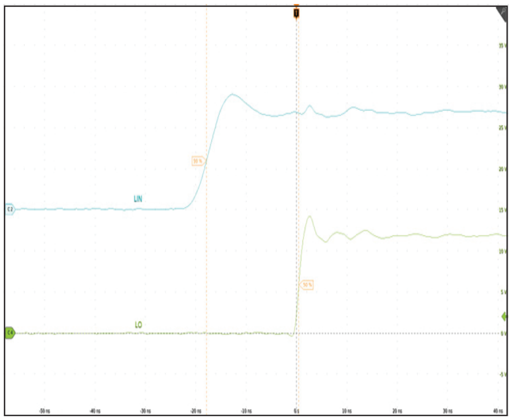
High Side Turn-off Propagation Delay = 20.05ns



Typical Characteristics *(Continued)*

VCC = VB - VS = 12V, V_{GND} = VS = 0V, V_{EN} = 5V, T_A = +25°C, unless otherwise specified.

Low Side Turn-on Propagation Delay = 18.36ns

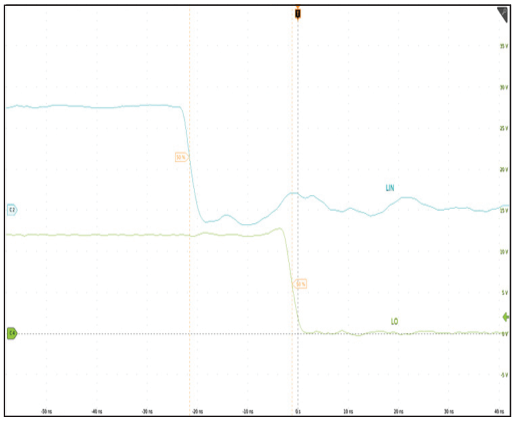


LIN
(2V/div)

LOUT
(5V/div)

10ns/div

Low Side Turn-off Propagation Delay = 20.41ns

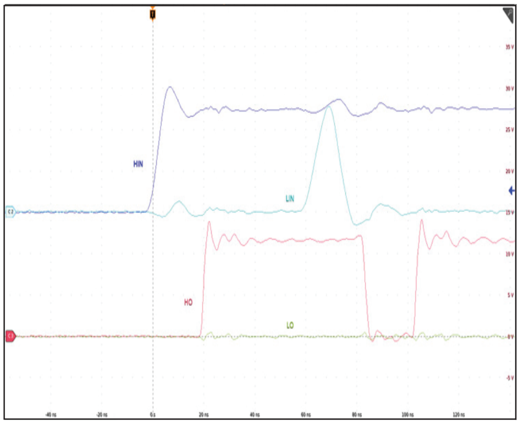


LIN
(2V/div)

LOUT
(5V/div)

10ns/div

Input Overlap Protection



HIN&LIN
(2V/div)

HOUT&LOUT
(5V/div)

20ns/div

Detailed Description

The AOZ32101ADV is a 100V half-bridge gate driver for driving high side and low side N-channel MOSFETs in synchronous buck or half-bridge configurations. The two outputs are independently controlled by two TTL compatible input signals.

They have sufficient drive capability and fast rise/fall times and can operate at high frequencies or with multiple MOSFETs in parallel. This component also integrates a 100V bootstrap diode device to charge the high side gate drive bootstrap capacitor and provide clean level translation from the control logic to the high side gate driver. Under voltage lockout (UVLO) is provided on both the low side and high side supply rails. The EN pin is provided to enable or disable driver settings. The driver also features an input interlock that shuts down both outputs when the two inputs overlap, protecting the MOSFETs from damage.

VCC Power Up and UVLO

In order to ensure the normal operation of the gate driver, if the EN pin is pulled high (normal working state), the gate driver will not work before V_{CC} is higher than the UVLO rising threshold (about 5V), until V_{CC} > 5V, the gate driver can work normally.

When V_{CC} drops to the UVLO falling threshold (about 4.5V), gate driver shunt down.

VB UVLO

The bootstrap capacitor voltage (V_B - V_S) is provided to the high side gate driver. The voltage (V_B - V_S) must be greater than rising threshold (about 3.7V), to make the high side gate driver start working. If it is less than falling threshold, there will be no output from the HOUT pin.

Enable Pin

The Enable (EN) pin is used to enable the gate driver. When the voltage of the EN pin is greater than the EN logic high voltage, the gate driver works normally. When the EN pin is floating or connected to ground, the gate driver does not work. The EN pin is internally connected to ground through a 285K pull-down resistor.

When the EN pin is not used, the EN pin can be connected to V_{CC} through an external pull-up resistor. The recommended resistor value is 10KΩ. In noise prone application, a small filter capacitor 1nF, should be connected from the EN pin to GND pin as close to the device as possible.

It is suggested to wait until the EN pin is enabled then applying an input signal.

Input Control Logic

When EN is pulled high, H_{OUT} and L_{OUT} follow their respective H_{IN} and L_{IN} signals through the gate driver to drive MOSFETs, and the internal circuit will also judge whether the H_{IN} and L_{IN} signals are high at the same time to avoid shoot-through of High/Low side MOSFETs. In a real system, the controller will have to take care of dead time adjustment. For synchronous buck topology switching for example, it requires careful selection of dead-time between the high side and low side switches to avoid cross conduction as well as excessive body diode conduction.

The truth table of the control logic is as follows:

Table 1. Control Logic Table

EN	HIN	LIN	HOUT	LOUT
L	L	L	L	L
	H	L	L	L
	L	H	L	L
	H	H	L	L
H	L	L	L	L
	H	L	H	L
	L	H	L	H
	H	H	L	L
H	Floating	L	L	L
	Floating	H	L	H
	L	Floating	L	L
	H	Floating	H	L
Floating	Floating	Floating	L	L

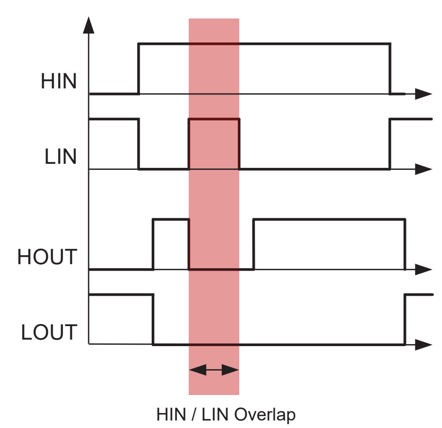


Figure 3. Input Overlap Protection

Application Information

Synchronous Buck Converter

The drivers can be used in half-bridge, full-bridge, synchronous boost, synchronous buck and active clamp topologies. For example, the following is a basic synchronous buck application circuit, as shown in Figure 4.

Operating at high frequencies, the bootstrap capacitor value is recommended to be a ceramic capacitor of 100nF with a good dielectric. The selection of MOSFETs depends on the load on the application system. The HIN and LIN input signal must be appropriately adjusted for dead-time, and the adjustment of R_g will also change the rise and fall times of MOSFETs.

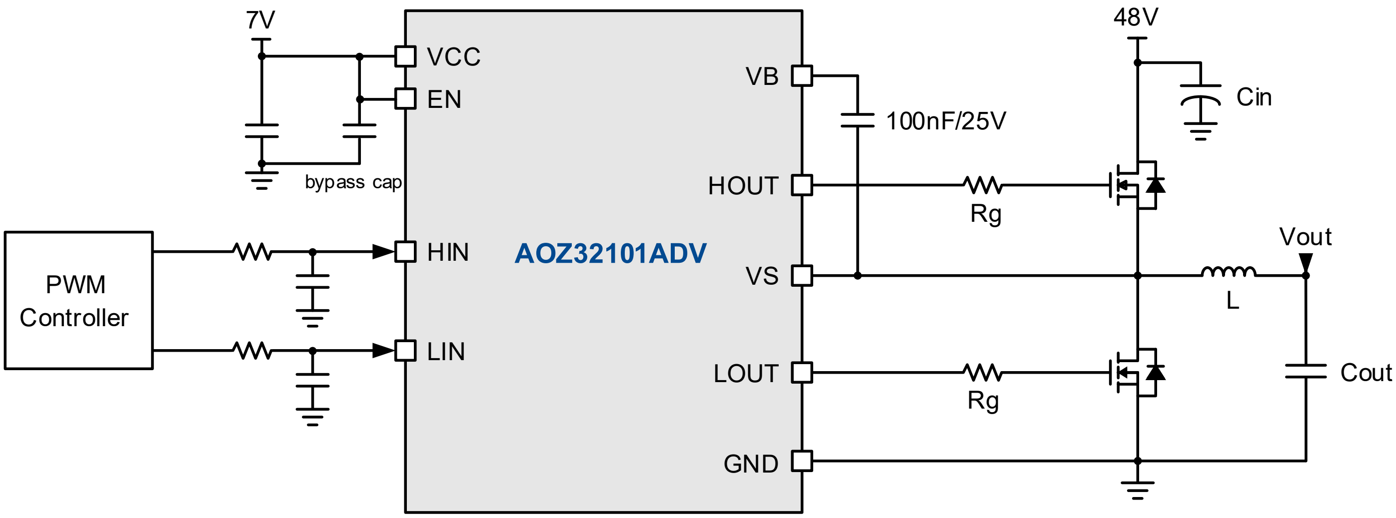


Figure 4. Synchronous Buck Reference Design Circuits

Half-bridge Motor Driver

In the high power half-bridge converter topology, a basic application circuit is shown in Figure 5.

Typically, a bootstrap capacitor must maintain the V_B - V_S voltage above the UVLO threshold to properly turn on the high side MOSFET. For the following reference circuit, when using high-power TOLL-MOSFETs, it is recommended that the bootstrap capacitor value be 2.2μF and ceramic capacitors with good dielectric properties be used. The value of the VCC bypass capacitor must be greater than the value of the bootstrap capacitor (generally 10 times the bootstrap capacitor value). If used in multiple parallel MOSFETs, the bootstrap capacitor value needs to be increased to provide sufficient total charge. Proper adjustment of R_g will also change the rise and fall time of MOSFET.

In addition, in motor system applications, high d_V/d_t and d_I/d_t in the circuit can cause negative voltages on different pins such as HOUT, LOUT, and VS, and the circuit may require additional protection components. In this case, a fast, low leakage Schottky diode should be used. This diode must be placed close to the gate driver component pin to effectively clamp excessive negative voltage on the pin.

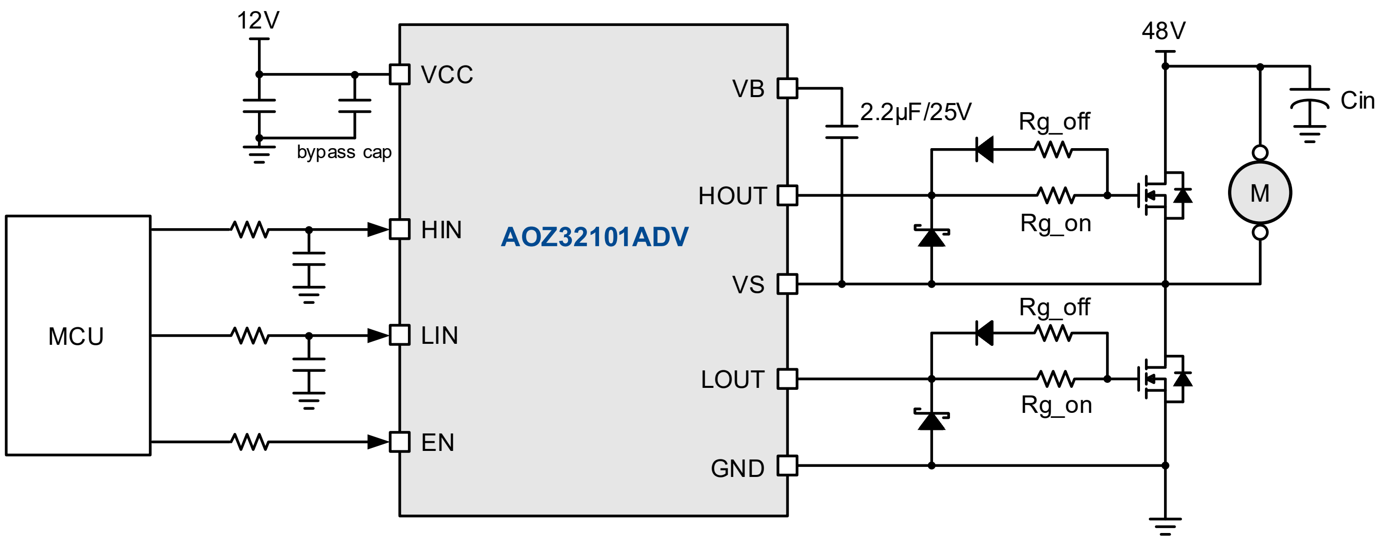


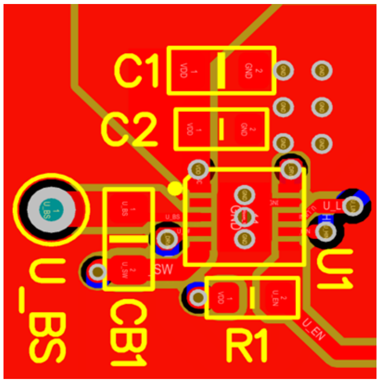
Figure 5. Half-bridge Motor Reference Design Circuits

Layout Guidelines

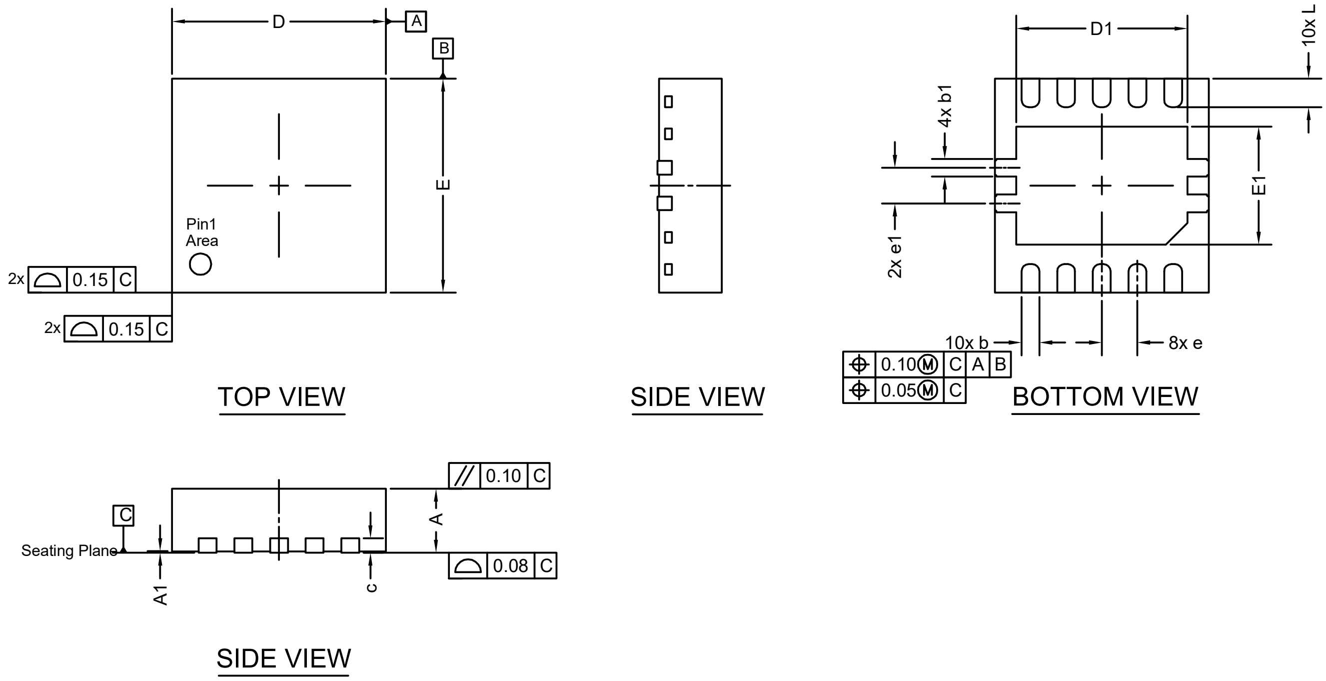
A good layout is very important for noise suppression and driver performance.

List the following five-point layout suggestions and refer to the figure below:

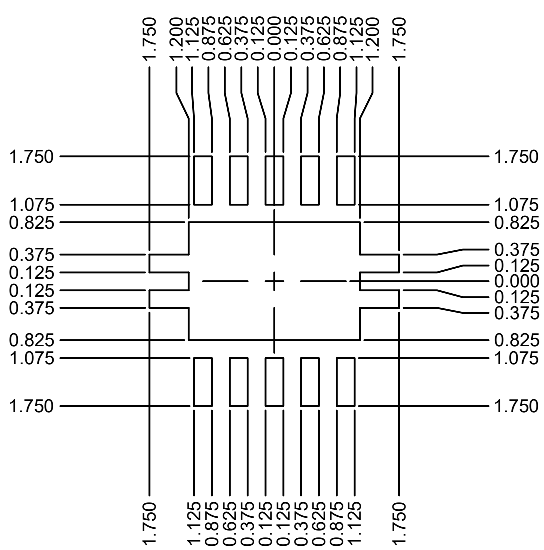
1. Ceramic capacitors should be connected as close to the VCC and GND pins as possible to reduce switching spikes.
2. Bootstrap capacitor needs to be close to the VB and VS pins, and the layout trace width is recommended to be more than 30mil.
3. During the conduction period, the HOUT and LOUT pins will draw high peak current from VCC to drive the external MOSFET gate. It is recommended that the width of the layout trace be more than 30mil.
4. The thermal pad should be connected to a large, heavy copper plane to improve the thermal performance of the device. Vias can also be added to the thermal pad to connect to a larger area of the device GND ground plane.
5. Placing the gate driver as close as possible to the MOSFET reduces loop inductance and noise issues at the MOSFET gate terminal.



Package Dimensions, DFN3x3-10L



RECOMMENDED LAND PATTERN



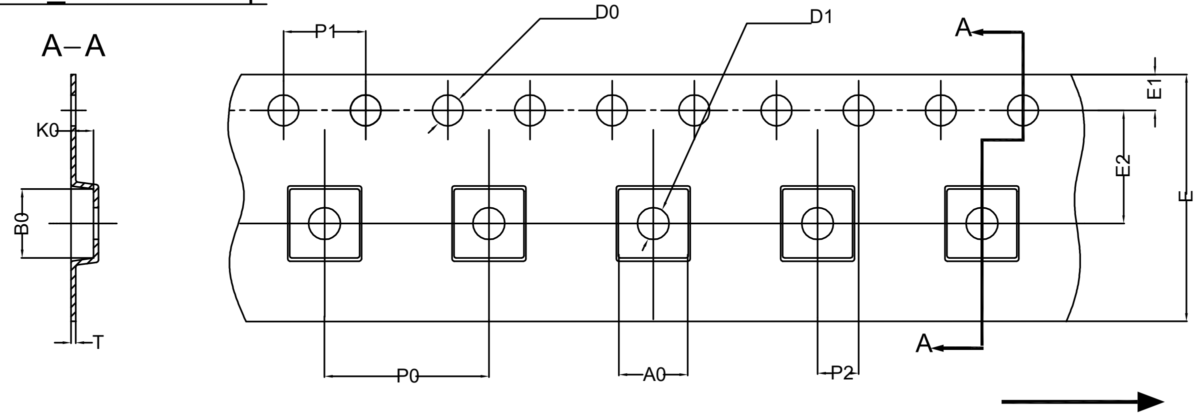
SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	-	0.05	0.000	-	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.25 REF			0.010 REF		
c	0.20 REF			0.008 REF		
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	1.55	1.65	1.75	0.061	0.065	0.069
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.30	2.40	2.50	0.091	0.094	0.098
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 BSC			0.020 BSC		
e1	0.50 BSC			0.020 BSC		

UNIT: mm

NOTE:
1. DIMENSIONING AND TOLERANCING COMPLY WITH ASME Y14.5M 1994.
2. CONTROLLED DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD(S) AND ALL TERMINAL LEADS HAVING METALIZATION.

Tape and Reel Dimensions, DFN3x3-10L

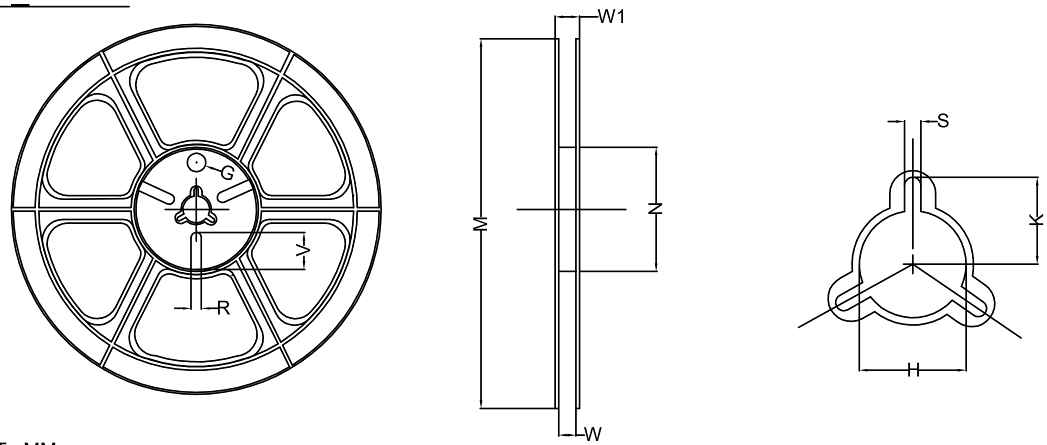
DFN3x3_EPCarrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3x3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 -0	1.50 +0.10 -0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

DFN3x3_EP Reel

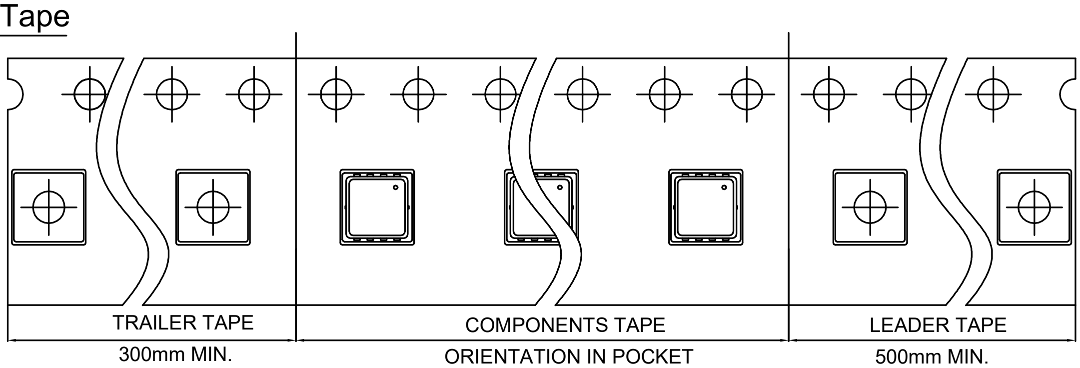


UNIT: MM

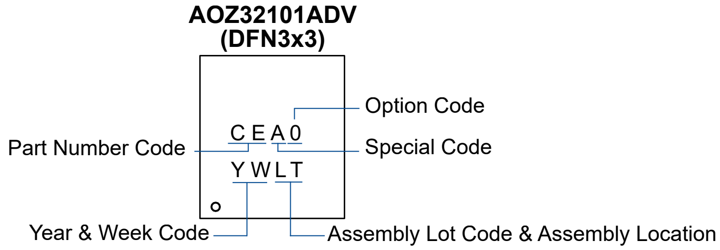
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.00 ±0.50	Ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	Ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	---	---	---

DFN3x3 EP Tape

PIC Normal
Unit Per Reel: 5000pcs



Part Marking



Part Number	Description	Code
AOZ32101ADV	Green Product	CEA0

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.