

General Description

AOZ5018QI-C is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra-low ON resistance to minimize conduction loss.

AOZ5018QI-C uses a PWM input for accurate control of the power MOSFETs switching activities, is compatible with 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5018QI-C a highly versatile power module. The bootstrap diode is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low parasitics, keeping their effects to a minimum.

Features

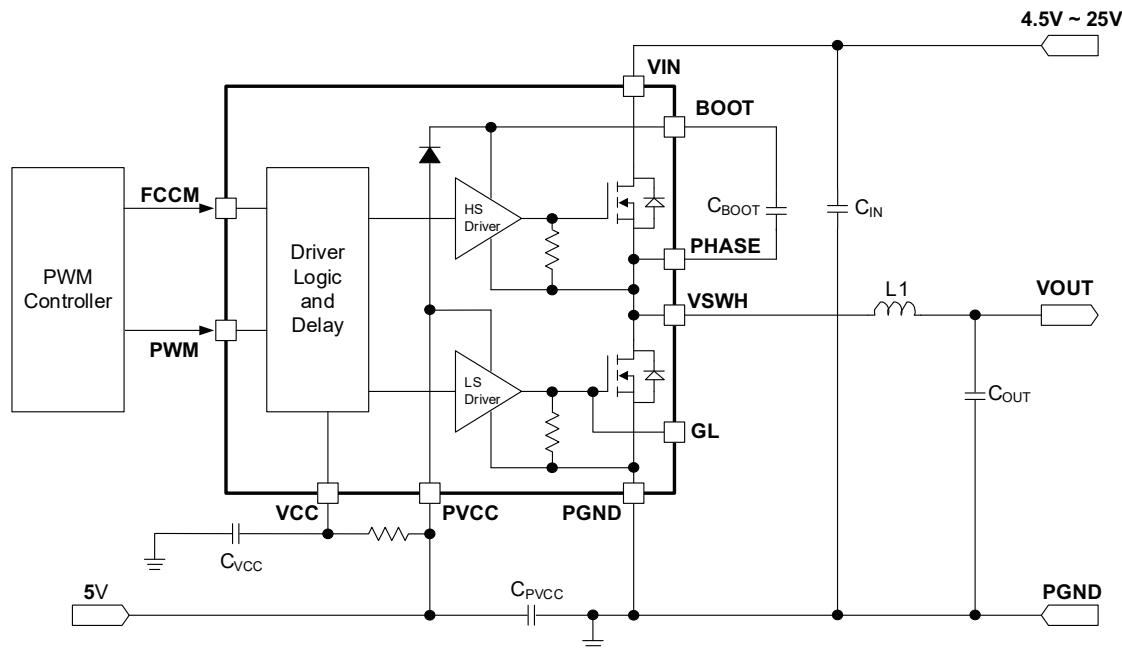
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- 65A continuous output current
 - Up to 80A with 10ms on pulse
 - Up to 120A with 10us on pulse
- Up to 2MHz switching operation
- 5V PWM and Tri-State input compatible
- Under-Voltage LockOut protection
- FCCM control for Diode Emulation / CCM operation
- Standard 5mm x 5mm QFN-31L package

Applications

- Memory and graphic cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming consoles



Typical Application Circuit



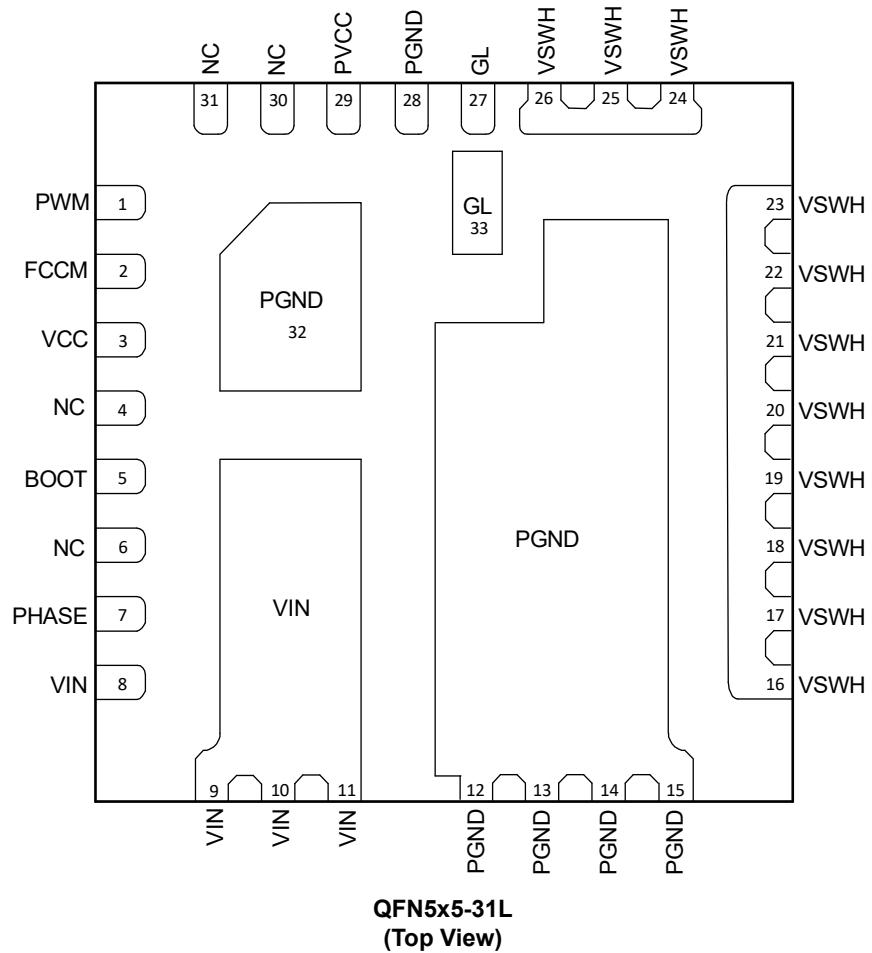
Ordering Information

Part Number	Junction Temperature Range	Package	Environmental
AOZ5018QI-C	-40°C to +150°C	QFN5x5-31L	RoHS



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
 Please visit <https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf> for additional information.

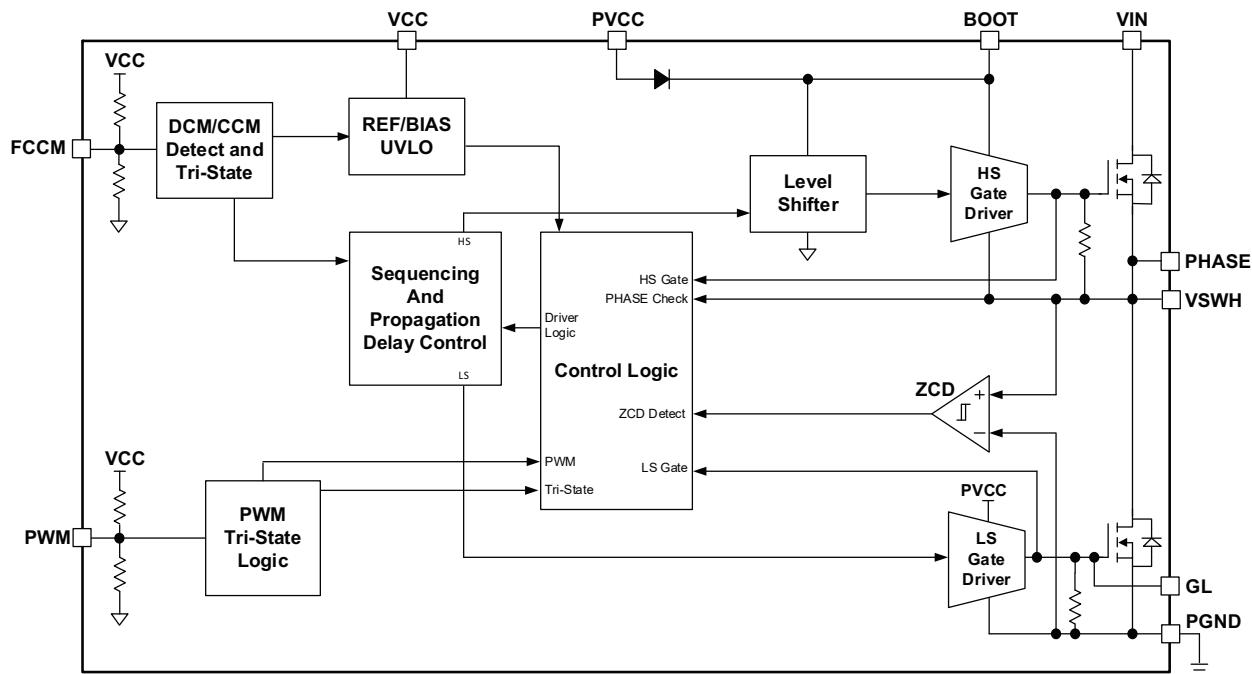
Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic level.
2	FCCM	Continuous conduction mode of operation is allowed when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. High impedance on the input of FCCM will shutdown both high side and low side MOSFETs.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1 μ F MLCC directly between VCC and PGND (Pin 28).
4	NC	Internally connected to PGND paddle. It can be left floating (No Connect) or tied to PGND.
5	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5).
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27, 33	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
28, 32	PGND	Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1 μ F directly between PGND and PVCC (Pin 29).
29	PVCC	5V Power Rail for High-Side and Low-Side MOSFET Drivers. Ensure to position a 1 μ F MLCC directly between PVCC and PGND (Pin 28).
30, 31	NC	No Connect

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, FCCM)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 33V
Bootstrap Voltage Transient ⁽¹⁾ (BOOT-PGND)	-8V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 7V
BOOT Voltage Transient ⁽¹⁾ (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient ⁽¹⁾ (PHASE/VSWH)	-8V to 38V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low-Side Gate Voltage Transient ⁽²⁾ (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	65A
VSWH Current 10ms Pulse	80A
VSWH Current 10us Pulse	120A
Storage Temperature (T _S)	-65°C to 150°C
Max Junction Temperature (T _J)	150°C
ESD Rating ⁽³⁾	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5Ω in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5V to 25V
Low Voltage / MOSFET Driver Supply (VCC, PVCC)	4.5V to 5.5V
Control Inputs (PWM, FCCM)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics⁽⁴⁾

$T_J = 0^\circ\text{C}$ to 150°C , $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $P_{VCC} = V_{CC} = 5\text{V}$, unless otherwise specified. Min/Max values are guaranteed by test, design or statistical correlation.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GENERAL						
V_{IN}	Power Stage Power Supply		4.5		25	V
V_{CC}	Low Voltage Bias Supply	$P_{VCC} = V_{CC} = 5\text{V}$	4.5		5.5	V
$R_{\theta JC}^{(5)}$	Thermal Resistance	PCB Temp = 100°C		2.5		$^\circ\text{C} / \text{W}$
$R_{\theta JA}^{(5)}$				12.5		$^\circ\text{C} / \text{W}$
INPUT SUPPLY AND UVLO						
V_{CC_UVLO}	Undervoltage LockOut	VCC Rising		3.4	3.9	V
V_{CC_HYST}		VCC Hysteresis		500		mV
I_{VCC}	Control Circuit Bias Current	FCCM = Floating, PWM = Floating		3	5	μA
		FCCM = 5V, PWM = Floating		80		
		FCCM = 0V, PWM = Floating		120		
PWM INPUT						
V_{PWM_H}	PWM Logic High Input Voltage		4.2			V
V_{PWM_L}	PWM Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-250		μA
I_{PWM_SNK}		PWM = 5V		250		μA
V_{TRI}	PWM Tri-State Window		1.6		3.4	V
FCCM INPUT						
V_{FCCM_H}	FCCM Logic High Input Voltage		3.9			V
V_{FCCM_L}	FCCM Logic Low Input Voltage				1.1	V
I_{FCCM}	FCCM Pin Input Current	FCCM = 5V		50		μA
		FCCM = 0V		-50		μA
V_{TRI}	FCCM Tri-State Window		2.1		2.9	V
t_{PS4_EXIT}	PS4 Exit Latency			2.5	5	μs
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to High-Side Gate	PWM: H \rightarrow L, VSWH: H \rightarrow L		18		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L \rightarrow H, GL: H \rightarrow L		25		ns
t_{PDHU}	LS to HS Gate Deadtime	GL: H \rightarrow L, VSWH: L \rightarrow H		20		ns
t_{PDHL}	HS to LS Gate Deadtime	VSWH: H \rightarrow 1V, GL: L \rightarrow H		20		ns
t_{TSSHLD}	Tri-State Shutdown Delay	PWM: L \rightarrow V_{TRI} , GL: H \rightarrow L and PWM: H \rightarrow V_{TRI} , VSWH: H \rightarrow L		150		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: $V_{TRI} \rightarrow$ H, VSWH: L \rightarrow H PWM: $V_{TRI} \rightarrow$ L, GL: L \rightarrow H		35		ns
t_{GLMIN}	LS Minimum On Time	FCCM = 0V (DCM Mode)		550		ns

Notes:

4. All voltages are specified with respect to the corresponding PGND pin.
5. Characterization value. Not tested in production.

Logic Timing Diagrams

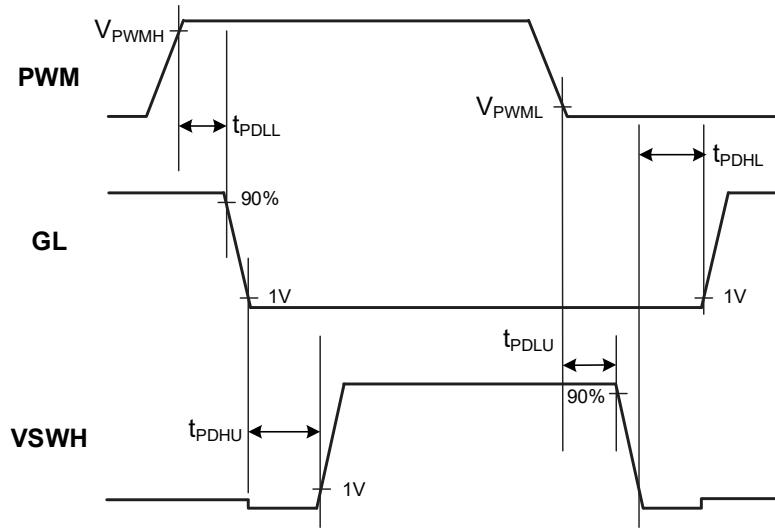


Figure 1. PWM Logic Input Timing Diagram

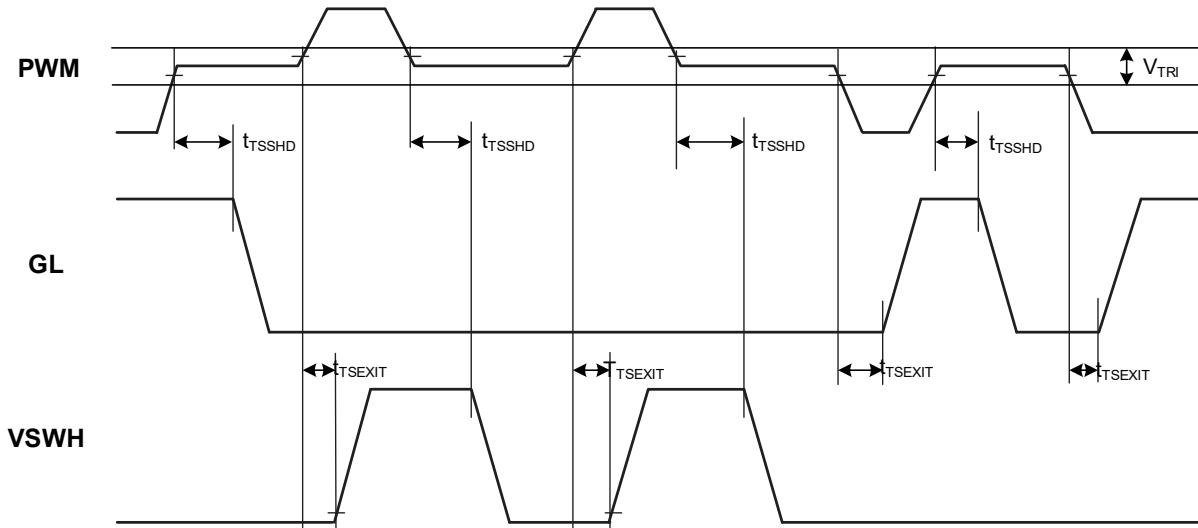


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $P_{VCC} = V_{CC} = 5\text{V}$, unless otherwise specified.

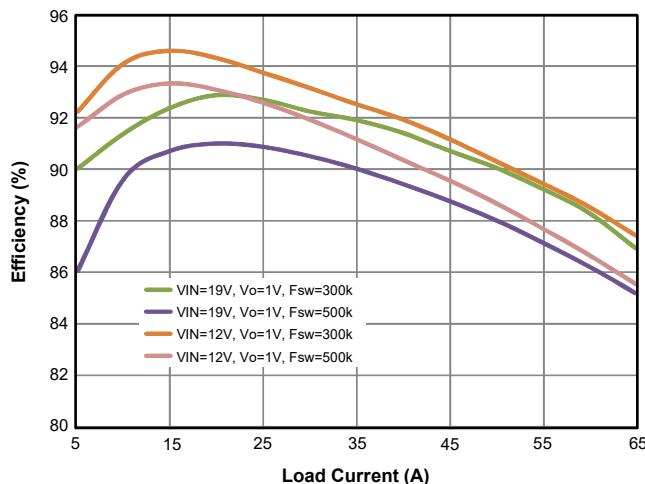


Figure 3. Efficiency vs. Output Current, $V_{OUT} = 1.0\text{V}$

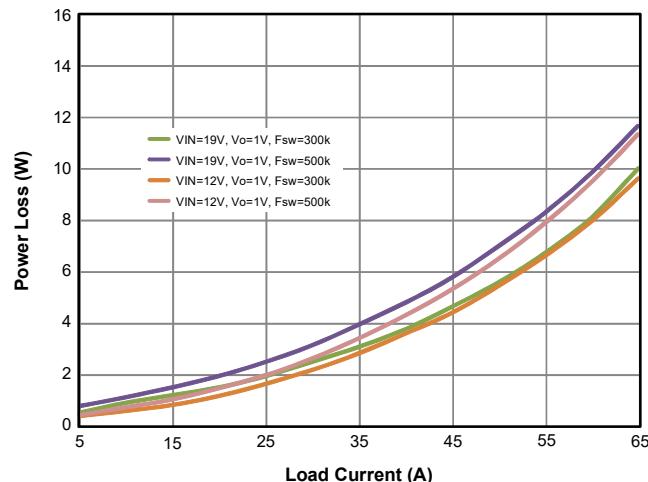


Figure 4. Power Loss vs. Output Current, $V_{OUT} = 1.0\text{V}$

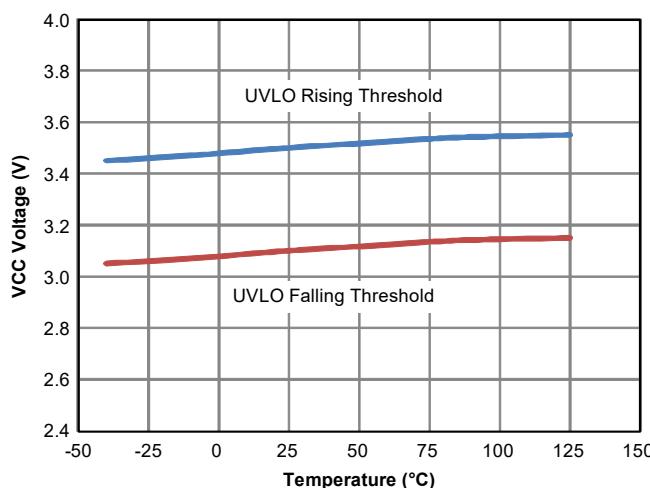


Figure 5. UVLO (VCC) Threshold vs. Temperature

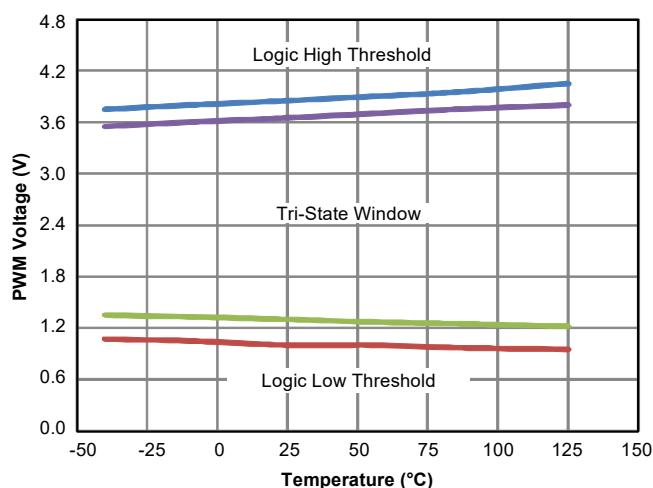


Figure 6. PWM Threshold vs. Temperature

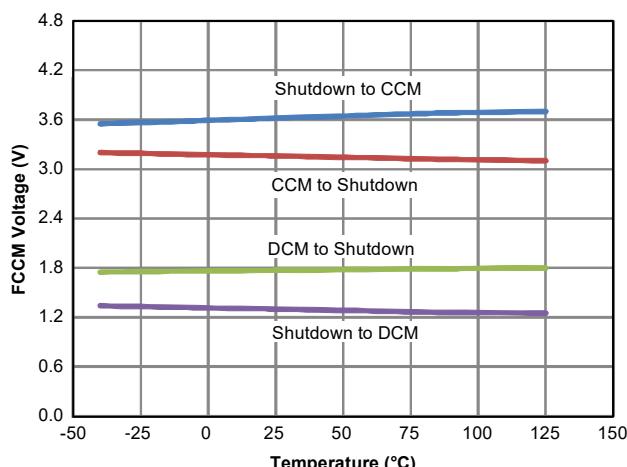


Figure 7. FCCM Threshold vs. Temperature

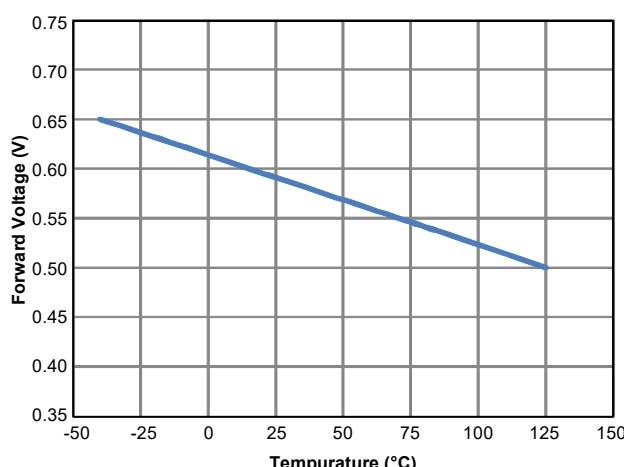


Figure 8. Boot Diode Forward Voltage vs. Temperature

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $P_{VCC} = V_{CC} = 5\text{V}$, unless otherwise specified.

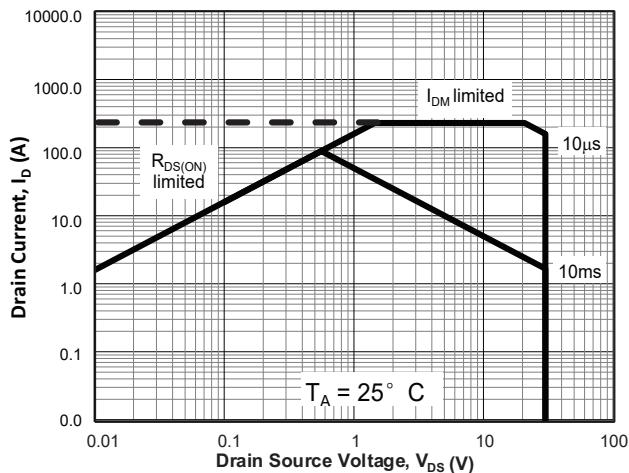


Figure 9. High-Side MOSFET SOA

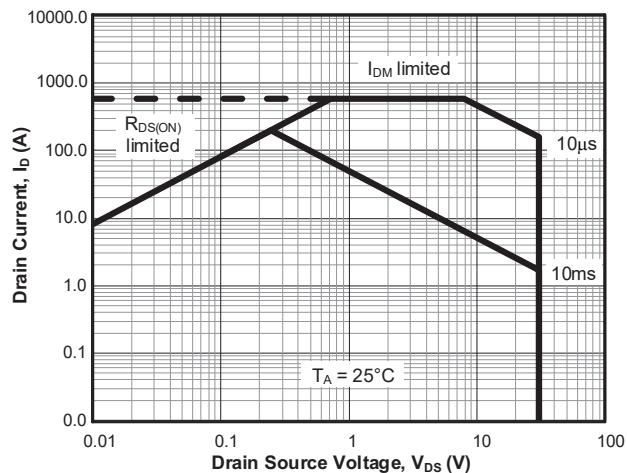


Figure 10. Low-Side MOSFET SOA

Application Information

AOZ5018QI-C is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on both High-Side and Low-Side for a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Powering the Module and the Gate Drives

An external supply $P_{VCC} = 5V$ is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages to achieve the most advantageous compromise between fast switching speed and minimal power loss. The integrated gate driver is capable of supplying large peak current into the Low-Side MOSFET to achieve fast switching. A ceramic bypass capacitor of $1\mu F$ or higher is recommended from P_{VCC} (Pin 29) to P_{GND} (Pin 28). The control logic supply V_{CC} (Pin 3) can be derived from the gate drive supply P_{VCC} (Pin 29) through an RC filter to bypass the switching noise (See Typical Application Circuit).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor ($100nF$) between the $BOOT$ (Pin 5) and the switching node $PHASE$ (Pin 7). It is recommended that this capacitor

C_{BOOT} should be connected to the device across Pin 5 and Pin 7 as close as possible. A bootstrap diode is integrated into the device to reduce external component count. An optional resistor R_{BOOT} in series with C_{BOOT} between 1Ω to 5Ω can be used to slow down the turn on speed of the High-Side MOSFET to achieve both short switching time and low V_{SWH} switching node spikes at the same time.

Under-voltage LockOut

AOZ5018QI-C starts up to normal operation when V_{CC} rises above the Under-Voltage LockOut (UVLO) threshold voltage. The UVLO release is set at 3.5V typically. Since the PWM control signal is provided from an external controller or a digital processor, extra caution must be taken during start up. AOZ5018QI-C must be powered up before PWM input is applied.

Normal system operation begins with a soft start sequence by the controller to minimize in-rush current during start up. Powering the module with a full duty cycle PWM signal may lead to many undesirable consequences due to excessive power. AOZ5018QI-C provides some protections such as UVLO and thermal monitor.

For system level protection, the PWM controller should monitor the current output and protect the load under all possible operating and transient conditions.

Input Voltage VIN

AOZ5018QI-C is rated to operate over a wide input range from 4.5V to 25V. For high current synchronous buck converter applications, large pulse current at high frequency and high current slew rates (di/dt) will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor very close to the package leads at the input supply (VIN). Both X7R or X5R quality surface mount ceramic capacitors are suitable.

The High-Side MOSFET is optimized for fast switching by using low gate charges (Q_G) device. When the module is operated at high duty cycle ratio, conduction loss from the High-Side MOSFET will be higher. The total power loss for the module is still relatively low but the High-Side MOSFET higher conduction loss may have higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. It is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure that they are operating within Safe Operating Area (SOA).

PWM Input

AOZ5018QI-C is compatible with 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives. AOZ5018QI-C is compatible with 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected both High-Side and Low-Side MOSFETs are turned off and V_{SWH} is in high impedance state. Table 1 shows the thresholds level for high-to-low and low-to-high transitions as well as Tri-State window.

There is a Holdoff Delay between the corresponding PWM Tri-State signal and the MOSFET gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches. The Holdoff Delay is typically 175ns.

Table 1. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5018QI-C	4.20V	0.72V	1.60V	3.40V

Note: See Figure 2 for propagation delays and Tri-State window.

Diode Mode Emulation of Low-Side MOSFET (FCCM)

AOZ5018QI-C can be operated in the diode emulation or pulse skipping mode using FCCM (Pin 2). This enables the converter to operate in asynchronous mode during start up, light load or under pre-bias conditions.

When FCCM is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction.

When FCCM is low, the module can operate in Discontinuous Conduction Mode (DCM). The High-Side MOSFET gate drive output is not affected but Low-Side MOSFET will enter diode emulation mode. See Table 2 for the truth table for PWM and FCCM inputs.

Table 2. Control Logic Truth Table

FCCM	PWM	GH	GL
L	L	L	H if $I_L > 0A$ L if $I_L < 0A$
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L
Tri-State	X	L	L

Note: Diode Emulation mode is activated when FCCM pin is Low.

Gate Drives

AOZ5018QI-C has an internal high current high speed driver that generates the floating gate driver for the High-Side MOSFET and a complementary driver for the Low-Side MOSFET. An internal shoot through protection scheme is implemented to ensure that both MOSFETs cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

1) PWM from Logic Low to Logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

2) PWM from Logic High to Logic Low

When the falling edge of switching node VSWH goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on

This mechanism prevents cross conduction across the input bus line VIN and PGND. The anti-overlap circuit monitors the switching node VSWH to ensure a smooth transition between the two MOSFETs under any load transient conditions.

PCB Layout Guidelines

AOZ5018QI-C is a high current module rated for operation up to 2MHz. This requires fast switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor C_{IN} . The PCB design is greatly simplified by the optimization of the AOZ5018QI-C pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors C_{IN} should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor L1, and output capacitor C_{OUT} is the next critical requirement. This requires second layer or “Inner 1” to be the PGND plane. VIAs should then be placed near PGND pads.

While AOZ5018QI-C is a highly efficient module, it is still dissipating significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

As shown in Figure 11, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop that runs along VIN pad originating from the input capacitors that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

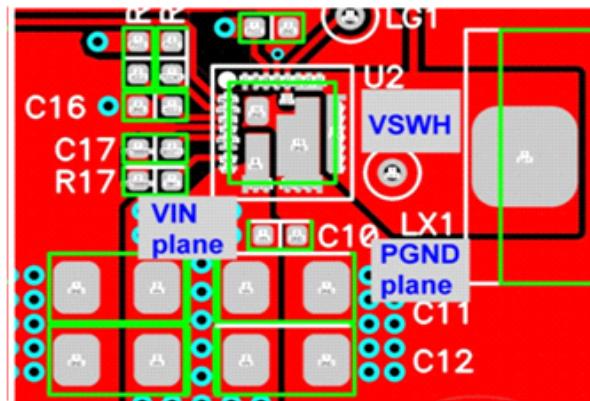


Figure 11. Top Layer of Demo Board, VIN, VSWH and PGND Copper Pads

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dt produced by the package parasitic. To minimize the effects of this interference at the VSWH terminal, at which the main inductor L1 is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this VSWH terminal, only enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers.

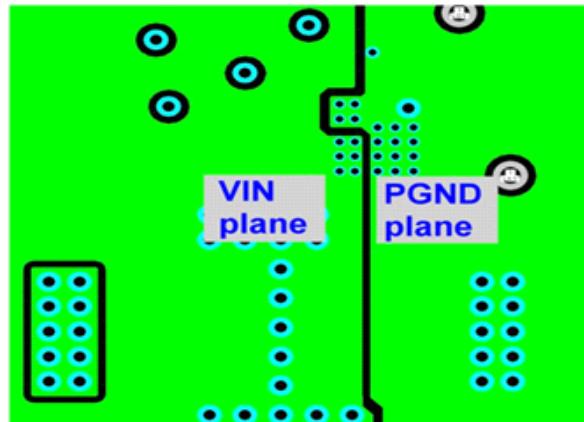
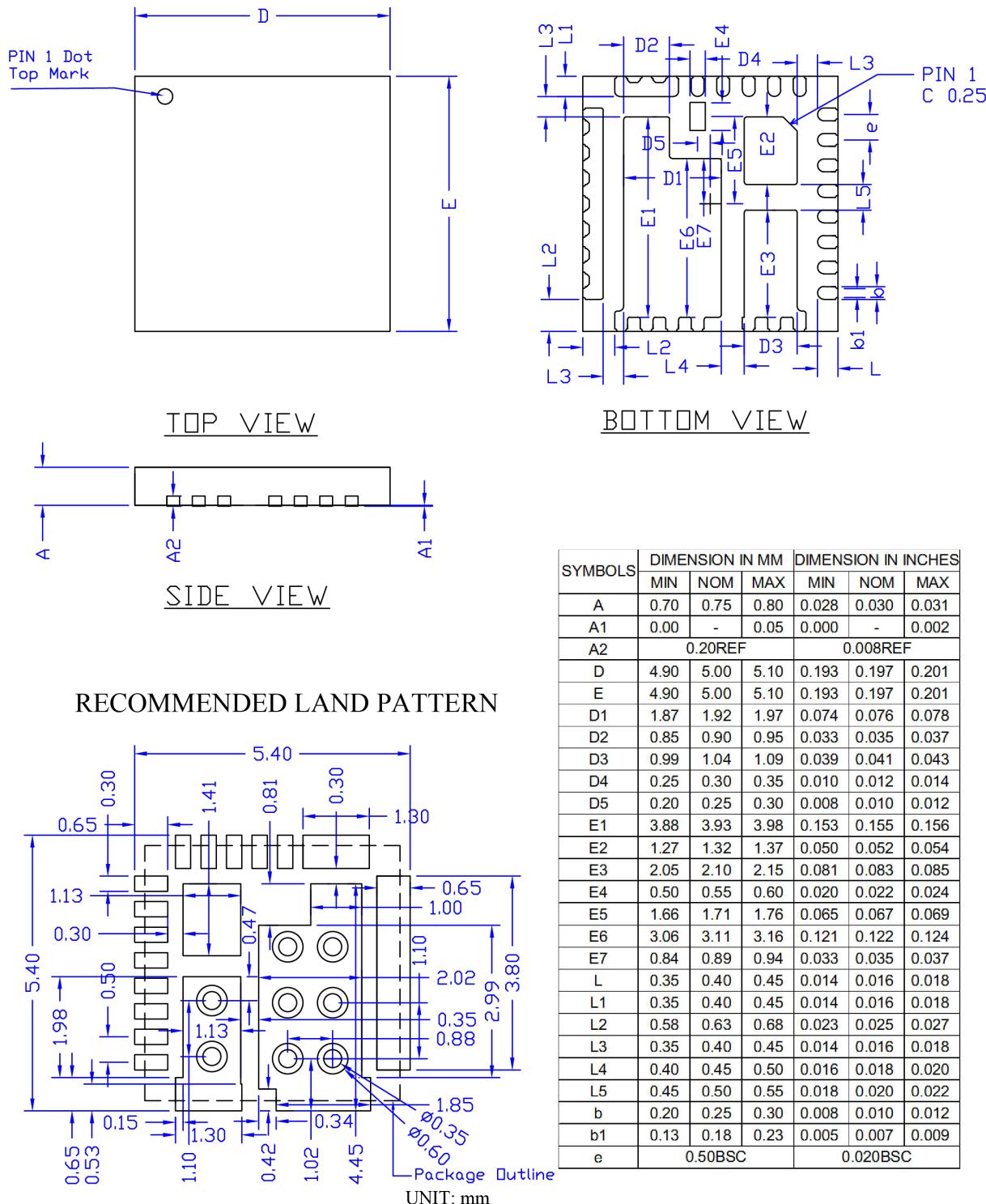


Figure 12. Bottom Layer of PCB

Positioning via through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter VIAs. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent exposed thermal pad.

Package Dimensions, QFN5x5-31L



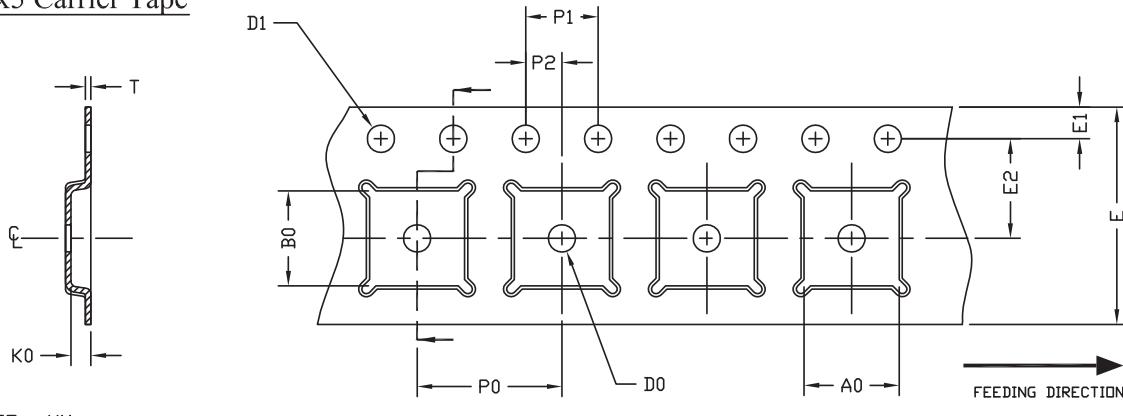
NOTE

CONTROLLING DIMENSION IS MILLIMETER.

CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Drawing, QFN5x5-31L

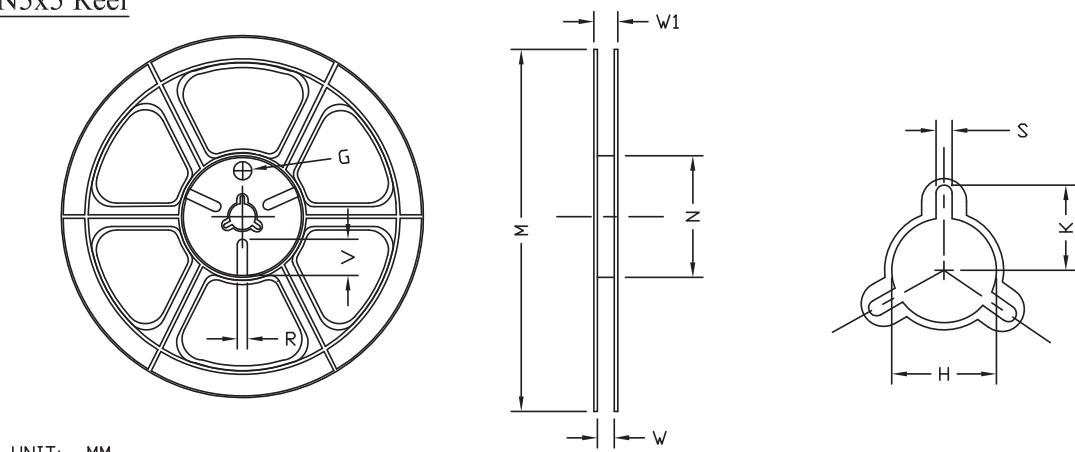
QFN5x5 Carrier Tape



UNIT: MM

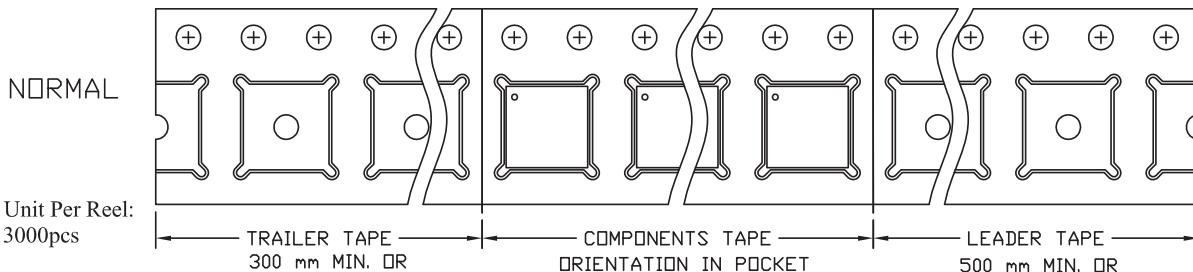
PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ± 0.10	5.25 ± 0.10	1.10 ± 0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ± 0.3	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05

QFN5x5 Reel

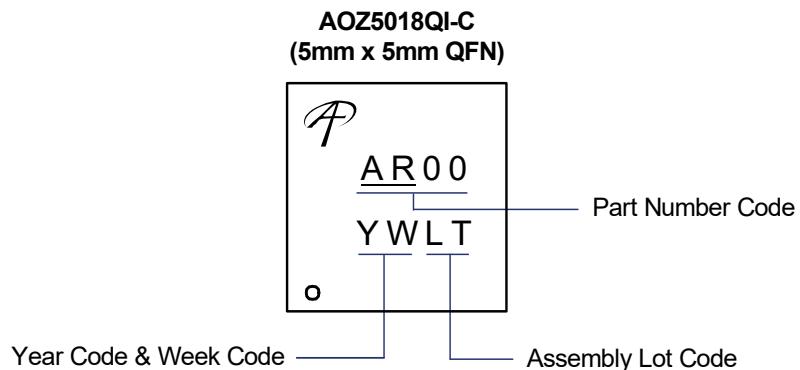


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\phi 330$	$\phi 330.0$ ± 2.0	$\phi 100.0$ ± 1.0	12.4 $^{+2.0}_{-0.0}$	17.0 $^{+2.6}_{-1.2}$	$\phi 13.0$ ± 0.5	10.5 ± 0.2	2.0 ± 0.5	---	---	---



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.