



General Description

The AOZ5516RQI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss. The compact 5mm x 5mm QFN package is optimally chosen and designed to minimize parasitic inductance for minimal EMI signature.

The AOZ5516RQI uses PWM and/or FCCM input for accurate control of the power MOSFETs switching activities, is compatible with 3.3V and 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5516RQI a highly versatile power module. The bootstrap diode is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low parasitics, keeping their effects to a minimum.

Features

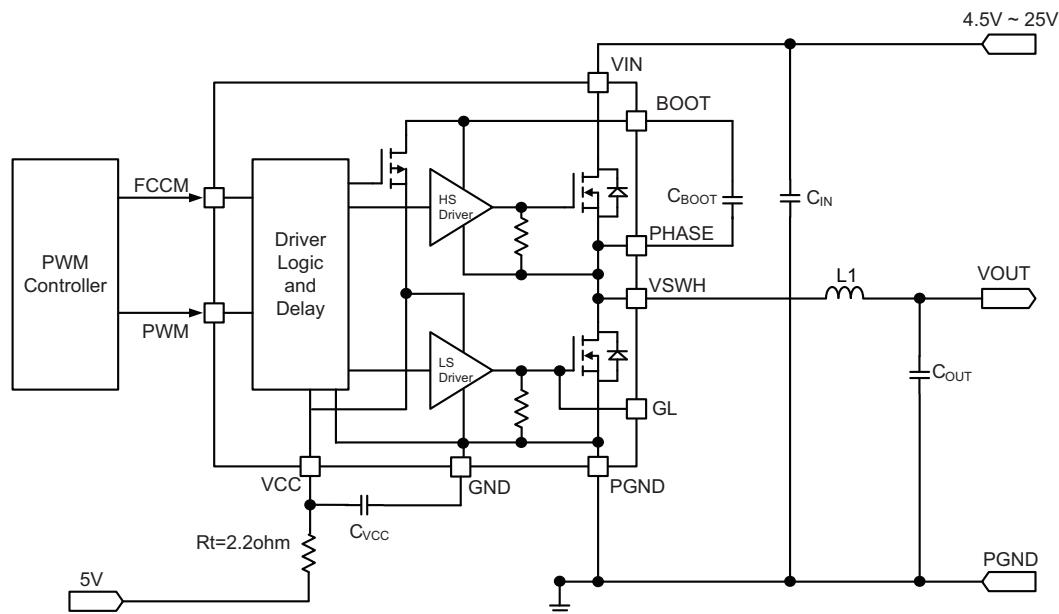
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- 55A continuous output current
 - Up to 80A with 10ms on pulse
 - Up to 120A with 10 μ s on pulse
- Up to 2MHz switching operation
- 3.3V and 5V PWM / Tri-State input compatible
- Under-Voltage Lockout protection
- FCCM pin control for Shutdown / CCM operation
- Standard 5mm x 5mm QFN-31L package

Applications

- Notebook computers
- Memory and graphic cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming console



Typical Application Circuit



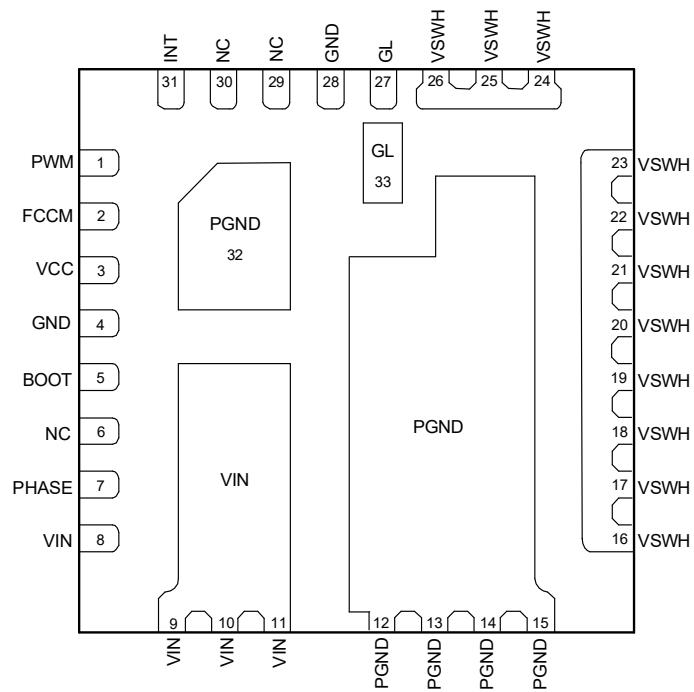
Ordering Information

Part Number	Junction Temperature Range	Package	Environmental
AOZ5516RQI	-40°C to +150°C	QFN5x5.5-31L	RoHS



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit <https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf> for additional information.

Pin Configuration



QFN5x5-31L
 (Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic level.
2	FCCM	Continuous conduction mode of operation is allowed when FCCM = High. FCCM low is undefined operation status. High impedance on the input of FCCM will shutdown both High-Side and Low-Side MOSFETs.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1 μ F MLCC directly between VCC and GND (Pin 4).
4, 28	GND	Ground for Driver Blocks and internal logic.
5	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5).
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
29, 30	NC	No Connect internally. Can connect to any external voltage.
31	INT	Internal testing pin. Shall not connect to any external voltage.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC)	-0.3V to 6.5V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, FCCM)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 35V
Bootstrap Voltage Transient ⁽¹⁾ (BOOT-PGND)	-8V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 6.5V
Bootstrap Voltage DC ⁽¹⁾ (BOOT-PHASE/VSWH)	-0.3V to 8V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient ⁽¹⁾ (PHASE/VSWH)	-7V to 35V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (VCC+0.3V)
Low-Side Gate Voltage Transient ⁽²⁾ (GL)	(PGND-2.5V) to (VCC+0.3V)
VSWH Negative Current 10µs Pulse	-80A
VSWH Current DC	55A
VSWH Current 10ms Pulse	80A
VSWH Current 10µs Pulse	120A
Storage Temperature (TS)	-65°C to +150°C
Max Junction Temperature (TJ)	150°C
ESD Rating ⁽³⁾	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5Ω in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5V to 25V
Low Voltage / MOSFET Driver Supply (VCC)	4.5V to 5.5V
Control Inputs (PWM, FCCM)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics⁽⁴⁾

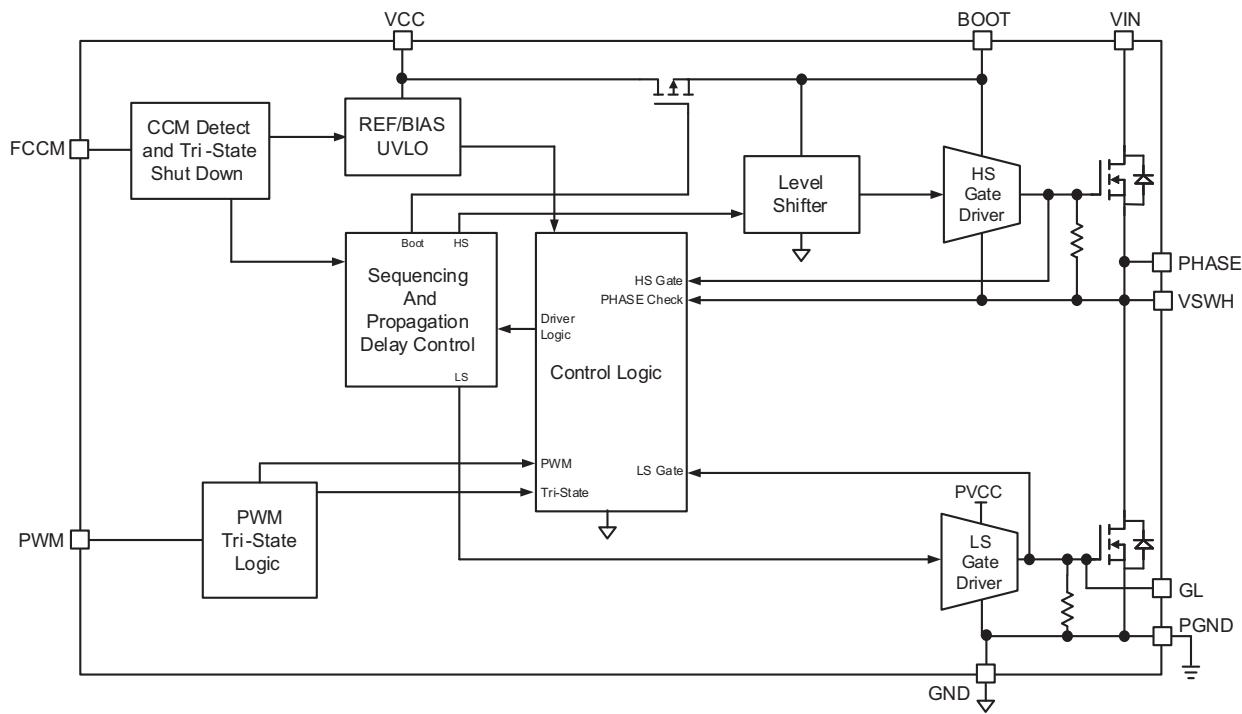
$T_J = 0^\circ\text{C}$ to 150°C , $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $V_{CC} = 5\text{V}$, unless otherwise specified. Min/Max values are guaranteed by test, design or statistical correlation.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GENERAL						
V_{IN}	Power Stage Power Supply		4.5		25	V
V_{CC}	Low Voltage Bias Supply		4.5		5.5	V
$R_{\theta JC}^{(4)}$	Thermal Resistance	Reference to High-Side MOSFET temperature rise		2.5		$^\circ\text{C} / \text{W}$
$R_{\theta JA}^{(4)}$		Freq = 300kHz. AOS Demo Board.		12.5		$^\circ\text{C} / \text{W}$
INPUT SUPPLY AND UVLO						
V_{CCM_UVLO}	Undervoltage Lockout	V_{CC} Rising			4.3	V
V_{CCM_HYST}		V_{CC} Hysteresis		300		mV
I_{VCC}	Control Circuit Bias Current	FCCM = Floating PWM = Floating		3	6	μA
		FCCM = 5V PWM = Floating		130		μA
		FCCM = 5V PWM = High or Low		130		μA
PWM INPUT						
V_{PWM_H}	Logic High Input Voltage		2.72			V
V_{PWM_L}	Logic Low Input Voltage				0.78	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-200		μA
I_{PWM_SNK}		PWM = 5V		200		μA
V_{PWM_TRI}	PWM Tri-State Window		1.4		2.2	V
FCCM INPUT						
V_{FCCM_H}	Logic High Input Voltage		2.73			V
V_{FCCM_L}	FCCM Low Status	FCCM Low is Undefined Operation Status				V
V_{FCCM_TRI}	FCCM Tri-State Window		1.4		2.1	V
t_{PS4_EXIT}	PS4 Exit Latency	FCCM from Tri-State to High			20	μs
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to HS Gate	PWM: H \rightarrow L, VSWH: H \rightarrow L		25		ns
t_{PDLL}	PWM to LS Gate	PWM: L \rightarrow H, GL: H \rightarrow L		20		ns
t_{PDHU}	LS to HS Gate Deadtime	GL: H \rightarrow L, VSWH: L \rightarrow H		30		ns
t_{PDHL}	HS to LS Gate Deadtime	VSWH: H \rightarrow 1V, GL: L \rightarrow H		30		ns
t_{TSSHLD}	Tri-State Shutdown Delay	PWM: L \rightarrow V_{TRI} , GL: H \rightarrow L and PWM: H \rightarrow V_{TRI} , VSWH: H \rightarrow L		50		ns
$t_{TSEEXIT}$	Tri-State Propagation Delay	PWM: $V_{TRI} \rightarrow$ H, VSWH: L \rightarrow H PWM: $V_{TRI} \rightarrow$ L, GL: L \rightarrow H		20		ns
t_{LGMIN}	LS Minimum On Time			35		ns

Notes:

4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.

Functional Block Diagram



Timing Diagrams

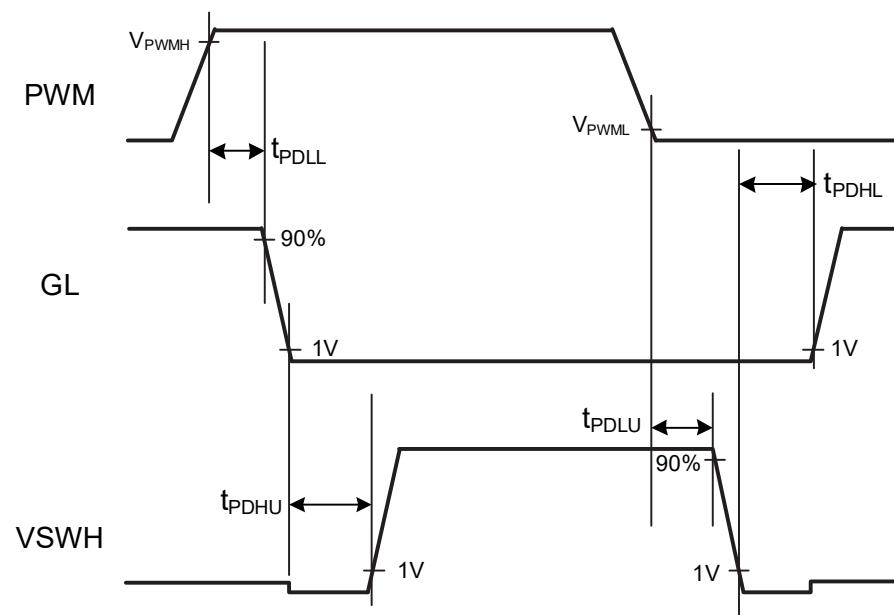


Figure 1. PWM Logic Input Timing Diagram

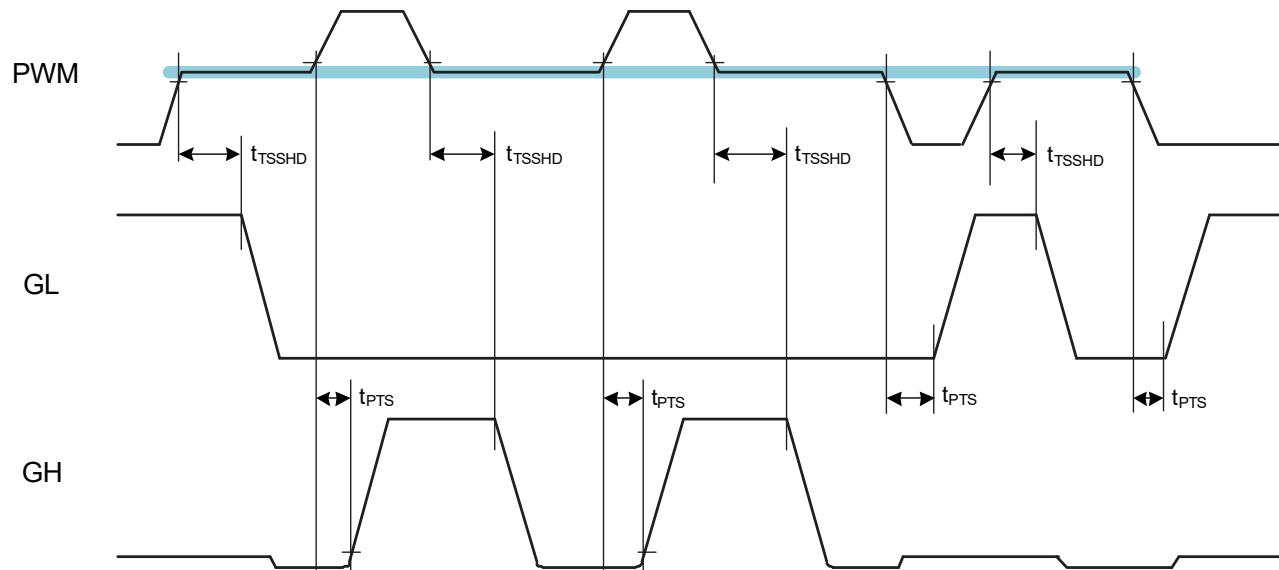


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 1\text{V}$, $V_{CC} = 5\text{V}$, unless otherwise specified.

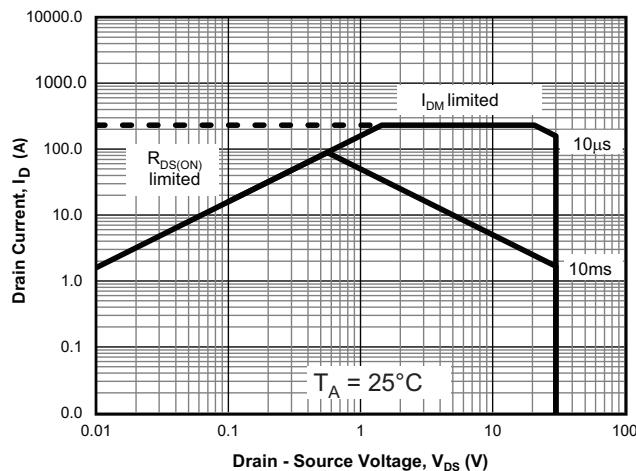


Figure 3. High-Side MOSFET SOA

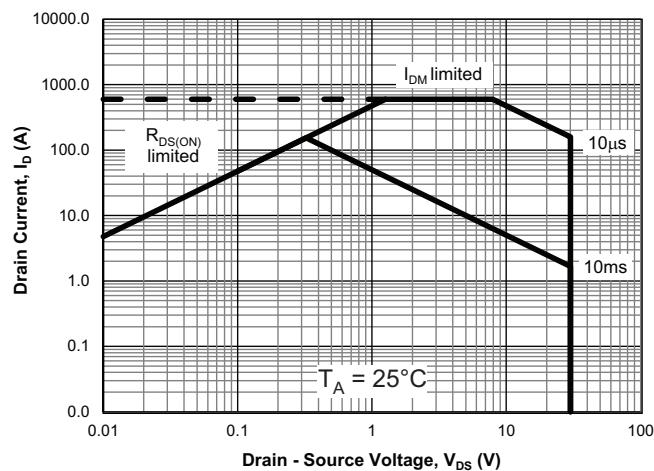


Figure 4. Low-Side MOSFET SOA

Application Information

AOZ5516RQI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on both High-Side and Low-Side for a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Powering the Module and the Gate Drives

An external supply $V_{CC} = 5V$ is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages to achieve the most advantageous compromise between high switching speed and minimal power loss. The integrated gate driver is capable of supplying large peak current into the Low-Side MOSFET to achieve fast switching. A ceramic bypass capacitor of $1\mu F$ or higher is recommended from V_{CC} (Pin 3) to GND (Pin 4). V_{CC} (Pin 3) can be derived from 5V power supply through an RC filter to bypass the switching noise (See Typical Application Circuit). The R value is recommended 1Ω , and the maximum value can not be higher than 2.2Ω to avoid large voltage drop during the high switching frequency operation.

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor ($100nF$) between the $BOOT$ (Pin 5) and the switching node $PHASE$ (Pin 7). It is recommended that this capacitor C_{BOOT} should be connected to the device across Pin 5 and Pin 7 as closely as possible. A bootstrap switch is integrated into the device to reduce external component count.

Under-voltage Lockout

AOZ5516RQI starts up to normal operation when V_{CC} rises above the Under-Voltage Lockout (UVLO) threshold voltage. Since the PWM control signal is provided from an external controller or a digital processor, extra caution must be taken during start up. AOZ5516RQI must be powered up before PWM input is applied.

Normal system operation begins with a soft start sequence by the controller to minimize in-rush current during start up. Powering the module with a full duty cycle

PWM signal may lead to many undesirable consequences due to excessive power. AOZ5516RQI provides some protections such as UVLO and thermal monitor. For system level protection, the PWM controller should monitor the current output and protect the load under all possible operating and transient conditions.

Input Voltage V_{IN}

AOZ5516RQI is rated to operate over a wide input range from 4.5V to 25V. For high current synchronous buck converter applications, large pulse current at high frequency and high current slew rates (di/dt) will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor very close to the package leads at the input supply (V_{IN}). Both X7R or X5R quality surface mount ceramic capacitors are suitable.

The High-Side MOSFET is optimized for fast switching by using a low gate charge (Q_G) device. When the module is operated at high duty cycle ratio, conduction loss from the High-Side MOSFET will be higher. The total power loss for the module is still relatively low but the High-Side MOSFET higher conduction loss may have higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. It is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure that they are operating within Safe Operating Area (SOA).

PWM Input

Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected, both High-Side and Low-Side MOSFETs are turned off and V_{SWH} is in high impedance state.

There is a Holdoff Delay between the corresponding PWM Tri-State signal and the MOSFET gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches.

FCCM Operation

When FCCM is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction.

Once FCCM is in tri-state, both HS and LS are off. When FCCM is in tri-state and PWM is tri-state, the module enters the shut down mode ($I_{VCC} = 3\mu A$). See Table 1 for the truth table for PWM and FCCM inputs.

Table 1. Control Logic Truth Table.

FCCM	PWM	GH	GL
L	X	NA	NA
H	H	H	L
H	L	L	H
H	Tri-State	L	L
Tri-State	Tri-State	L	L
Tri-State	H	L	L
Tri-State	L	L	L

Gate Drives

AOZ5516RQI has an internal high current high speed driver that generates the floating gate driver for the High-Side MOSFET and a complementary driver for the Low-Side MOSFET. An internal shoot through protection scheme is implemented to ensure that both MOSFETs cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

1) PWM from logic Low to logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

2) PWM from logic High to logic Low

When the falling edge of switching node VSWH goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on.

This mechanism prevents cross conduction across the input bus line VIN and PGND. The anti-overlap circuit monitors the switching node VSWH to ensure a smooth transition between the two MOSFETs under any load transient conditions.

PCB Layout Guidelines

AOZ5516RQI is a high current module rated for operation up to 2MHz. This requires high switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor C_{IN} . The PCB design is greatly simplified by the optimization of the AOZ5516RQI pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors C_{IN} should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor L1, and output capacitor C_{OUT} is the next critical requirement. This requires second layer or "Inner 1" to be the PGND plane. VIAs should then be placed near PGND pads.

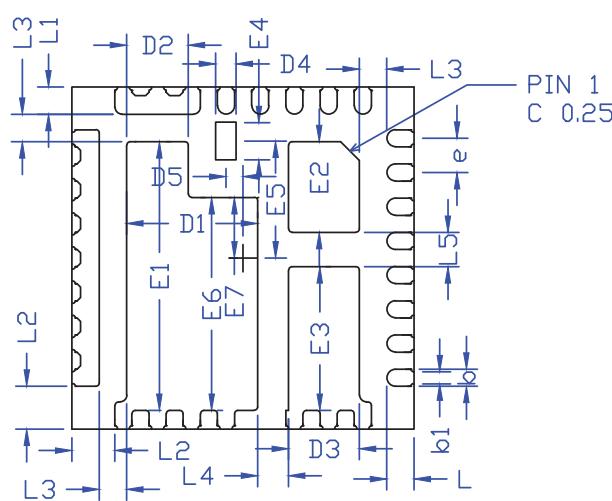
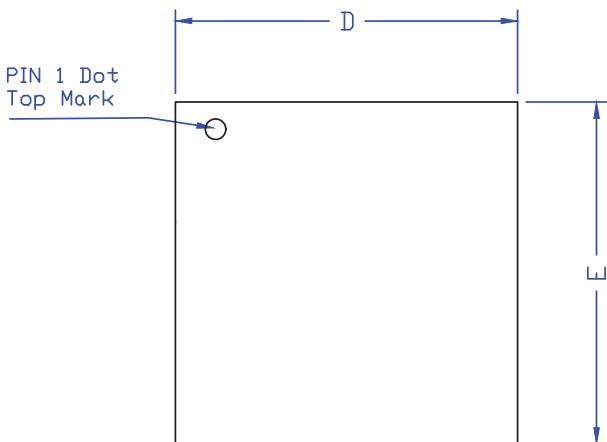
While AOZ5516RQI is a highly efficient module, it still dissipates a significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and VSWH pads should

be attached to large areas of PCB copper. Thermal relief pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

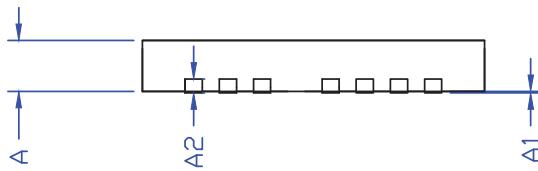
The top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop which runs along VIN pad originating from the input capacitors C10, C11, and C12 that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fans out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spikes appear at the VSWH terminal which are caused by the large internal di/dt produced by the package parasitic. To minimize the effects of this interference at the VSWH terminal, at which the main inductor L1 is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this VSWH terminal, only enough so the inductor can be securely mounted.

Package Dimensions, QFN5x5A-31L

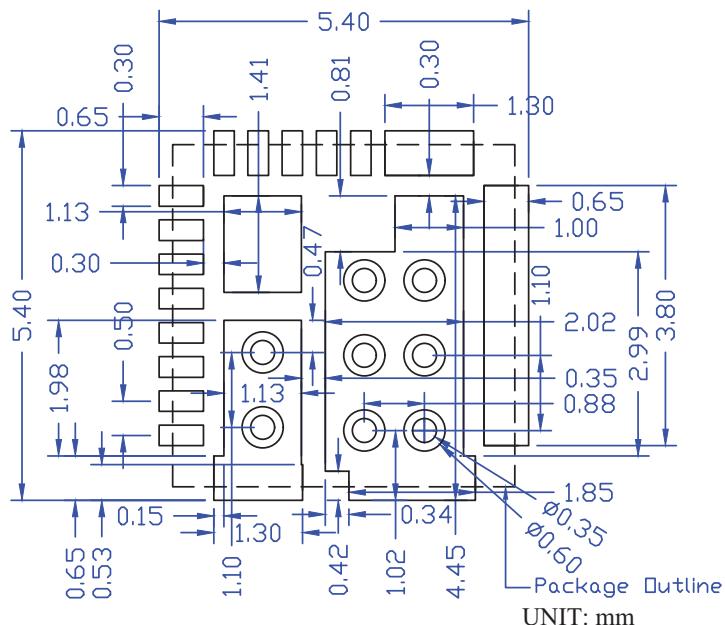


TOP VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



NOTE

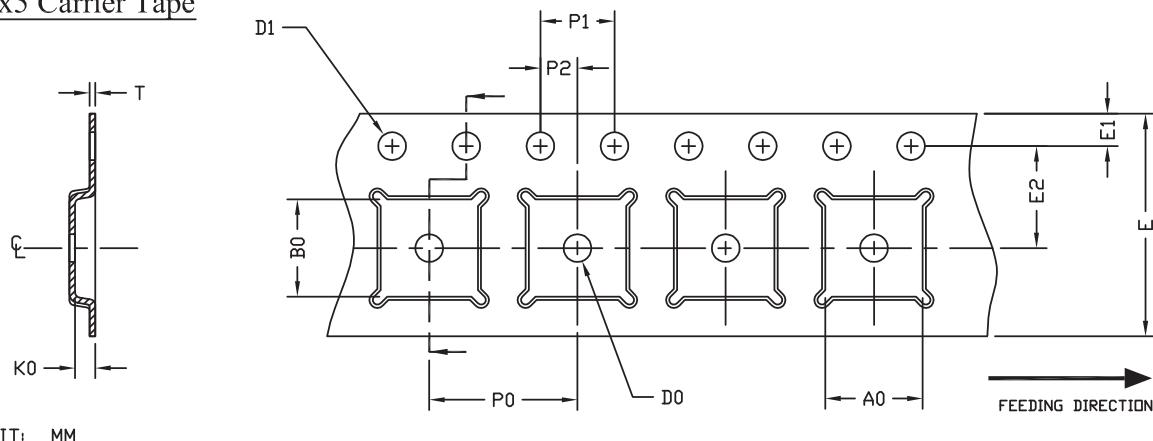
CONTROLLING DIMENSION IS MILLIMETER.

CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2			0.20REF	0.008REF		
D	4.90	5.00	5.10	0.193	0.197	0.201
E	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.87	1.92	1.97	0.074	0.076	0.078
D2	0.85	0.90	0.95	0.033	0.035	0.037
D3	0.99	1.04	1.09	0.039	0.041	0.043
D4	0.25	0.30	0.35	0.010	0.012	0.014
D5	0.20	0.25	0.30	0.008	0.010	0.012
E1	3.88	3.93	3.98	0.153	0.155	0.156
E2	1.27	1.32	1.37	0.050	0.052	0.054
E3	2.05	2.10	2.15	0.081	0.083	0.085
E4	0.50	0.55	0.60	0.020	0.022	0.024
E5	1.66	1.71	1.76	0.065	0.067	0.069
E6	3.06	3.11	3.16	0.121	0.122	0.124
E7	0.84	0.89	0.94	0.033	0.035	0.037
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.35	0.40	0.45	0.014	0.016	0.018
L2	0.58	0.63	0.68	0.023	0.025	0.027
L3	0.35	0.40	0.45	0.014	0.016	0.018
L4	0.40	0.45	0.50	0.016	0.018	0.020
L5	0.45	0.50	0.55	0.018	0.020	0.022
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.13	0.18	0.23	0.005	0.007	0.009
e	0.50BSC			0.020BSC		

Tape and Reel Drawing, QFN5x5A-31L

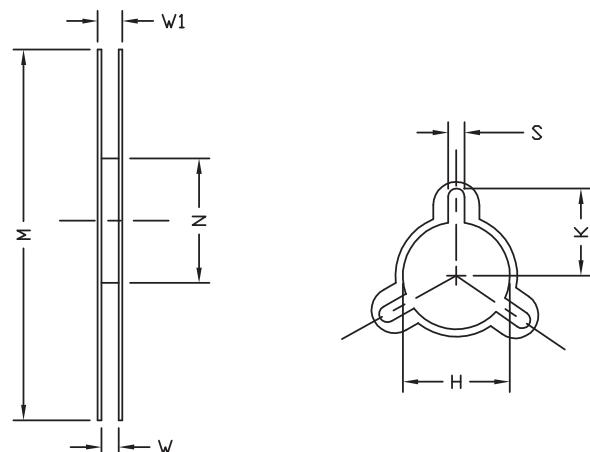
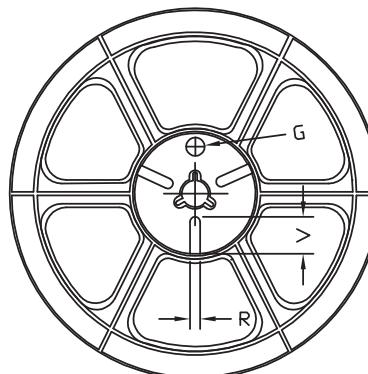
QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ± 0.10	5.25 ± 0.10	1.10 ± 0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ± 0.3	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05

QFN5x5 Reel



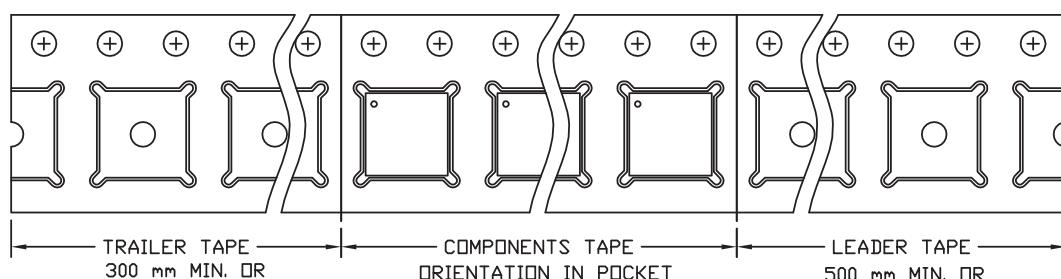
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	$\varnothing 330$	$\varnothing 330.0$ ± 2.0	$\varnothing 79.0$ ± 1.0	12.4 $^{+2.0}_{-5.0}$	17.0 $^{+2.0}_{-1.2}$	$\varnothing 13.0$ ± 0.5	10.5 ± 0.2	2.0 ± 0.5	---	---	---

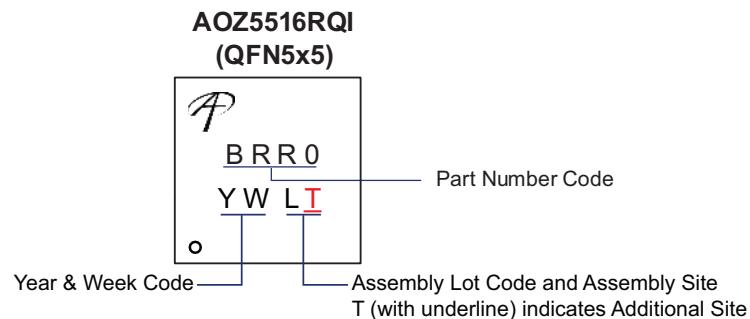
Leader / Trailer & Orientation

NORMAL

Unit Per Reel:
3000pcs



Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.