

General Description

The AOZ73456QV is a monitoring IC capable of simultaneously multiplexing up to 4 bus voltages, currents, 2 IMON inputs and reference ground calibration into one differential output signal.

The bus current is sensed via a shunt resistor, and provided into a high accuracy built-in input differential amplifier. The bus voltages and currents can be scaled to a lower voltage using individual programmable gains. The scaled bus voltages, currents, IMON data, and the reference ground information are multiplexed and sequentially output by a different amplifier.

An integrated I²C interface allows for customization, including configuring the activity of each output channel, setting the scaling gains of bus voltages and currents, adjusting the offset voltage and common mode voltage of the output differential amplifier, enabling the alternating polarity mode, timeout, and setting the skip cycles for dual-device mode.

The AOZ73456QV is available in a 4mm×4mm QFN-32L package and is rated over a -40°C to +105°C operating temperature range.

Features

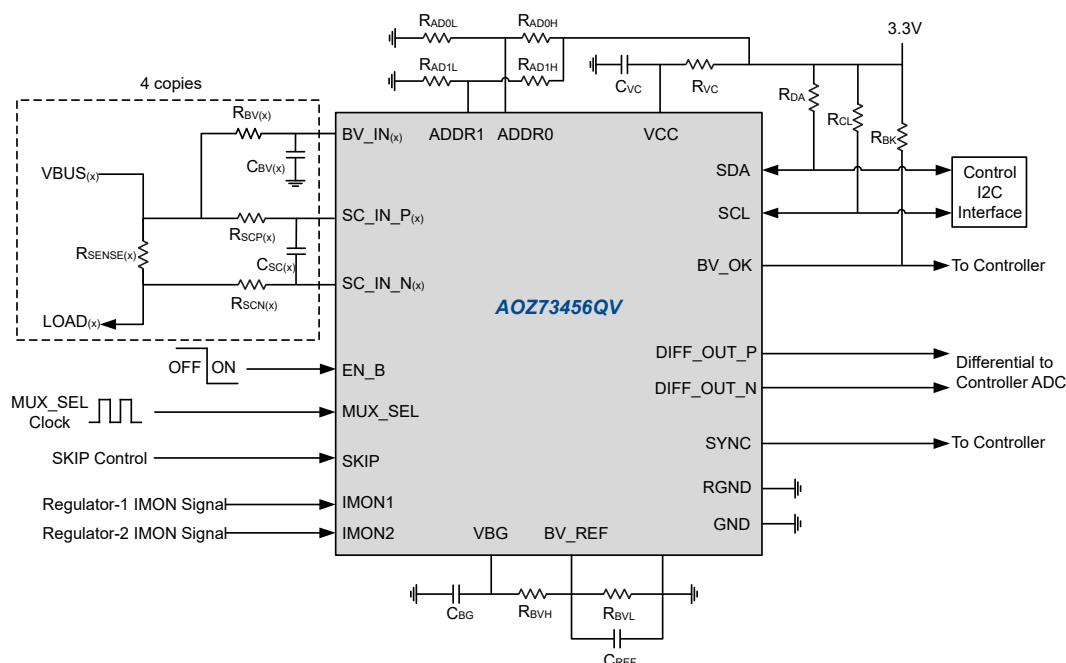
- Supports up to maximum 4 bus channels monitoring with single device
- Supports up to maximum 8 bus channels monitoring with dual-device mode
- Bus voltage monitoring range up to 26V
- Supports 2 IMON signal monitoring
- Reference ground calibration
- High accuracy differential output for the scaled signals from the selected channel of multiplexer
- I²C interface configuration
- Bus voltage OK indication
- Thermally enhanced 32-pin 4mm×4mm QFN

Applications

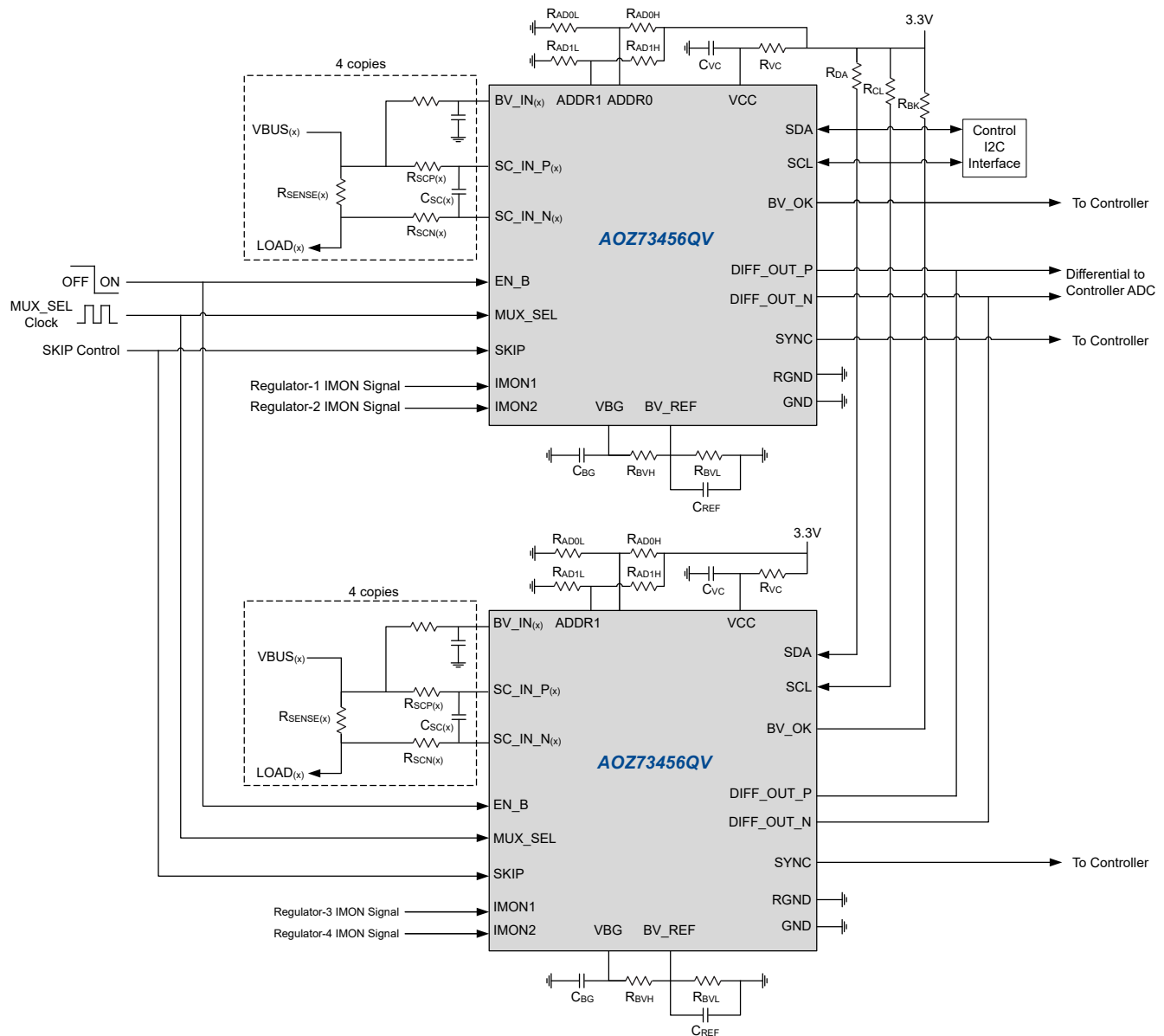
- Computers / notebooks / graphics card
- Power management
- Battery chargers



Single-Device Mode Typical Application



Dual-Device Mode Typical Application



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ73456QV	-40°C to +105°C	QFN4x4-32L	Green



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit <https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf> for additional information.

Pin Configuration

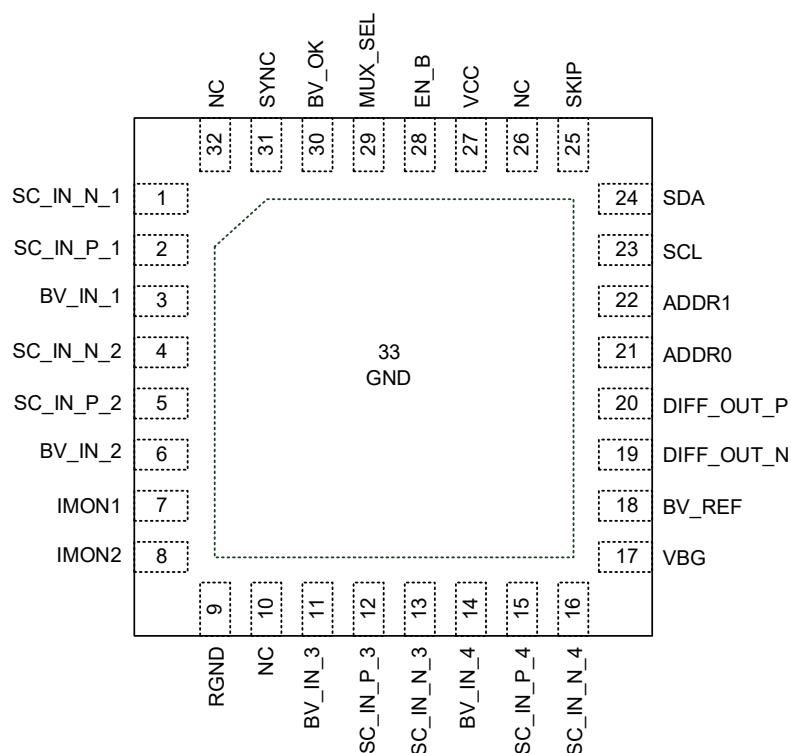


Figure 1. QFN4x4-32L
(Top View)

Pin Description

Pin Number	Pin Name	I/O	Pin Function
1, 4, 13, 16	SC_IN_N _(x)	AI	Negative input node of internal shunt current differential amplifier. Connect this pin to the negative node of shunt resistor.
2, 5, 12, 15	SC_IN_P _(x)	AI	Positive input node of internal shunt current differential amplifier. Connect this pin to the positive node of shunt resistor.
3, 6, 11, 14	BV_IN _(x)	AI	Bus voltage sense input. Connect this pin to the expected monitoring node.
7, 8	IMON _(x)	AI	Current monitoring signal input. Connect this pin to the IMON output of monitored voltage regulator.
9	RGND	GND	Reference ground for multiplexer and differential amplifier.
10, 26, 32	NC		No Connect.
17	VBG	AO	1.3V band-gap reference voltage output. Connect a 100nF bypass MLCC on this pin.
18	BV_REF	AI	Reference voltage input for BV_OK comparator.
19	DIFF_OUT_N	AO	Negative output of differential amplifier. Connect this pin to the negative node of GPU's analog-to-digital converter.
20	DIFF_OUT_P	AO	Positive output of differential amplifier. Connect this pin to the Positive node of GPU's analog-to-digital converter.
21,22	ADDR0,1	DI	Bit 0, bit 1 of I ² C address setting.
23	SCL	DI	I ² C clock input terminal.
24	SDA	DI/DO	I ² C data input/output terminal.
25	SKIP	DI	Mask for bus voltage OK indication.
27	VCC	PWR	Device power supply input. Bypass VCC pin with a minimum 1μF MLCC.
28	EN_B	DI	Enable control input.
29	MUX_SEL	DI	Multiplexer selection input.
30	BV_OK	DO	Bus voltage OK indication output. An open-drain MOSFET output is used to indicate the status of bus voltage is ready or not.
31	SYNC	DO	Synchronous pulse output. A pulse is outputted from this pin at the first cycle of MUX_SEL sequence.
33	GND	GND	Device ground.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
BV_IN _(x) , SC_IN_P _(x) , SC_IN_N _(x) to GND	-0.3V to +30V
VCC to GND	-0.3V to +5.5V
DIFF_OUT_P, DIFF_OUT_N to GND	-0.3V to +1.8V
RGND to GND	-0.3V to +5.5V
Other Pins to GND	-0.3V to +5.5V
Operating Temperature Range	-40°C to +105°C
Functional Temperature Range	-40°C to +125°C
Maximum Junction Temperature	+125°C
Storage Temperature	-65°C to +150°C
ESD Rating HBM	1.5kV
ESD Rating CBM	1.0kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Input Power, VCC	2.8V to 3.8V
Bus Monitoring Input Voltages, BV_IN _(x) , SC_IN_P _(x) , SC_IN_N _(x)	5V to 26V
Differential Amplifier Output, (DIFF_OUT_P – DIFF_OUT_N)	-0.8V to 0.8V
Ambient Temperature (T _A)	-40°C to +85°C
Junction Temperature (T _J)	-40°C to +125°C

Package Thermal Information

Symbol	Parameter	Rating
θ_{JA}	Junction-to-Ambient Thermal Resistance	40°C/W
θ_{JC}	Junction-to-Case Resistance	10°C/W

Electrical Characteristics

T_A = 25°C, VCC = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Multiplexer						
E _{STL1}	Multiplexer Settling Error @t=100nS ⁽¹⁾	From rising edge of MUX_SEL to target timing			9.375	mV
E _{STL2}	Multiplexer Settling Error @t=300nS ⁽¹⁾				3	mV
t _{Timeout}	MUX_SEL Timeout		35		45	μs
t _{MUX}	MUX_SEL Period		0.185			μs
f _{MUX}	MUX_SEL Frequency				5.5	MHz
V _{th_high_MUX}	MUX_SEL Input High Threshold		0.945			V
V _{th_low_MUX}	MUX_SEL Input Low Threshold				0.405	V
Shunt Current Input Differential Amplifier						
V _{SC_OFST}	Input Amplifier Offset		-2		2	mV
V _{SC_OFST_DR}	Input Amplifier Offset Drift ⁽¹⁾		-6		6	mV
V _{SC_CMRR}	Input Amplifier CMRR ⁽¹⁾		80			dB
G _{SC}	Shunt Current Gain Range		2		24	V/V
G _{SC_tol}	Shunt Current Gain Tolerance				0.6	%

Electrical Characteristics

T_A = 25°C, VCC = 3.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Bus Voltage Monitoring						
G _{BV}	Bus Voltage Gain Range		1/64		1/4	V/V
G _{BV_tol}	Bus Voltage Gain Tolerance				0.6	%
Input Current Consumptions (Full Functional Mode)						
I _{BV_FF}	BV_IN Current (Full Functional Mode)				600	μA
I _{SCP_FF}	SC_IN_P Current (Full Functional Mode)				60	μA
I _{SCN_FF}	SC_IN_N Current (Full Functional Mode)				60	μA
I _{CC_FF}	VCC Current (Full Functional Mode)			2.8		mA
Input Current Consumptions (Limited Function Mode)						
I _{BV_LIM}	BV_IN Current (Limited Function Mode)				120	μA
I _{SCP_LIM}	SC_IN_P Current (Limited Function Mode)				1	μA
I _{SCN_LIM}	SC_IN_N Current (Limited Function Mode)				1	μA
I _{CC_LIM}	VCC Current (Limited Function Mode)			300		μA
Input Current Consumptions (Standby Mode)						
I _{BV_STB}	BV_IN Current (Standby Mode)				2	μA
I _{SCP_STB}	SC_IN_P Current (Standby Mode)				1	μA
I _{SCN_STB}	SC_IN_N Current (Standby Mode)				1	μA
I _{CC_STB}	VCC Current (Standby Mode)			250		μA
I _{BV_VCC_FLT}	BV_IN Current (VCC Floating)				2	μA
Bus Voltage OK Indicator (BV_OK) and Band-Gap Reference						
V _{BG}	Band-Gap Reference Output		1.274	1.3	1.326	V
I _{BG}	Band-Gap Reference Maximum Loading Current				100	μA
R _{BV_OK}	BV_OK Low Impedance				300	Ω
V _{th_BVOK}	BV_REF Voltage Range		100		800	mV
V _{BV_OK_HYS}	BV_OK Comparator Hysteresis			10		%
r _{BV_divider}	Bus Voltage Input Divider Ratio for BV_OK			1/32		
I _{BV_REF}	BV_REF Input Leakage Current				100	nA
Power Reset (POR)						
V _{th_VCC_POR}	VCC POR Threshold for BV_OK Comparator		2.6		2.8	V
V _{th_VCC_HYS}	VCC POR Hysteresis for BV_OK Comparator			150		mV
Enable						
R _{EN_tri}	Enable Tri-state Resistance		100			kΩ
V _{th_EN_H}	Enable Input High Threshold		0.945			V
V _{th_EN_L}	Enable Input Low Threshold				0.405	V
T _{DLY}	Delay Time of Standby or Limited Function Mode to Full Function Mode				40	μs

Electrical Characteristics

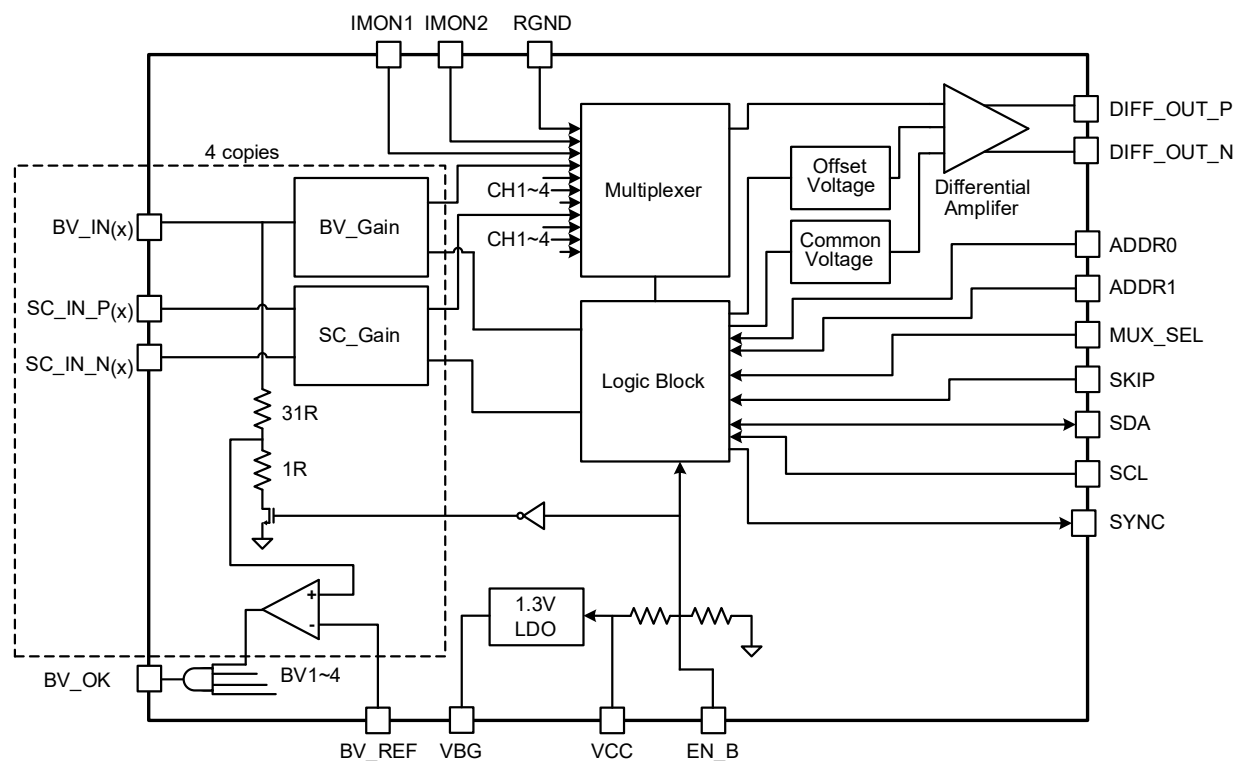
$T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SKIP						
$V_{\text{SKIP_H}}$	SKIP Input High Range		2.8		3.8	V
$V_{\text{th_SKIP_L}}$	SKIP Input Low Threshold				0.405	V
Address Setting						
$V_{\text{th_ADDR_H}}$	ADDR Input High Threshold		0.945			V
$V_{\text{th_ADDR_L}}$	ADDR Input Low Threshold				0.405	V
I_{ADDR}	ADDR Input Leakage Current				100	nA
IMON						
I_{MON}	IMON Input Leakage Current				100	nA
$V_{\text{IMON_OFST}}$	IMON Offset Voltage		-2		2	mV
RGND						
$V_{\text{RGND_OFST}}$	RGND Offset Voltage		-2		2	mV

Note:

1. Guaranteed by design.

Functional Block Diagram



I²C Control Specification

Guaranteed by design. No test in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency				400	kHz
V_{IH}	Input High Threshold		$0.7V_{DD}$			V
V_{IL}	Input Low Threshold				$0.3V_{DD}$	V
V_{I2C_OL}	Low Level Output voltage	Open drain, 3mA sink current			0.4	V
$t_{HD;STA}$	Hold Time (Repeated), START Condition		0.26			μs
t_{LOW}	Low Period of SCL Clock		0.5			μs
t_{HIGH}	High Period of SCL Clock		0.26			μs
$t_{SU;STA}$	Set-up Time (Repeated), START Condition		0.26			μs
$t_{HD;DAT}$	Data Hold Time		0			ns
$t_{SU;DAT}$	Data Set-up Time		50			ns
t_r	Rise Time (SDA, SCL)				120	ns
t_f	Fall Time (SDA, SCL)		$20 \times (V_{DD}/5.5V)$		120	ns
$t_{SU;STO}$	Set-up Time for STOP Condition		0.26			μs
t_{BUF}	Bus Free Time between STOP and START Conditions		0.5			μs
C_b	Capacitive Load for Each Bus Line				550	pF

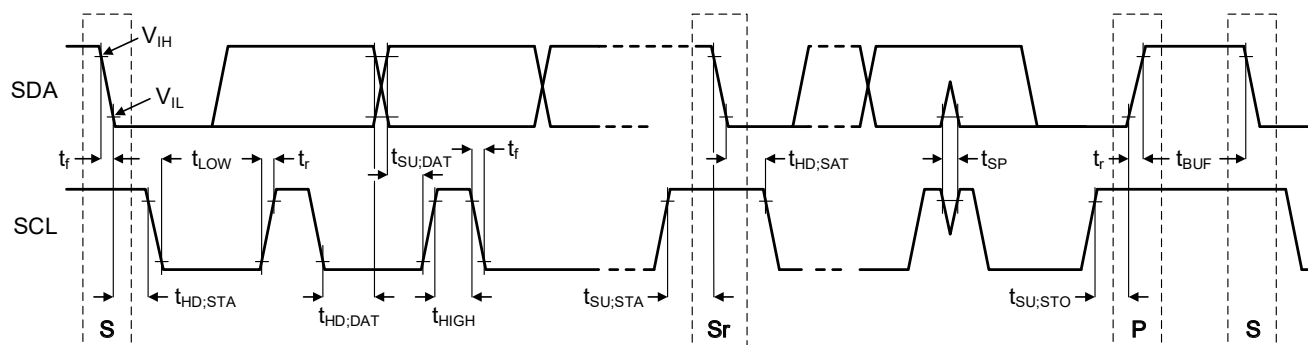


Figure 2. I²C BUS Timing Diagram

I²C Register Map

Register Address	Register Name	Bits	R/W	Description	Default	New Value Takes Effect
0x00	Vendor ID	7:0	R			
0x01	Device ID	7:0	R			
0x04	Active_Channel	7	R/W	Ground Reference	0 (Disable)	At next MUX_SEL cycle
		6	--	No definition	--	--
		5	R/W	IMON Channel 2	0 (Disable)	At next MUX_SEL cycle
		4	R/W	IMON Channel 1	0 (Disable)	At next MUX_SEL cycle
		3	R/W	Bus Channel 4	1 (Enable)	At next MUX_SEL cycle
		2	R/W	Bus Channel 3	1 (Enable)	At next MUX_SEL cycle
		1	R/W	Bus Channel 2	1 (Enable)	At next MUX_SEL cycle
		0	R/W	Bus Channel 1	1 (Enable)	At next MUX_SEL cycle
0x05	MUX_SEL_Skip	7:4	R/W	Pulses to skip at the start of MUX_SEL cycle	0 (No skip)	Immediately
		3:0	R/W	Pulses to skip at the end of MUX_SEL cycle	0 (No skip)	Immediately
0x06	Alternating_Polarity_Mode	7:7	R/W	0b1: Enable alternating mode 0b0: Disable alternating mode	0 (Disable)	Immediately
0x07	Diff_Amp_Offset	3:0	R/W	0b1111: -375 mV	0b0000 (0mV)	Immediately
				0b1110: -350 mV		
				0b1101: -325 mV		
				0b1100: -300 mV		
				0b1011: -275 mV		
				0b1010: -250 mV		
				0b1001: -225 mV		
				0b1000: -200 mV		
				0b0111: -175 mV		
				0b0110: -150 mV		
				0b0101: -125 mV		
				0b0100: -100 mV		
				0b0011: -75 mV		
				0b0010: -50 mV		
				0b0001: -25 mV		
				0b0000: 0 mV		

I²C Register Map

Register Address	Register Name	Bits	R/W	Description	Default	New Value Takes Effect
0x08	Diff_Amp_CM	3:0	R/W	0b1111: 875mV	0b0111 (675mV)	Immediately
				0b1110: 850mV		
				0b0111: 675mV		
				0b0100: 600mV		
				0b0011: 575mV		
0x0F	Timeout	7:7	R/W	0b1: Disable Timeout	0 (Active)	Immediately
				0b0: Timeout Active		
0x10	Bus_Gain1	5:1	R/W	See Table 4	0x00 (64)	Immediately
0x11	Bus_Gain2	5:1	R/W		0x00 (64)	Immediately
0x12	Bus_Gain3	5:1	R/W		0x00 (64)	Immediately
0x13	Bus_Gain4	5:1	R/W		0x00 (64)	Immediately
0x20	Shunt_Gain1	5:1	R/W	See Table 5	0x00 (2)	Immediately
0x21	Shunt_Gain2	5:1	R/W		0x00 (2)	Immediately
0x22	Shunt_Gain3	5:1	R/W		0x00 (2)	Immediately
0x23	Shunt_Gain4	5:1	R/W		0x00 (2)	Immediately
0x24	Lock	1	R/W	Lock I ² C interface writes	0 (Not locked)	Immediately
		0	R/W	Lock I ² C interface reads / writes	0 (Not locked)	Immediately

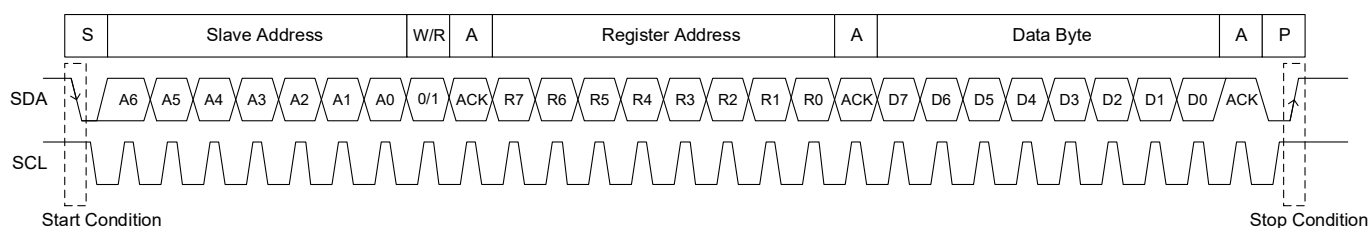


Figure 3. I²C Read/Write Protocol Format

I²C Serial Interface Description

The AOZ73456QV serial data interface works as an I²C Slave device. It supports most standard data transfer mode (100kbps) and fast transfer mode (400kbps). The serial interface provides various customizable setting of signal monitoring. A one-byte data is written by the I²C Master to the AOZ73456QV and stored in a data buffer. The content of the data buffer can also be read back by the Master. After I²C is enabled, the AOZ73456QV starts to check the address code sent by the Master every time a START condition is detected. If a valid address code, AD[6:0], is recognized, it will send out an ACK bit by pulling down on the SDA bus during the clock pulse 9 of the SCL bus. The ACK time of the clock pulse 9 of the SCL bus can be written as shown in Figure 3.

Address Mapping

The I²C address of device is configurable by set the logic states of ADDR0 and ADDR1. The table below shows the address setting corresponding to the logic states of ADDR0 and ADDR1.

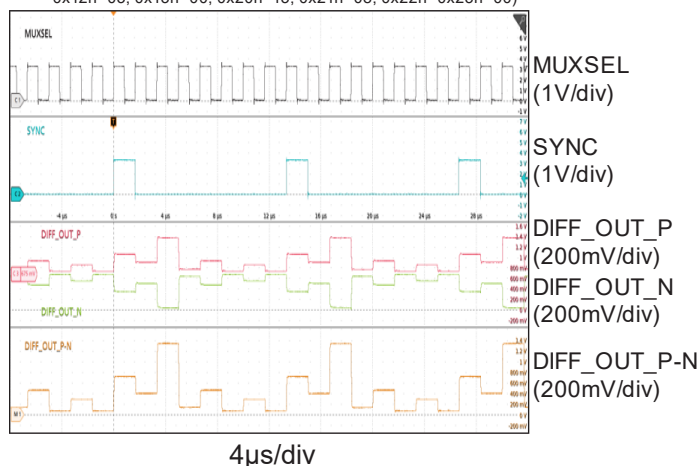
Table 1. Address Mapping

ADDR1	ADDR0	Device Address
Low	Low	34h
Low	High	35h
High	Low	36h
High	High	37h

Typical Characteristics

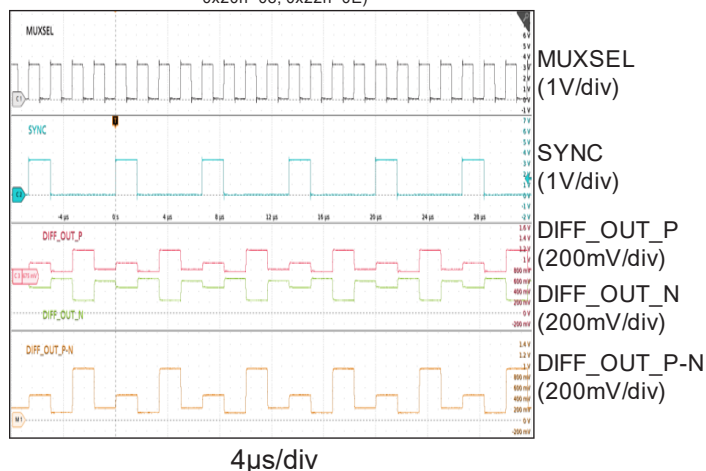
Default Operation (Active CH1 to CH4)

(BV_INx=19V, Shunt_INx_P-N=50mV, x=1-4, 0x10h=0A, 0x11h=12, 0x12h=05, 0x13h=00, 0x20h=15, 0x21h=08, 0x22h=0x23h=00)



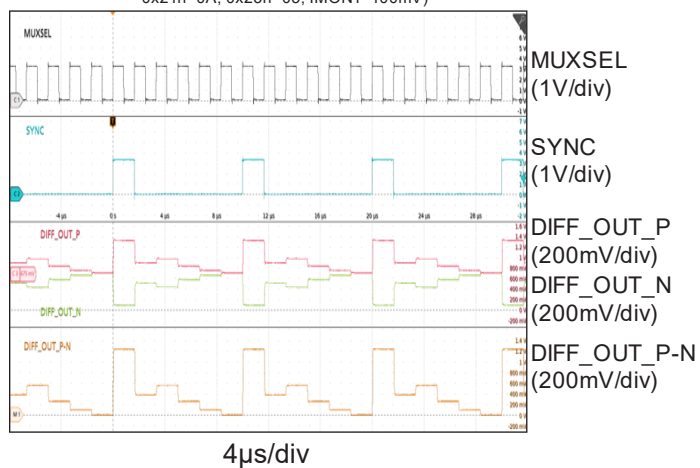
Reduce Channel (Active CH1 and CH3)

(BV_INx=19V, Shunt_INx_P-N=50mV, x=1&3, 0x10h=05, 0x12h=0D, 0x20h=08, 0x22h=0E)



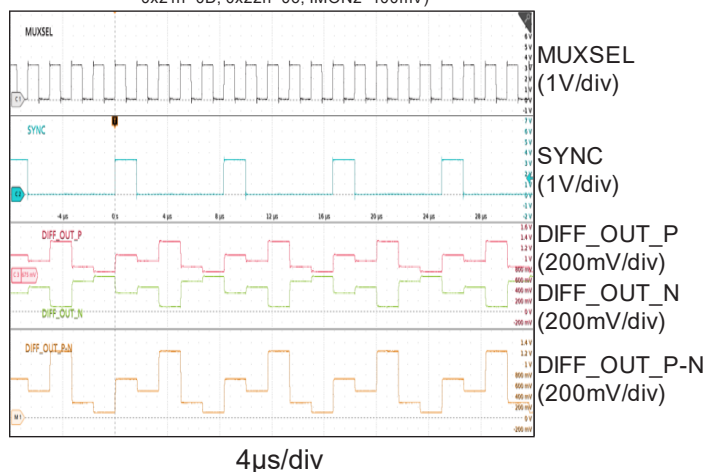
Active Ch2, CH4, IMON1, RGND

(BV_INx=19V, Shunt_INx_P-N=100mV, x=2&4, 0x11h=10, 0x13h=07, 0x21h=0A, 0x23h=05, IMON1=100mV)



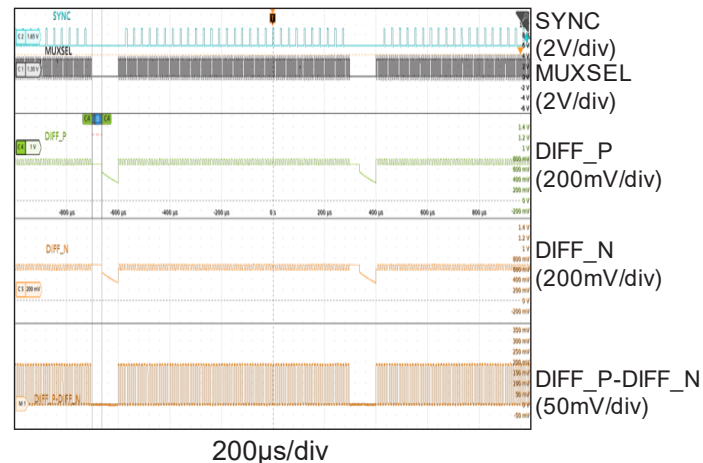
Active Ch2, CH3, IMON2

(BV_INx=19V, Shunt_INx_P-N=100mV, x=2&3, 0x11h=0A, 0x12h=10, 0x21h=0D, 0x22h=06, IMON2=100mV)



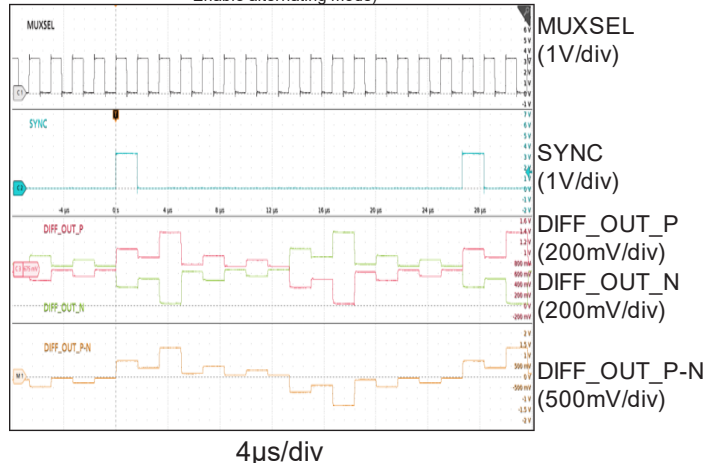
MUXSEL Timeout

(0x0Fh[7]=0b: timeout Active)



Alternating Mode

(BV_INx=19V, Shunt_INx_P-N=50mV, x=1-4, 0x10h=0A, 0x11h=12, 0x12h=05, 0x13h=00, 0x20h=15, 0x21h=08, 0x22h=0x23h=00, 0x06h[7]=1b: Enable alternating mode)



Detailed Description

Enable Control

There are three operating modes for AOZ73456QV: Full functional mode, limited function mode, and standby mode. The descriptions of these 3 modes are provided in the table below:

Table 2. EN_B Logic for Operating Modes

EN_B	Mode	Description
Low	Full Functional Mode	Fully functional for all functions.
Tri-state	Limited Function Mode	Only BV_OK indicator is functional, others are turned off. Diff_out remains in Hi-Z. MUX_SEL is suggested not provide.
High	Standby Mode	All functions are turned off.

Power Sequence

When VCC rises above the POR threshold, the BV_OK function activates. A 1ms delay after the POR is required before writing to the I²C register. The EN_B state should be changed only after the VCC and the bus voltages are stable. When switching to full functional mode, a 40μs delay time is necessary before starting to send MUX_SEL. During operation, the I²C writes can be performed at any time, and the new register setting will be valid in the next multiplexer sequence.

Band-gap Reference Output (VBG) & BV_REF

A 1.3V high-accuracy band-gap voltage is provided at the VBG pin for users to set the BV_OK reference. To ensure stable VBG operation, a 100nF low ESR bypass capacitor (preferably a MLCC) is required. The BV_OK reference can be derived either from a voltage divider connected to the VBG pin or from external voltage sources.

Bus Voltage OK Indication (BV_OK)

The BV_OK pin offers an open-drain output which requires a pull-up resistor. The BV_OK threshold is set by BV_REF pin. The internal BV_OK comparator has built in hysteresis of 10% to prevent chatter as bus voltage come up. When all monitored bus voltages exceed the user-defined threshold, the BV_OK is pulled high. User can use the SKIP pin to modify the logic as shown in Table 3. The SKIP pin is used to provide power to hold BV_OK low in the absence of VCC.

Table 3. Operating Modes Table

VCC	EN_B	BV_IN(x)	SKIP	BV_OK	Operating Mode
L	L	x	L	Open drain	(No power)
L	L	x	H	L	SKIP pin provides power to hold BV_OK low
H	H	x	L	Open drain	Standby mode
H	H	x	H	L	Standby mode
H	L	L	H	L	Fully functional mode
H	Hi-Z	L	H	L	Limited function mode
H	L	H	H	Open drain	Fully functional mode
H	Hi-Z	H	H	Open drain	Limited function mode
H	L	x	L	Open drain	Fully functional mode
H	Hi-Z	x	L	Open drain	Limited function mode

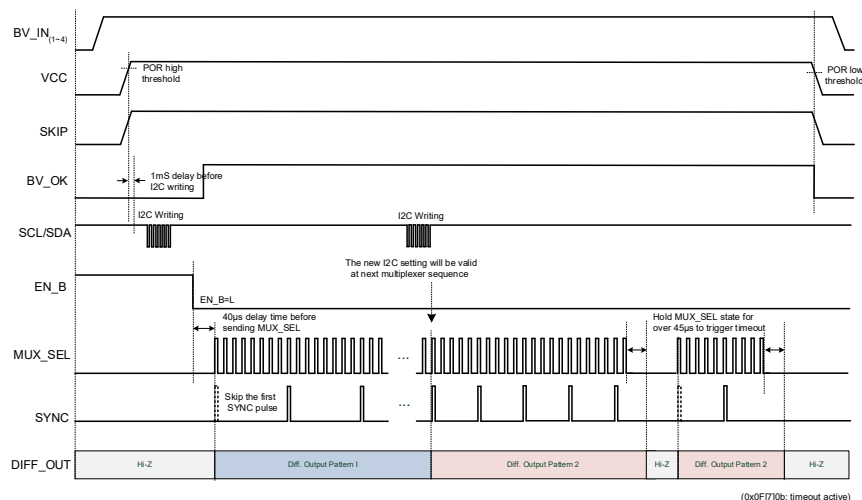


Figure 4. Power Sequence

Bus Voltage Monitor

The BV_IN pins should be connected to their respective target bus for bus voltage monitoring. A RC low pass filter between BV_IN and monitored bus is recommended to ensure stable operation without noise coupling. The sensed bus voltage is scaled by the internal voltage divider. Its ratio can be programmed from 1/4 to 1/64 by I²C register and fed to the multiplexer. Table 4 shows the configurable bus voltage gains and its corresponding I²C register setting. In bus voltage cycles of multiplexer sequence, the voltage of output differential amplifier represents the scaled bus voltage signal, which can be calculated by the following formula:

$$V_{\text{Diff_OUT_BV}} = \frac{V_{\text{BUS}}}{\text{Bus Gain}} \quad (1)$$

Shunt Current Monitor

The bus current is sensed by an external shunt resistor. The positive and negative node of the shunt resistor comes in a pair pin to SC_IN_P and SC_IN_N. The differential input SC_IN_P should be connected to the same node as BV_IN. Note that the PCB routing between external shunt resistor to SC_IN_P and SC_IN_N pins should be Kelvin connection. A differential RC low pass filter between SC_IN_P/N to the sensed nodes of shunt resistor is recommended to ensure stable operation without noise coupling. The sensed voltage across shunt resistor is converted into a single-ended signal by an internal high-accuracy current sense amplifier and scaled according to the shunt current gain configured via I²C register before being fed to the multiplexer. Table 5 shows the configurable shunt current gains and their corresponding I²C register setting.

Table 4. Bus Voltage Gain

Bit[5:1]	Hex (include bit 0)	Bus Gain	Bit[5:1]	Hex (include bit 0)	Bus Gain
00000	0x00	64.000	10000	0x20	15.300
00001	0x02	58.524	10001	0x22	13.991
00010	0x04	53.517	10010	0x24	12.794
00011	0x06	48.939	10011	0x26	11.700
00100	0x08	44.752	10100	0x28	10.699
00101	0x0A	40.923	10101	0x2A	9.783
00110	0x0C	37.422	10110	0x2C	8.946
00111	0x0E	34.220	10111	0x2E	8.181
01000	0x10	31.292	11000	0x30	7.481
01001	0x12	28.615	11001	0x32	6.841
01010	0x14	26.167	11010	0x34	6.256
01011	0x16	23.928	11011	0x36	5.720
01100	0x18	21.881	11100	0x38	5.231
01101	0x1A	20.009	11101	0x3A	4.783
01110	0x1C	18.297	11110	0x3C	4.374
01111	0x1E	16.732	11111	0x3E	4.000

Note: Bit[7:6] and Bit[0] are 0

Table 5. Shunt Current Gain

Bit[5:1]	Hex (include bit 0)	Shunt Gain	Bit[5:1]	Hex (include bit 0)	Shunt Gain
00000	0x00	2.000	10000	0x20	7.212
00000	0x02	2.167	10001	0x22	7.813
00010	0x04	2.348	10010	0x24	8.465
00011	0x06	2.544	10011	0x26	9.172
00100	0x08	2.756	10100	0x28	9.937
00101	0x0A	2.986	10101	0x2A	10.767
00110	0x0C	3.235	10110	0x2C	11.665
00111	0x0E	3.505	10111	0x2E	12.639
01000	0x10	3.798	11000	0x30	13.694
01001	0x12	4.115	11001	0x32	14.837
01010	0x14	4.458	11010	0x34	16.075
01011	0x16	4.830	11011	0x36	17.417
01100	0x18	5.233	11100	0x38	18.870
01101	0x1A	5.670	11101	0x3A	20.445
01110	0x1C	6.143	11110	0x3C	22.151
01111	0x1E	6.656	11111	0x3E	24.000

Note: Bit[7:6] and Bit[0] are 0

In shunt current cycles of multiplexer sequence, the voltage of output differential amplifier represents the scaled shunt current signal, which can be calculated by the following formula:

$$V_{\text{Diff_OUT_SC}} = I_{\text{BUS}} \cdot R_{\text{Shunt}} \cdot \text{Shunt Gain} \quad (2)$$

IMON

Two IMON inputs are supported for monitoring two voltage regulators. The monitored IMON signal is directly sent to multiplexer via a unity gain buffer. In IMON cycles of multiplexer sequence, the voltage of output differential amplifier represents the input IMON voltage.

Reference Ground (Calibration Cycle)

If bit 7 of register 0x04 is set to 1, a calibration cycle will be added to the end of the multiplexer sequence. The differential output voltage during calibration cycle indicates the offset error of the differential amplifier, which is used for offset cancellation if required.

Differential Output Amplifier

The input information mentioned above (bus voltages, shunt currents, IMONs and calibration cycle) is sequentially delivered to the DIFF_OUT_P and DIFF_OUT_N pins via the multiplexer. The common-mode voltage of the differential output amplifier is configurable from 575mV to 875mV in 25mV/step via the I²C register (0x08h) to offer flexibility for the ADC to read differential outputs. The offset of the differential output can also be programmable from 0mV to -375mV in 25mV/step via the I²C register (0x07h). The output differential amplifier is capable of driving a load range of R = 0.86~8.6Ω and C = 8.2~82pF, which can represent a lumped equivalent impedance from board and GPU package traces.

Multiplexer Sequence

The multiplexer selection is managed by a single digital control input at MUX_SEL pin. The differential amplifier cyclically outputs the monitored signals in a fixed sequence as Figure 5. The sequence is repeated until a timeout event occurs or the device is disabled. Register 0x04 configures the enable/disable settings for each channel's monitoring. Channels that are disabled will not be included in the multiplexer sequence.

SYNC Signal

A SYNC pulse is simultaneously output with the first cycle of each multiplexer sequence for synchronization. As shown in

Figure 6, the SYNC pulse for the first multiplexer sequence is skipped, while SYNC pulses for subsequent multiplexer sequences are continuously output until interrupted.

Alternating Polarity Mode

Users can enable the alternating polarity mode by configuring I²C register 0x06 to 80h. This mode adds extra reversed polarity output cycles at the end of multiplexer sequence. As shown in Figure 7, a sequence of reversed polarity output cycles is continually delivered after the standard polarity output cycles. In this mode, the SYNC pulses are simultaneously output with the first standard polarity cycle of each multiplexer sequence.

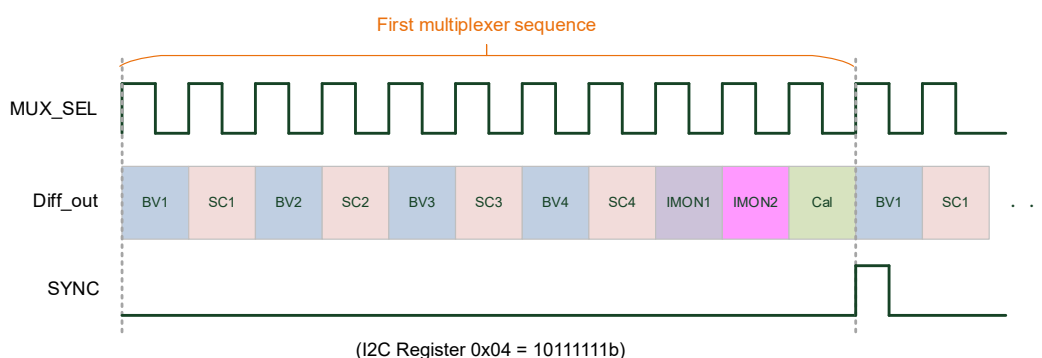


Figure 5. An Example for Single Device Mode Operating

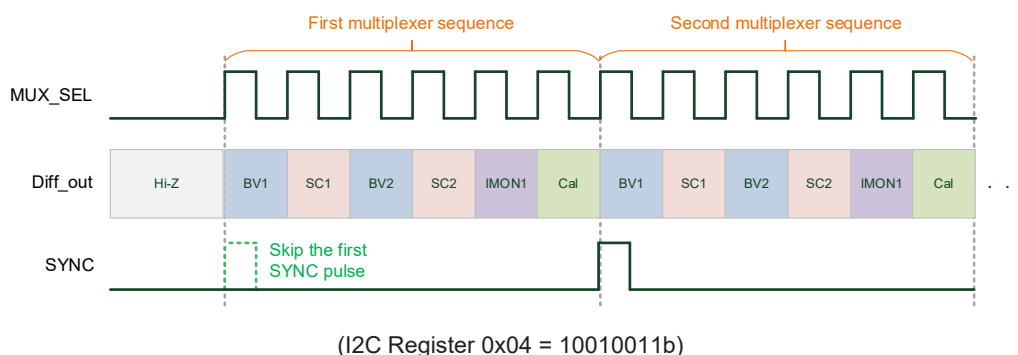


Figure 6. Skip First SYNC Pulse

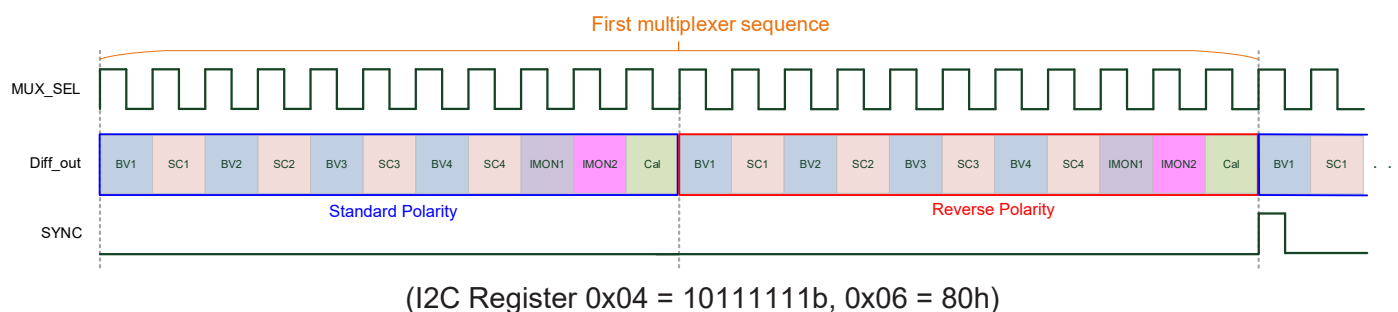


Figure 7. An Example for Single Device Mode + Alternating Polarity Mode

With the reversed polarity output cycles, users can cancel the differential output amplifier offset by calculating half of the difference between the standard and reversed cycles. Assuming the input signal from multiplexer is V_M and the offset of differential output amplifier is V_{OFST} , the output voltages of standard polarity and reversed polarity can be represented by following equations:

$$V_{Diff_OUT_Standard} = V_M + V_{OFST} \quad (3)$$

$$V_{Diff_OUT_Reversed} = (-V_M) + V_{OFST} \quad (4)$$

The accurate output voltage with the differential amplifier offset canceled is:

$$V_{Diff_OUT_Accurate} = \frac{V_{Diff_OUT_Standard} - V_{Diff_OUT_Reversed}}{2} = V_M \quad (5)$$

Single-Device Mode and Dual-Device Mode

If the number of monitored bus channels less than 4 and the number of the monitored IMON is less than 2, only one device is needed, which is referred to as single-device mode. To monitor additional channels, user can connect two devices

together and configure the I²C register settings to operate in dual-device mode, as detailed in the Typical Application section. The settings for each mode are described as below:

1. Single-Device Mode:

In single device mode, no pulses need to be skipped. Register 0x05 must be set to 0h. All other settings can be referenced to the relevant sections in this datasheet.

2. Dual-Device Mode

In dual-device mode, one device operates as device-A and the other as device-B. The differential output cycles of device-A are always preceded those of device-B. To enable separate I²C communication, device-A and device-B must be assigned to different addresses. Configure device-A register 0x05[3:0] to set the pulse number to skip at the end of the MUX_SEL cycles, which the number of skipped pulses should match the output cycle counts of device-B. Similarly, configure device-B register 0x05[7:4] to set the pulse number to skip at the beginning of the MUX_SEL cycles, which the number of skipped pulses should match the output cycle counts of device-A. This configuration ensures that the output cycles of device-A and device-B are complementary, as illustrated in Figure 8.

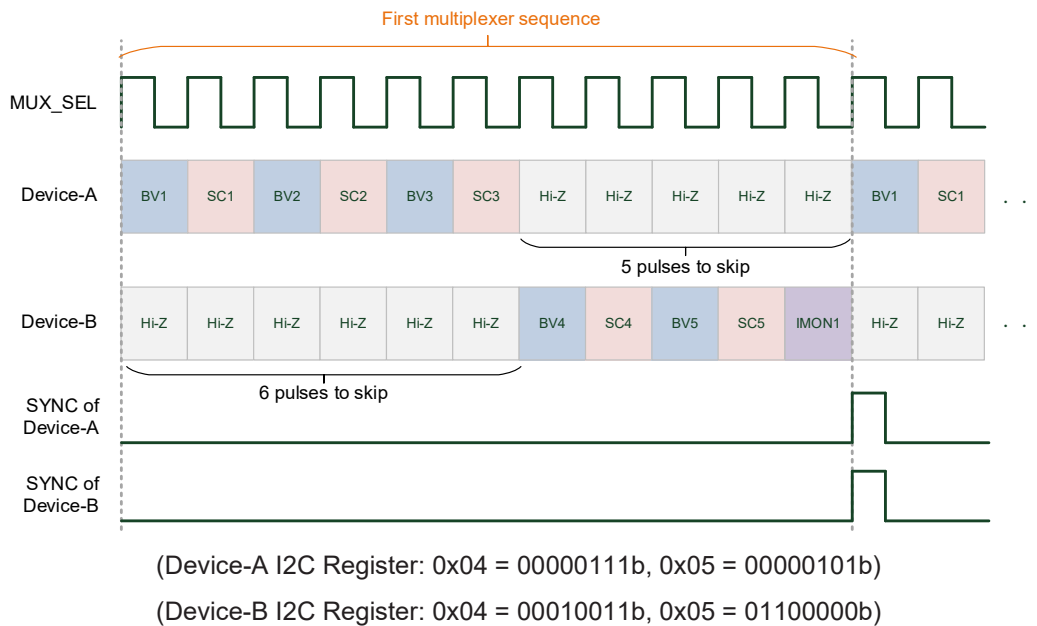


Figure 8. An Example for Dual-Device Mode

If the alternating polarity mode is required in dual-device mode, the register 0x06 of both devices must be set to 80h. Figure 9 illustrates an example of enabling alternating polarity mode in dual-device mode.

To correctly operates in dual-device mode, the register settings for Diff_Amp_Offset (0x07), Diff_Amp_CM (0x08), Alternating_Polarity_Mode (0x06), and Timeout (0x0F) must be matched between two devices. Table 6 (below) shows an example of I²C register setting for dual-device mode.

Timeout and Reset

If timeout is enabled by configuring the I²C register, a timeout event will be triggered when MUX_SEL state is held for more than 45μs. This timeout event will stop the output of Diff_out_P and Diff_out_N, setting their state to high output impedance. Additionally, the timeout event will reset MUX_SEL cycles to the initial state.

Connection for Unused Channels

All unused channels should be disabled by setting its corresponding register and be connected as below rules:

BV_IN_(x): Connect to any active BV_IN node.

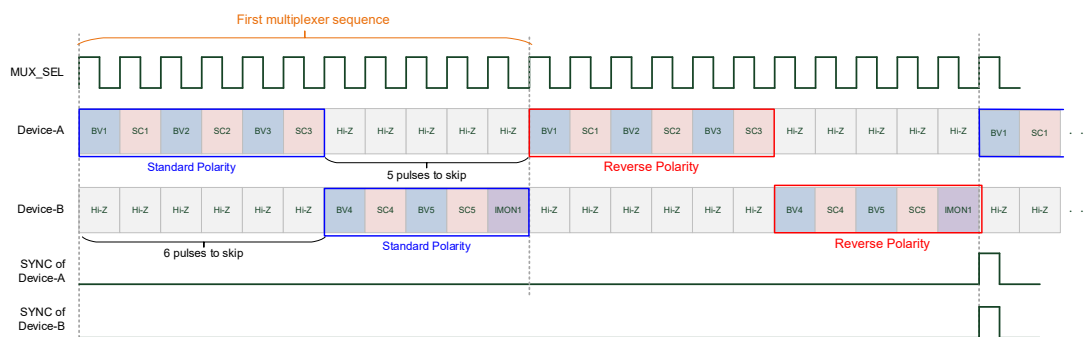
SC_IN_P_(x): Connect to any active BV_IN node.

SC_IN_N_(x): Connect to the same potential as SC_IN_P_(x).

IMON_(x): Short to ground.

SYNC: Left in floating.

Note that for each unused channel x, its BV_IN(x), SC_IN_P(x), and SC_IN_N(x) should be tied to the same voltage node.



(Device-A I²C Register: 0x04 = 00000111b, 0x05 = 00000101b, 0x06 = 80h)

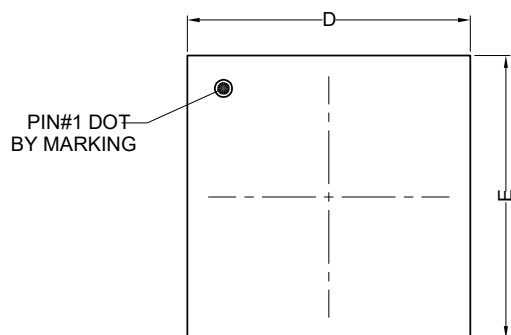
(Device-B I²C Register: 0x04 = 00010011b, 0x05 = 01100000b, 0x06 = 80h)

Figure 9. An Example for Dual-Device Mode + Alternating Polarity Mode

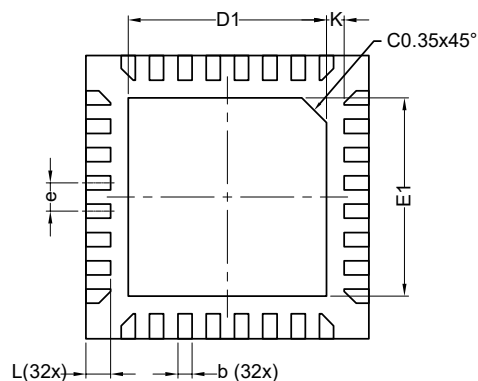
Table 6. An Example of I²C Register Setting for Dual-Device Mode

I ² C Register	The device-A reports bus channel 1, 2, and 3 (total 6 output cycles) The device-B reports bus channel 4, 5, and IMON1 (total 5 output cycles) Differential amplifier offset = -350mV Differential amplifier common mode voltage = 675mV					
	Active_Channel	MUX_SEL_Skip	Alternating_Polarity_Mode	Diff_Amp_Offset	Diff_Amp_CM	Timeout
	0x04	0x05	0x06	0x07	0x08	0x0F
Device-A	07h	05h	80h	0Eh	07h	0h
Device-B	13h	60h	80h	0Eh	07h	0h
Note	Set skipped cycles to make 2 device output cycles complementary These settings must be match between 2 devices					

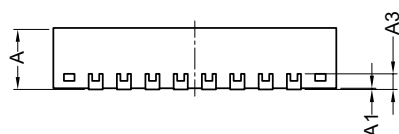
Package Dimensions, QFN4x4-32L



TOP VIEW

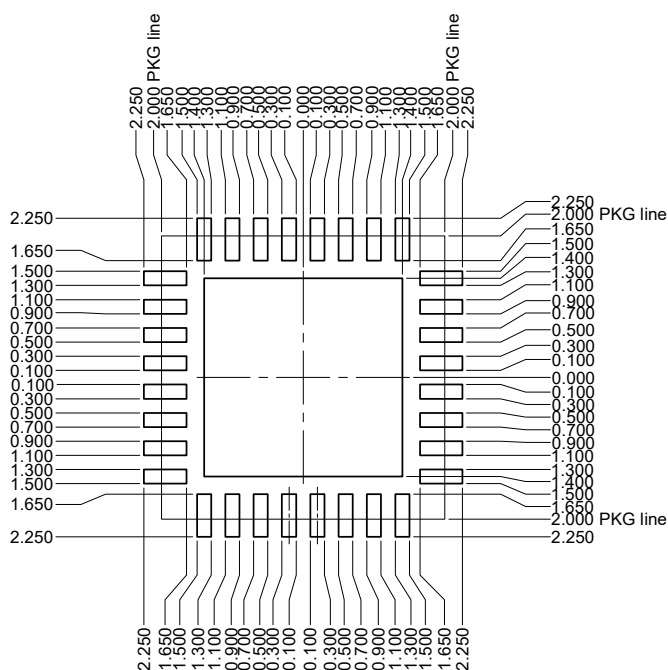


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



UNIT: mm

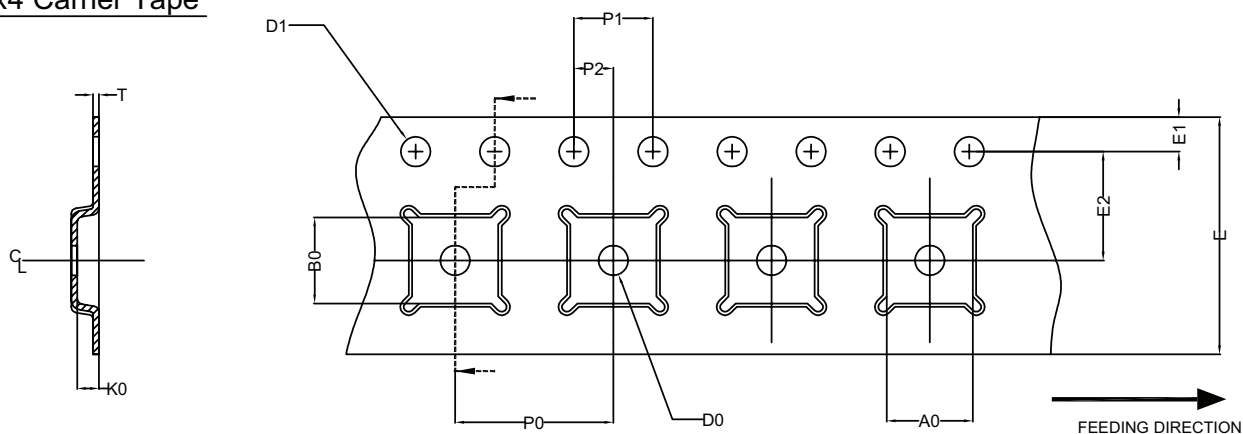
SYMBOLS	DIM. IN MILLIMETERS			DIM. IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	-	0.05	0.000	-	0.002
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.90	4.00	4.10	0.154	0.157	0.161
D1	2.70	2.80	2.90	0.106	0.110	0.114
E	3.90	4.00	4.10	0.154	0.157	0.161
E1	2.70	2.80	2.90	0.106	0.110	0.114
e	0.40 BSC			0.016 BSC		
L	0.25	0.35	0.45	0.010	0.014	0.018
K	0.25 REF.			0.010 REF.		

NOTE:

1. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN4x4-32L

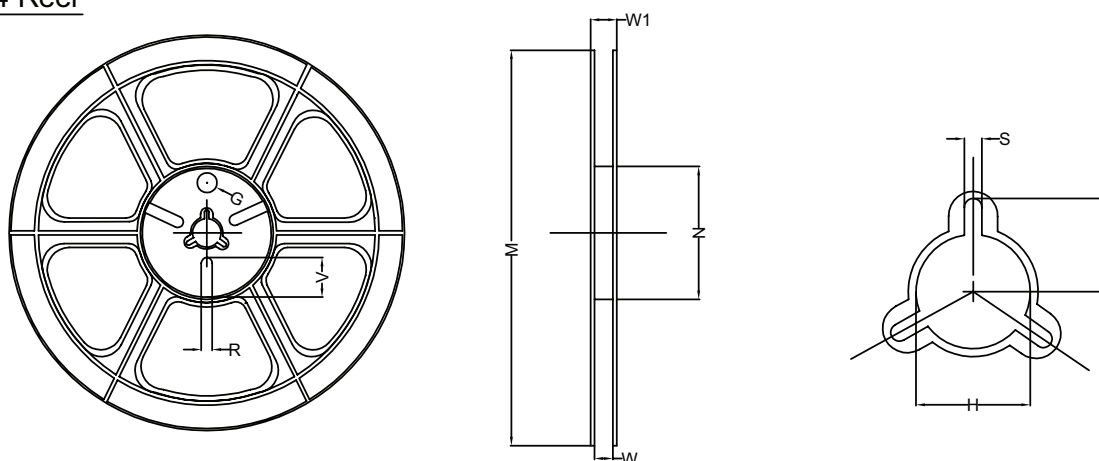
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 -0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN4x4 Reel



UNIT: MM

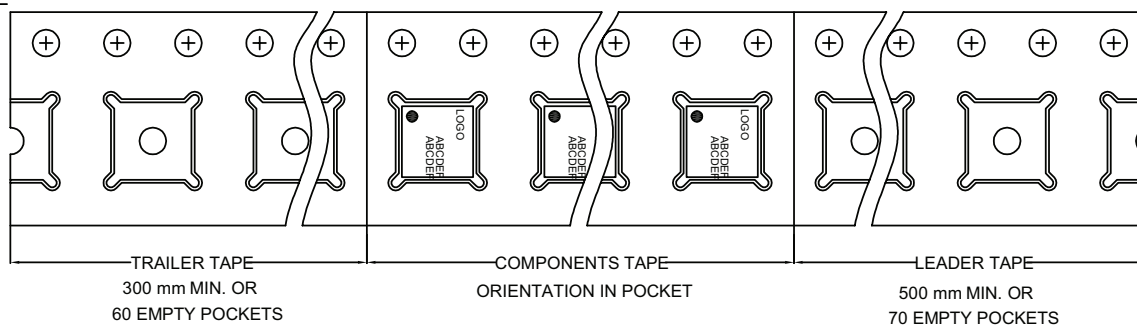
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.0 ±2.0	Ø79.0 ±1.0	12.4 +2.0 -0.0	17.0 +2.6 -1.2	Ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape

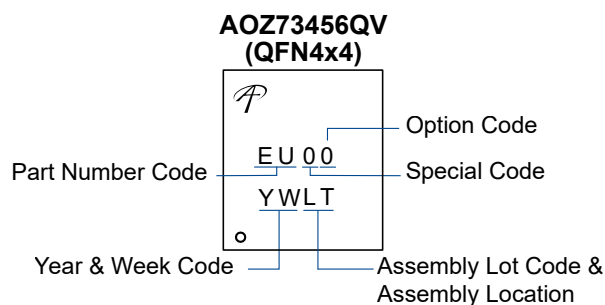
Leader / Trailer
& Orientation

Normal

Unit Per Reel:
3000pcs



Part Marking



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