ALPHA & OMEGA SEMICONDUCTOR

AOFE035V10GA1

100V GaN Enhancement-mode Power Transistor

Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra low On-resistance
- Very small footprint

Applications

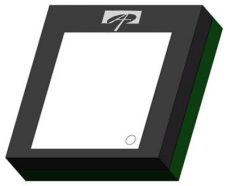
- High frequency DC/DC converter
- High density DC/DC power module
- Synchronous rectification
- Motor driver

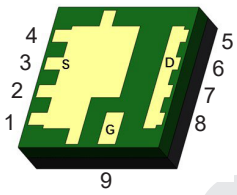
Product Summary at T_J = 25°C

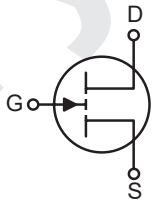
$V_{DS,\ max}$	100V
$R_{DS(on),\ max}$ @ V_{GS} = 5V	3.5mΩ
$Q_{g,\ typ}$ @ V_{DS} = 50V	7.6nC
$I_{DS,\ pulse}$	230A
Q_{OSS} @ V_{DS} = 50V	42nC

RoHS Compliant

Pin Configuration







Pin Information

Gate	Drain	Source
9	5-8	1, 2, 3, 4

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AOFE035V10GA1	En-FCLGA 3.3mm×3.3mm	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter		AOFE035V10GA1	Units
V_{DS}	Drain-source voltage	Continuous	100	V
$V_{DS(tr)}$	Drain-source voltage transient (1)	V_{GS} = 0V , 1h total time, T_A = T_{JMAX}	120	V
I_D	Continuous current	V_{GS} = 5V, T_C = 25°C, $R_{\theta JC}$ = 0.49°C/W	201	A
		V_{GS} = 5V, T_C = 100°C, $R_{\theta JC}$ = 0.49°C/W	127	
		V_{GS} = 5V, T_A = 25°C, $R_{\theta JA}$ = 62.41°C/W (2)	17.8	
	Pulsed	T_J = 25°C, T_{PULSE} = 300µs	230	
V_{GS}	Gate-source voltage		6	V
	Gate-source voltage		-4	
T_J	Operating temperature		-40 to 150	°C
T_{STG}	Storage temperature		-40 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Note	Units
$R_{\theta JC}$	Thermal resistance junction-to-case	0.49		°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board	4.16		°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient (3)	62.41		°C/W
	Thermal resistance junction-to-ambient (4), without heat sink	33.61		
	Thermal resistance junction-to-ambient (5), with 12.25cm^2 heat sink	26.22		
T_{sold}	Maximum reflow soldering temperature	260	MSL3	°C

Electrical Characteristics

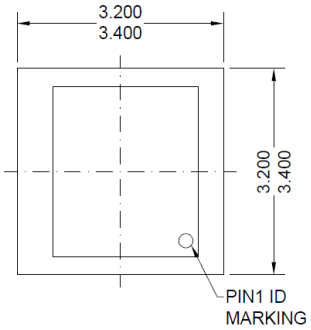
(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
I_{DSS}	Drain-source leakage current	V_{DS} = 100V, V_{GS} = 0V		1	100	µA
I_{GSS}	Gate-to-source forward leakage	V_{GS} = 6V		0.5	100	µA
	Gate-to-source reverse leakage	V_{GS} = -4V		0.1	100	
$V_{GS(TH)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 7.6mA	0.8	1.1	2.1	V
$R_{DS(on)}$	Drain-source On-state resistance (5)	V_{GS} = 5V, I_D = 25A		2.9	3.5	mΩ
V_{SD}	Source-drain forward voltage	V_{GS} = 0V, I_S = 0.5A		1.3		V
DYNAMIC						
C_{ISS}	Input capacitance	V_{DS} = 50V, V_{GS} = 0V		905		pF
C_{OSS}	Output capacitance	V_{DS} = 50V, V_{GS} = 0V		425		
C_{RSS}	Reverse transfer capacitance	V_{DS} = 50V, V_{GS} = 0V		7		
$C_{OSS(ER)}$	Energy related C_{OSS}	V_{DS} = 0V to 50V, V_{GS} = 0V		595		
$C_{OSS(TR)}$	Time related C_{OSS}	V_{DS} = 0V to 50V, V_{GS} = 0V		835		
R_G	Gate resistance	f = 5MHz, open drain		1.5		Ω
Q_G	Total gate charge	V_{DS} = 50V, V_{GS} = 5V, I_D = 25A		7.6		nC
Q_{GS}	Gate-to-source charge	V_{DS} = 50V, I_D = 25A		1.6		
Q_{GD}	Gate-to-drain charge	V_{DS} = 50V, I_D = 25A		1.5		
$Q_{GD(TH)}$	Gate charge at threshold	V_{DS} = 50V, I_D = 25A		0.9		
Q_{OSS}	Output charge	V_{DS} = 50V, V_{GS} = 0V		42		
Q_{rr}	Reverse recovery charge	V_{DS} = 50V, I_S = 25A		0		

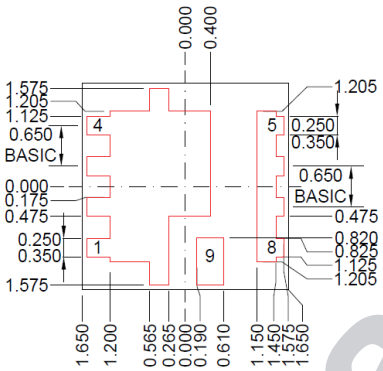
Notes:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.
2. Device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.
3. $R_{\theta ja}$ is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.
4. Device on 60mm*36mm*1.6mm PCB FR4 with four layers, 2 oz copper.
5. Device on 60mm*36mm*1.6mm PCB FR4 with four layers, 2 oz copper. The heat sink (35mm*35mm*15mm) is vertically placed on the top of the device.
6. $R_{DS(on)}$ is measured without prior drain bias or switching stress.

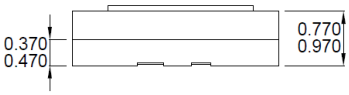
Package Dimensions, En-FCLGA 3.3mm×3.3mm



TOP VIEW



BOTTOM VIEW

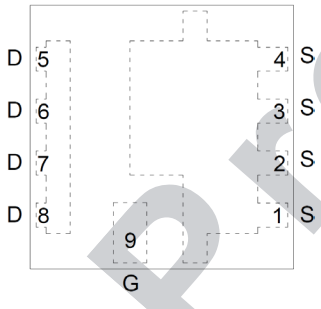


SIDE VIEW

NOTE:

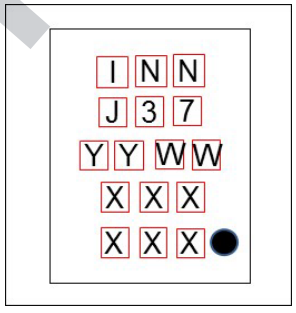
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

PIN configuration



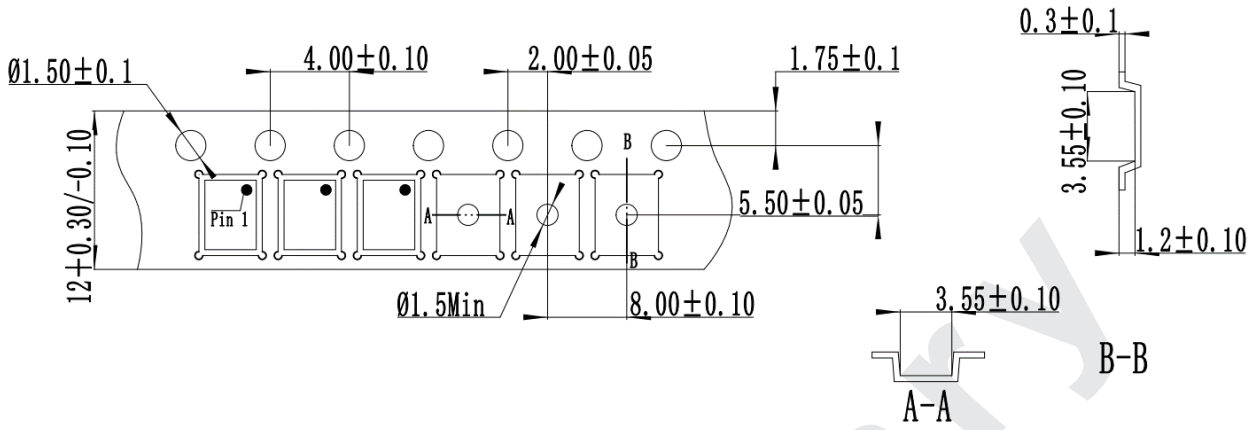
Top View

Marking Reference

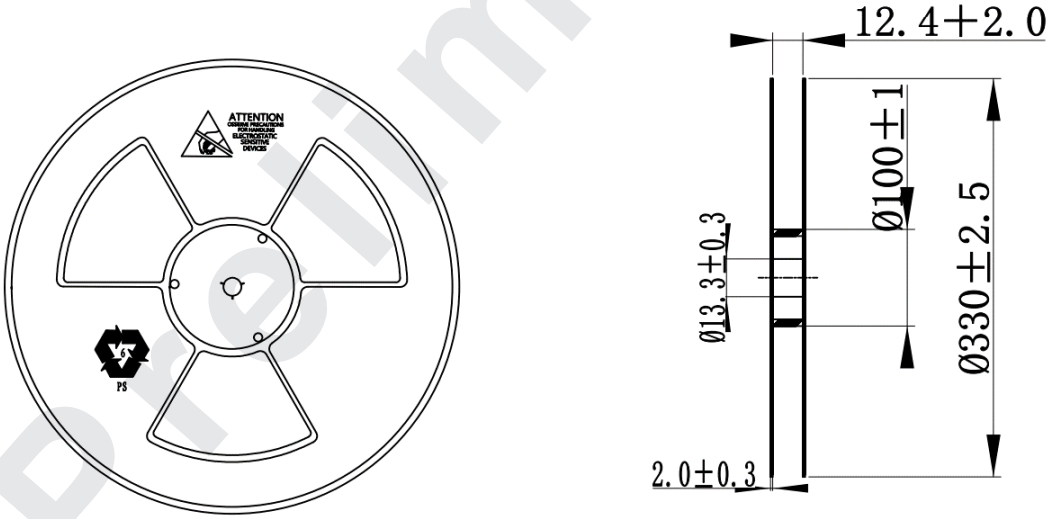


Row	Description	Example
Row 1	Company Name	INN
Row 2	Product Code	J37
Row 3	Date code	YYWW
Row 4	Lot code	XXX
Row 5		XXX

Tape and Reel Dimensions, En-FCLGA 3.3mm×3.3mm



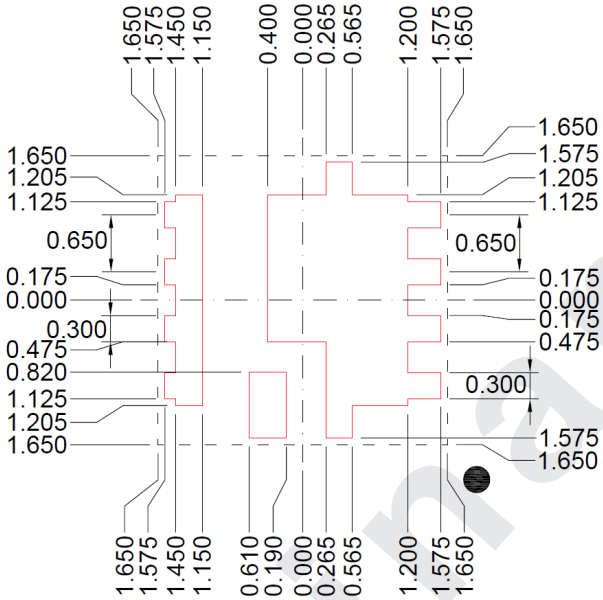
Notes:
(1)The cumulative error of any 10 sprocket holes shall not exceed ± 0.20mm;
(2)The material thickness shall be measured based on the edge of the carrier tape;
(3)The unspecified tolerance is ± 0.1mm, and R<0.3mm is not specified;
(4)The unmarked demolding slope is 5 ° ;
(5)Surface Resistivity: 1*10 e 5 Ω/Δ~ 1*11 e11



Notes:
1、The surface of the product should be smooth, clean, and free of injection molding defects, and there should be no significant burrs;
2、Material surface resistance:1*10e5Ω/Δ~1*10e10Ω/Δ;
3、No tolerance marked: ±0.3mm;

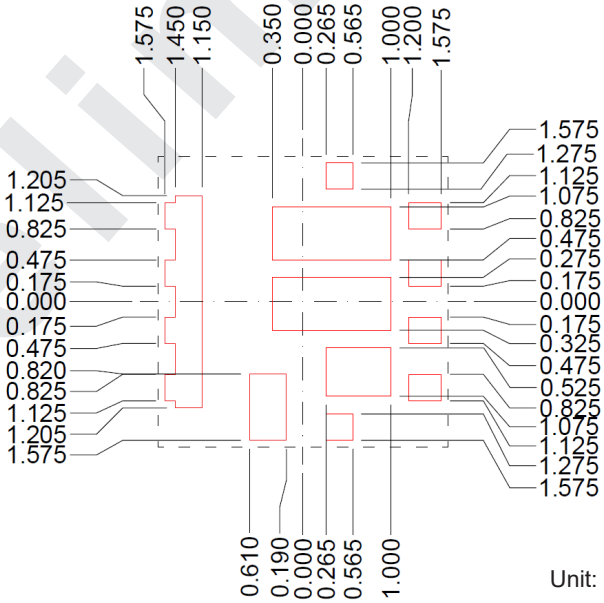
Land Pattern, En-FCLGA 3.3mm×3.3mm

Recommended land pattern



Unit: mm

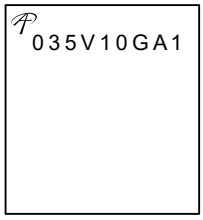
Recommended Stencil drawing



Unit: mm

Part Marking

AOFE035V10GA1



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