ALPHA & OMEGA SEMICONDUCTOR

AOFG018V10GA1

100V GaN Enhancement-mode Power Transistor

Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra low On-resistance
- Very small footprint

Applications

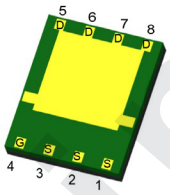
- High frequency DC/DC converter
- High density DC/DC power module
- Synchronous rectification
- Motor driver

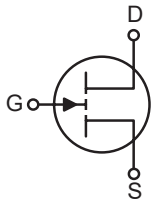
Product Summary at T_J = 25°C

$V_{DS,\ max}$	100V
$R_{DS(on),\ max}$ @ V_{GS} = 5V	1.8mΩ
$Q_{g,\ typ}$ @ V_{DS} = 50V	19nC
$I_{DS,\ pulse}$	580A
Q_{OSS} @ V_{DS} = 50V	100nC

RoHS Compliant

Pin Configuration





Pin Information

Gate	Drain	Source
4	5-8	1, 2, 3

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AOFG018V10GA1	En-FCLGA 5mm×6mm	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter		AOFG018V10GA1	Units
V_{DS}	Drain-source voltage		100	V
$V_{DS(tr)}$	Drain-source voltage transient (1)	V_{GS} = 0V , 1h total time, $T_A = T_{JMAX}$	120	V
I_D	Continuous current	V_{GS} = 5V, T_C = 25°C, $R_{\theta JC}$ = 0.2°C/W	495	A
		V_{GS} = 5V, T_C = 100°C, $R_{\theta JC}$ = 0.2°C/W	313	
		V_{GS} = 5V, T_A = 25°C, $R_{\theta JA}$ = 38.1°C/W	35	
	Pulsed	T_J = 25°C, T_{PULSE} = 300µs	580	
V_{GS}	Gate-source voltage		6	V
	Gate-source voltage		-4	
P_{tot}	Power dissipation	V_{GS} = 5V, T_C = 25°C, $R_{\theta JC}$ = 0.2°C/W	442	W
		V_{GS} = 5V, T_A = 25°C, $R_{\theta JA}$ = 38.1°C/W	2.2	
T_J	Operating temperature		-40 to 150	°C
T_{STG}	Storage temperature		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Note	Units
$R_{\theta JC}$	Thermal resistance junction-to-case	0.2		°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board	2.2		°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient (2)	38.1		°C/W
T_{sold}	Maximum reflow soldering temperature	260	MSL3	°C

Electrical Characteristics

(T_J = 25°C, unless otherwise noted)

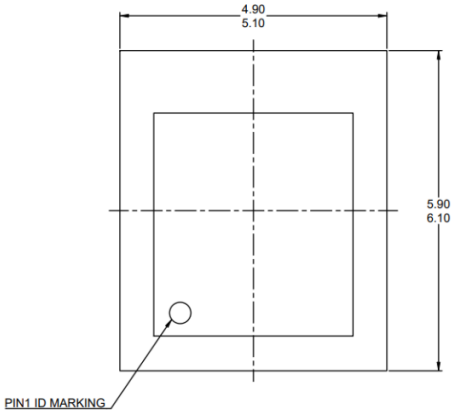
Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
I_{DSS}	Drain-source leakage current	V_{DS} = 100V, V_{GS} = 0V		2.5	200	µA
		V_{DS} = 100V, V_{GS} = 0V, T_J = 125°C		500		
I_{GSS}	Gate-to-source forward leakage	V_{GS} = 6V		2	200	µA
		V_{GS} = 6V, T_J = 125°C		50		
	Gate-to-source reverse leakage	V_{GS} = -4V		0.1	200	
$V_{GS(TH)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 19mA	0.9	1.1	2.1	V
$R_{DS(on)}$	Drain-source On-state resistance (3)	V_{GS} = 5V, I_D = 50A		1.5	1.8	mΩ
V_{SD}	Source-drain forward voltage	V_{GS} = 0V, I_S = 5A		1.8		V
DYNAMIC (4)						
C_{ISS}	Input capacitance	V_{DS} = 50V, V_{GS} = 0V		2350		pF
C_{OSS}	Output capacitance	V_{DS} = 50V, V_{GS} = 0V		1010		
C_{RSS}	Reverse transfer capacitance	V_{DS} = 50V, V_{GS} = 0V		14		
$C_{OSS(ER)}$	Energy related C_{OSS}	V_{DS} = 0V to 50V, V_{GS} = 0V		1415		
$C_{OSS(TR)}$	Time related C_{OSS}	V_{DS} = 0V to 50V, V_{GS} = 0V		2000		
R_G	Gate resistance	f = 5MHz, open drain		0.73		Ω
Q_G	Total gate charge	V_{DS} = 0V to 50V, V_{GS} = 5V, I_D = 50A		19		nC
Q_{GS}	Gate-to-source charge	V_{DS} = 0V to 50V, V_{GS} = 5V, I_D = 50A		4.2		
Q_{GD}	Gate-to-drain charge	V_{DS} = 0V to 50V, V_{GS} = 5V, I_D = 50A		3		
V_{Plat}	Gate plateau voltage	V_{DS} = 50V, V_{GS} = 0V to 5V, I_D = 50A		1.9		V
$Q_{GD(TH)}$	Gate charge at threshold	V_{DS} = 0V to 50V, V_{GS} = 5V, I_D = 50A		2.4		nC
Q_{OSS}	Output charge	V_{DS} = 0V to 50V, V_{GS} = 0V		100		
Q_{rr}	Reverse recovery charge	V_{DS} = 50V, I_S = 50A		0		

Notes:

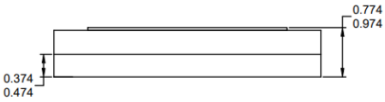
1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.
2. $R_{\theta ja}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.
3. $R_{DS(on)}$ is measured without prior drain bias or switching stress.
4. Guaranteed by design.

Package Dimensions, En-FCLGA 5mm×6mm

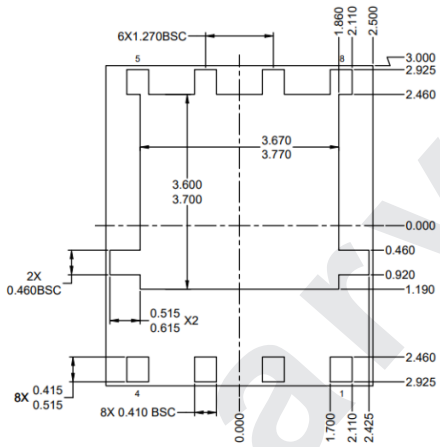
Package Reference



TOP VIEW



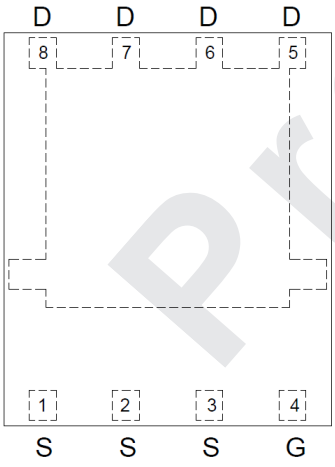
SIDE VIEW



BOTTOM VIEW

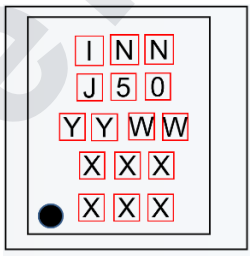
NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Pin Configuration:



TOP VIEW

Marking Reference:

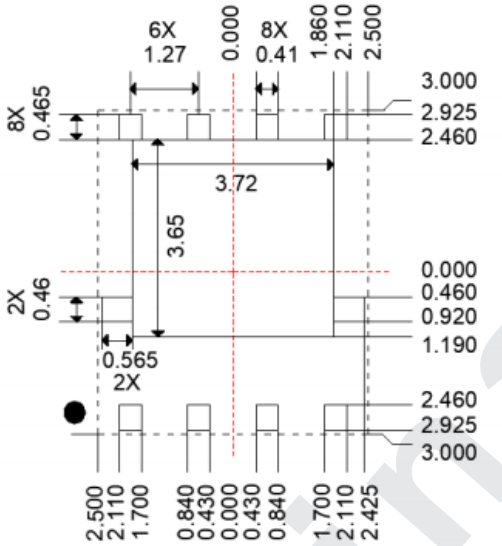


TOP-Side View

Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Date code	YYWW
Row4	Lot ID	XXX
Row5	Lot ID+Subcon	XXX

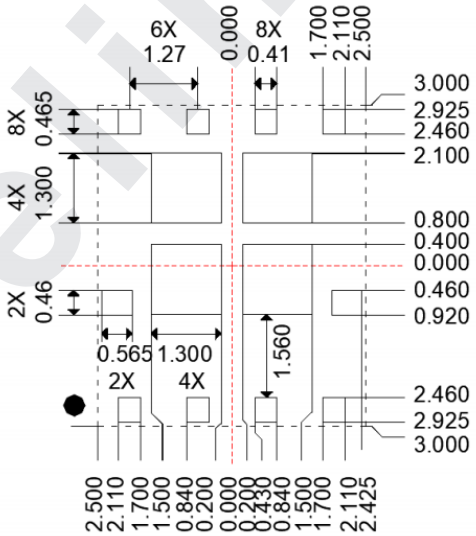
Land Pattern, En-FCLGA 5mm×6mm

Recommended Land Pattern



Unit: mm

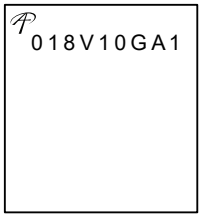
Recommended Stencil Drawing



Unit: mm

Part Marking

AOFG018V10GA1



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.