ALPHA & OMEGA SEMICONDUCTOR

AOFQ018V10GA1

100V GaN Enhancement-mode Power Transistor

Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small footprint

Applications

- High frequency DC-DC converter
- Point of Load
- RF envelope tracking
- PC charger
- Mobile power bank
- Motor driver

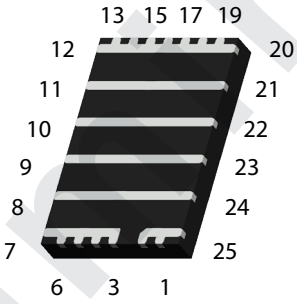
Product Summary at T_J = 25°C

$V_{DS, max}$	100V
$R_{DS(on), max}$ @ V_{GS} = 5V	1.8mΩ
$Q_{g, typ}$ @ V_{DS} = 50V	22nC
$I_{D, pulse}$	320A
Q_{oss} @ V_{DS} = 50V	125nC

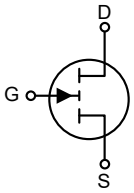
GREEN Product

Pin Configuration

Top View



Bottom View



Pin Information

Pin	Pin Description	Pin Function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Source	Source
8,10,12-20,22,24	Drain	Power Drain

Ordering Information

Ordering Part Number	Package Type	Form	Shipping Quantity
AOFQ018V10GA1	FCQFN 4X6	Tape and Reel	1500

Contact local sales office for full product datasheet.

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	AOFQ018V10GA1	Units
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage (up to 300,000 5ms pulse at 150 ˚C)	120	

Absolute Maximum Ratings

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	AOFQ018V10GA1	Units
I_D	Continuous current	100	A
	Pulsed (25°C, T_{Pulse} = 100 µs)	320	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

Symbol	Parameter	Typ	Note	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	13.96		°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	1.92		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (1)	57.56		
T_{sold}	Maximum Reflow Soldering Temperature	260	MSL3	°C

Note:

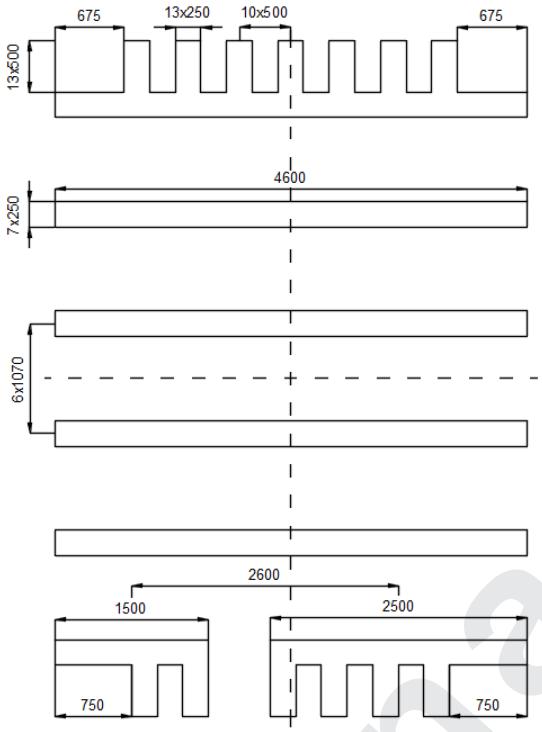
1. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Electrical Characteristics

(T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 900 µA	100	-	-	V
I_{DSS}	Drain Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V	-	9.5	93	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V	-	2.8	55	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V	-	0.3	1.2	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 21 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On-state Resistance	VGS = 5 V, I_D = 40 A	-	1.4	1.8	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V	-	1.5	-	V
DYNAMIC						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V	-	2500	-	pF
C_{OSS}	Output Capacitance	V_{GS} = 0 V, V_{DS} = 50 V	-	1100	-	
C_{RSS}	Reverse Transfer Capacitance	V_{GS} = 0 V, V_{DS} = 50 V	-	19	-	
$C_{OSS(ER)}$	Energy Related COSS	V_{GS} = 0 V, V_{DS} = 0 V to 50 V	-	1700	-	
$C_{OSS(TR)}$	Time Related COSS	V_{GS} = 0 V, V_{DS} = 0 V to 50 V	-	2500	-	
R_G	Gate resistance	f = 5 MHz, open drain	-	1.8	-	Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, v = 50 V, I_D = 40 A	-	22	-	nC
Q_{GS}	Gate to Source Charge	V_{GS} = 50 V, I_D = 40 A	-	4.5	-	
Q_{GD}	Gate to Drain Charge	V_{GS} = 50 V, I_D = 40 A	-	4.5	-	
$Q_{G(TH)}$	Gate Charge at Threshold	V_{DS} = 50 V, I_D = 40 A	-	2.5	-	
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V	-	125	-	

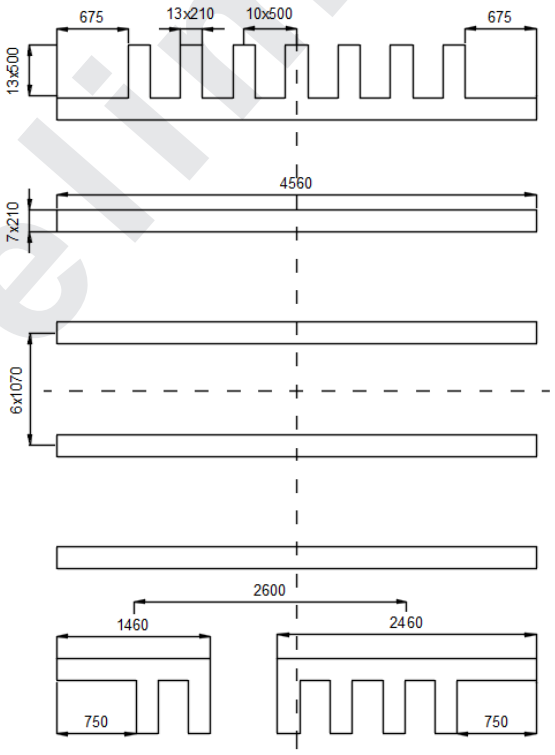
Recommended Land Pattern



Unit: μm

TOP VIEW

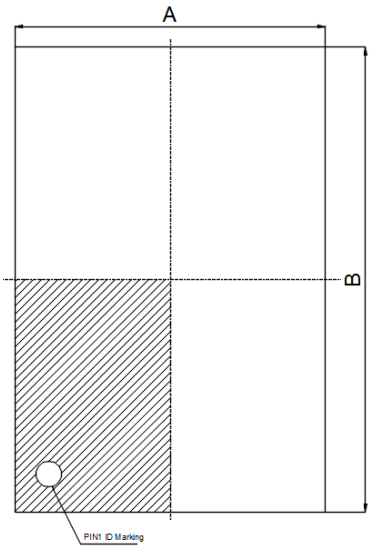
Recommended Stencil Drawing



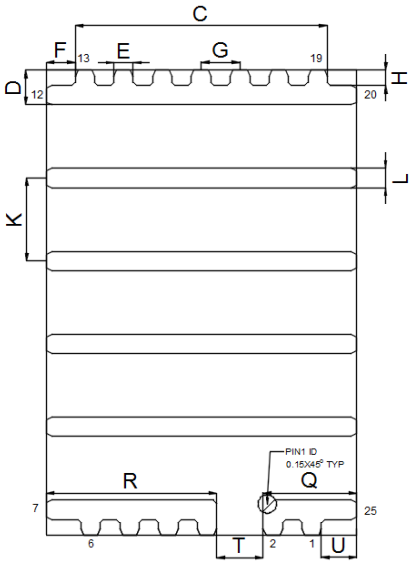
Unit: μm

TOP VIEW

Package Dimensions, FCQFN 4X6

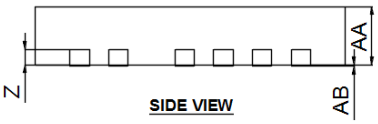


TOP VIEW



BOTTOM VIEW

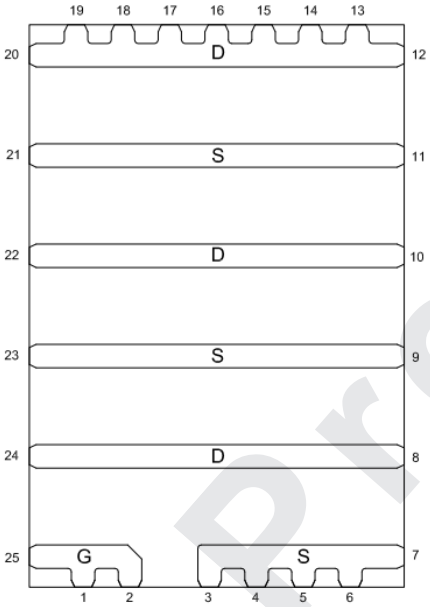
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	5.9	6.0	6.1	
C	3.15	3.25	3.35	
D	0.35	0.45	0.55	3X
E	0.20	0.25	0.30	13X
F		0.375 REF		2X
G		0.5 BASIC		10X
H		0.2 REF		3X
K		1.07 BASIC		6X
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
T	0.55	0.60	0.65	
U		0.45 REF		2X
Z		0.203 REF		7X
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	



SIDE VIEW

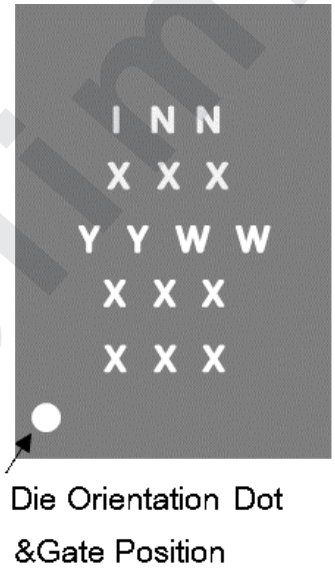
NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS FT TESTER SIDE VIEW.
3)LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-220.
5)DRAWING IS NOT TO SCALE.

Pin information:



TOP VIEW

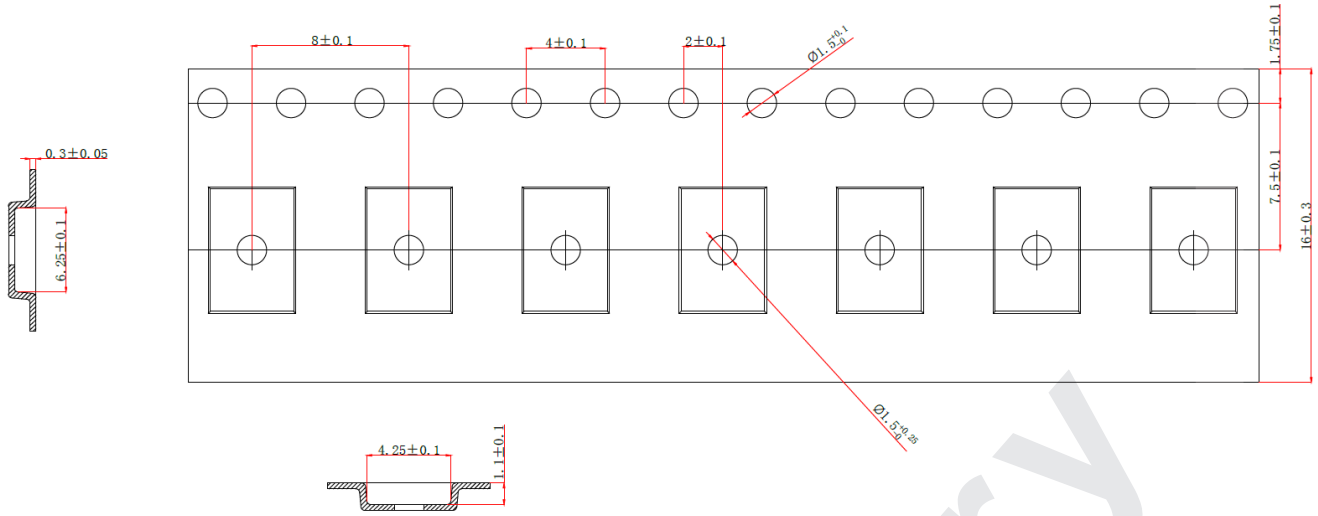
Marking Reference:



Die Orientation Dot
&Gate Position

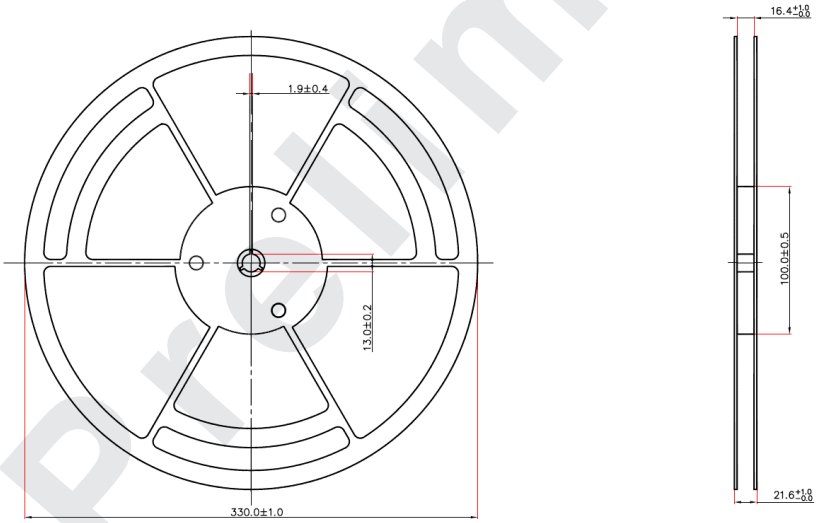
Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot No	XXX
Row 5	Lot No	XXX

Tape and Reel Dimensions, FCQFN 4X6

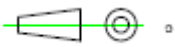


NOTES:

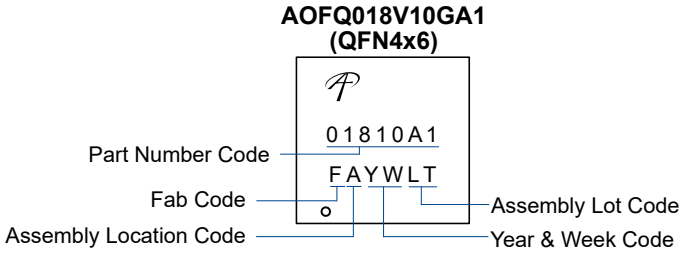
1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING



NOTES:

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW: 

Part Marking



LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. Alpha and Omega Semiconductor does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.